3D Vertical Integration Technologies for Advanced Semiconductor Radiation Sensors and Readout Electronics

Valerio Re
University of Bergamo
Department of Industrial Engineering, Viale Marconi, 5, Dalmine (BG), Italy
valerio.re@unibg.it

Abstract

The development of 3D vertical integration in the microelectronic industry brings along significant advantages for pixelated semiconductor radiation sensors in cutting-edge scientific experiments at high luminosity particle accelerators and advanced X-ray sources. These applications set very demanding requirements on the performance of sensors and their readout electronics, in terms of pixel pitch, radiation tolerance, signal-to-noise ratio and capability of handling very high data rates. 3D vertical integration of two or more layers with sensors and CMOS devices naturally leads the designer towards extending pixel-level processing functionalities and achieving novel structures where each layer is optimized for a specific function. This paper reviews the efforts towards the development of novel vertically integrated pixel sensors and discusses the challenges that are being tackled to qualify these devices for actual applications.

Introduction

Nowadays 3D vertical integration technology is already playing an important role in the design of advanced silicon pixel sensors for commercial imaging applications. The performance of imaging devices can be greatly enhanced by the high-density interconnection of two or more layers with CMOS sensor and advanced readout electronics, which can be thinned for backside illumination and tiled to achieve a large area coverage with no dead regions [1].

In the past few years, the developments in this field have suggested that 3D integration could bring along a performance leap for semiconductor radiation detectors in future high energy physics experiments at particle accelerators [2]. In these applications, a fundamental problem will be the reconstruction of charged particle tracks with high resolution pixelated sensors. These sensors, along with the readout electronics, will be required to have a small pixel pitch ($\leq$ 20 μm in some applications), a high degree of radiation tolerance, a large signal-to-noise ratio, a low mass to minimize particle scattering, a low power dissipation and the capability of handling very high data rates. To meet the requirements of these applications, advanced functions have to be performed in the electronics elementary cell of each pixel to cope with signal-to-noise ratio and high data rate requirements. These functions include amplification, filtering, calibration, discriminator threshold adjustment, analog-to-digital conversion, zero suppression (also called data sparsification) and time stamping. 3D integration can be a solution to the problem of integrating all these functions inside a small pixel, avoiding the use of aggressively scaled CMOS, below 100 nm feature size, which can be expensive and challenging for analog circuit design.

Two main research lines and technical solutions are being followed to exploit 3D vertical integration in high energy physics. The first one can be seen as a development of the classical CMOS MAPS (Monolithic Active Pixel Sensors) concept of signal charge generation and collection by diffusion in an undepleted silicon region. In this case, vertical integration of two (or more) CMOS layers makes it possible to separate the analog front-end electronics from the digital readout sections, with great advantages in terms of pixel size, functionalities and performance. Different readout architectures have been designed to handle a large data flow without the constraints that may arise when digital electronics is implemented on the same substrate as the sensor (as in standard MAPS).

The second research line explores the possibility of using 3D integration to interconnect layers fabricated in different technologies, i.e. to connect a sensor built in a fully-depleted high resistivity silicon substrate to readout electronics fabricated in a deep submicron CMOS process. This can provide a large benefit in terms of radiation hardness and signal-to-noise ratio.

Besides particle tracking in high energy physics experiments, imagers for advanced X-ray sources such as XFEL may also strongly benefit from the improved functionalities and performance that come along with vertical integration and allow for small pitch pixels capable of handling high data rates.

This paper will present a review of some of the ideas and of the devices that are being developed to satisfy the needs of these application with the help of 3D integration technologies. The main focus will be on the activities that are being carried out by the Italian R&D collaboration VIPIX funded by the Italian Institute of Nuclear Physics (INFN).

3D Monolithic Active Pixel Sensors

3D vertical integration technologies appear to be extremely attractive for the development of MAPS. In a standard MAPS, it is difficult to integrate advanced functionalities in the pixel cell, since PMOSFETs are avoided; they are located inside N-type wells which compete for charge collection with the signal electrode (also N-type), and degrade the fill factor. A multilayer sensor structure (with thin layers interconnected by vertical vias) promises to overcome this typical limitation of MAPS. In a 3D MAPS device, for example, a layer may host sensing electrodes and analog circuits, whereas digital electronics may be located in upper layers. In this way, it is possible to use a full CMOS electronics in the pixel cell, where most (if not all) the PMOSFETs and their competitive N-wells are removed from the sensor layer, in principle achieving a 100% fill factor. A multilayer structure allows also for a smaller pixel pitch and a

978-1-4577-0624-0/11/$26.00 ©2011 IEEE

smaller sensor capacitance, leading to a better trade-off between noise and power dissipation. The removal of layout constraints related to efficiency problems may also have a beneficial impact on the digital readout architecture, adding more complex functionalities and increasing flexibility.

The VIPIX collaboration is planning to apply 3D integration to Deep N-Well (DNW) MAPS [3]. In the pixel cell of these devices, the charge collecting electrode is the deep N-well that is available in modern CMOS processes. This electrode is extended over a relatively large fraction of the cell area. In this way, fully CMOS analog and digital circuit blocks can be used in the pixel, provided that the area of standard N-wells housing PMOSFETs is small compared to the deep N-well electrode, with which they compete for charge collection. A 3D implementation promises to deliver several important performance advantages to this kind of device. First of all, most (if not all) PMOSFETs with their competitive N-wells can be removed from the layer where the sensing electrode is located, improving the charge collection efficiency. Secondly, it appears possible to increase complexity and functionality in electronic readout circuits by exploiting the multilayer device structure [4].

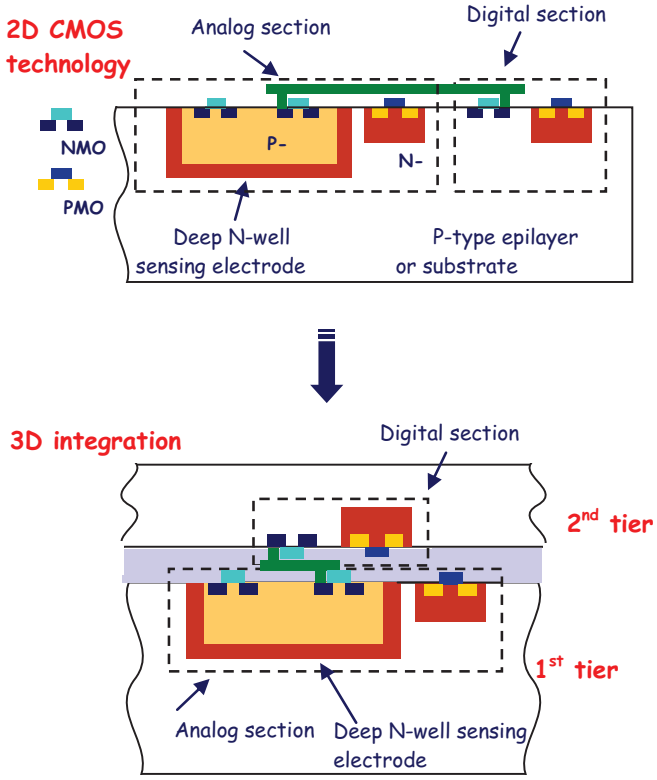

Figure 1: Evolution of a DNW MAPS from a standard 2D CMOS process to a 3D vertical integration technology.

For the VIPIX collaboration, the first step in the 3D direction has been the design of two-tier DNW MAPS by the face-to-face bonding of two 130 nm CMOS wafers with the vertical integration process by Tezzaron Semiconductor [5]. This is a so-called "via middle" approach to 3D integration, where the Through-Silicon Vias (TSVs) for vertical interconnection are etched in CMOS wafers just after transistor fabrication, before the process steps for the various metal interconnects. A high density of TSVs (with a pitch of a few μm) can be achieved with this kind of processing. The evolution of a DNW MAPS from a standard 2D CMOS process to a 3D technology is schematically shown by Figure 1. In the 3D device, the basic idea is to keep the DNW charge collecting electrode and the analog electronics section in the first layer, whereas the digital readout section is located in the second CMOS layer. A charge-sensitive preamplifier is the first stage of the analog section, so that the gain is set by its feedback capacitance and is instead independent of the value of the capacitance of the sensing electrode. After signal shaping and filtering, the signal is applied to the input of a discriminator providing a binary information (hit / no hit). The discriminator is located in the digital tier and is followed by a latch and by the sparsification and time stamping logic integrated in the pixel. Because of the functional density allowed by 3D integration, in the pixel cell it is possible to include a 4-bit digital-to-analog converter for a local correction of the threshold voltage. This makes it possible to reduce the threshold dispersion across the pixel matrix to an acceptable level.

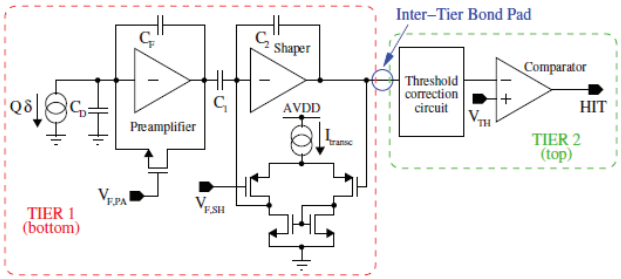

Figure 2: Block diagram of the front-end circuit for a 3D DNW MAPS.

Charge sensitivity	850 mV/fC
Peaking time	300 ns
Equivalent Noise Charge	35 e rms
Threshold dispersion after DAC correction	15 e rms
Analog power consumption	30 μW/pixel
Pixel array size	128 x 100
Pixel size	50 μm x 50 μm

Table 1: Main performance parameters of the 3D DNW MAPS prototype.

Fig. 2 shows the block diagram of the analog channel in this 3D MAPS design. In the digital tier, the pixel-level logic (not shown in Fig. 2) enables a sparsified, time-ordered triggered readout of the pixel matrix [6]. This feature is especially useful in applications of this device to vertex detectors in high energy physics experiments, where the so-called Level 1 Trigger signal is generated only when interesting physics events are detected. To accomplish this, a time stamp information is stored in the pixel and is compared to a time stamp provided by the triggering system and broadcasted to

the matrix by the readout blocks located in the chip periphery. Only pixels where the two time stamps are the same send a "data out" bit to the periphery, where their address is formatted and sent off-chip. This readout architecture allows a big reduction of the amount of information that has to be transmitted off-chip, relaxing the requirements of the on-chip data output interface. Table 1 summarizes the main performance parameters of the 3D DNW MAPS, that is currently at an advanced design stage.

A 3D CMOS readout chip for high resistivity, fully-depleted pixel sensors

The standard substrates or epitaxial layers of CMOS technologies have a relatively low resistivity as compared to the high resistivity bulk that is typical of dedicated fabrication processes for fully-depleted pixel sensors. This results in a higher sensitivity of CMOS sensors to the bulk damage that can be caused by hits from massive particles (e.g., neutrons and heavy ions) in high energy physics or space applications. In this case, it is mandatory to use high resistivity pixel detectors, which are more tolerant to displacement damage because charge collection is governed by a drift process, and not by a diffusion one as in the undepleted epitaxial layer of standard CMOS sensors [7].

Vertical integration can be used to interconnect layers fabricated in different technologies, e.g. to connect a sensor built in a fully-depleted high resistivity silicon substrate to readout electronics fabricated in a commercial ultra deep submicron process. Note that the readout electronics itself may already be produced in a 3D process, as in the example shown in Figure 3. The challenge then is the formation of a strong, reliable, low-mass bond between the sensor and the readout electronics. For high energy physics applications, several 3D techniques have been explored for sensor and readout integrated circuit integration to overcome the limitations of standard bump bonding technology in terms of pitch and of material [2]. A decrease of the amount of material in the system is crucial to reduce errors in track reconstruction due to multiple scatterings of particles in the detectors.

Fig. 4 shows the schematic of the pixel cell that the VIPIX collaboration is presently integrating in a 3D chip for the readout of a 32x128 high resistivity pixel matrix. This is quite similar to the readout scheme of the MAPS device in Fig. 2, with preamplifier and shaper in the first (analog) tier, and the discriminator with the DAC for threshold adjustment in the second (digital) tier. The in-pixel logic and the global readout architecture are also the same as for the 3D MAPS. However, there are some important differences in the design of the analog blocks, as dictated by the different parameters of the sensor. In a CMOS sensor, signal charge is collected in a layer of a thickness of the order of 10-15 μm, and seldom exceeds 1000 electrons. Instead, the entire bulk (of a typical thickness of 100-300 μm) of a fully-depleted high resistivity pixel sensor delivers the charge carriers generated by radiation to the collecting electrodes. In the case of the minimum ionizing particles that are relevant for high energy physics experiments, this gives a considerably larger signal than in MAPS. It is then possible to relax the requirements on the noise and the threshold dispersion, which allows the analog pixel cell to operate at a lower power dissipation. This is apparent in Table 2, showing the main simulation parameters for the 3D CMOS readout chip that is currently being designed by the VIPIX collaboration.

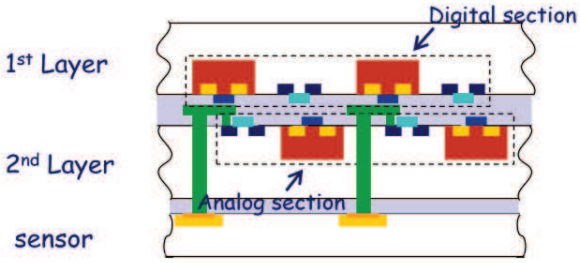

Figure 3: Concept for the interconnection between a 3D CMOS readout chip and a high resistivity pixel sensor.

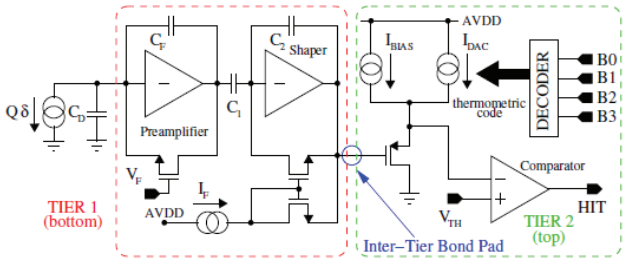

Figure 4: Block diagram of the front-end circuit in the 3D CMOS chip for the readout of high resistivity pixel sensors.

Charge sensitivity	50 mV/fC
Peaking time	250 ns
Equivalent Noise Charge	130 e rms (for an estimated capacitance of sensor and strays of 150 fF)
Threshold dispersion after DAC correction	65 e rms
Analog power consumption	30 μW/pixel
Pixel array size	128 x 32
Pixel size	50 μm x 50 μm

Table 2: Main performance parameters of the 3D CMOS chip for the readout of high resistivity pixel sensors.

Status of the R&D on 3D integration for semiconductor pixel radiation sensors

To meet the challenges associated with design, fabrication and testing of 3D vertically integrated pixel sensors, the radiation detector community has organized itself in various consortia, with the goal of tackling different technologies and design solutions. The 3D-IC Consortium [8] was promoted by Fermi National Accelerator Laboratory to explore various issues associated to vertical integration. European and U.S. institutions are presently members of this Consortium, which, as a first step, is going to investigate 3D devices based on two layers ("tiers") of the 130 nm CMOS technology by

GlobalFoundries, vertically integrated with the previously described Tezzaron interconnection technology.

The 3D MAPS and the 3D CMOS readout chip that were discussed in the previous sections are presently (June 2011) at an advanced design stage. However, the submission and fabrication of these devices will be put on hold, waiting for the experimental results from the first 3D prototypes that the 3D-IC consortium submitted to Tezzaron in a 2009 multiproject wafer (MPW) run. The 130 nm CMOS wafers from this run were fabricated by GlobalFoundries; one of these wafers was diced before the 3D interconnection, so that it was possible to test separately analog and digital circuits in the two tiers. All these tests were successful, showing that the various blocks are fully functional; a DNW MAPS structure was also tested with radioactive sources, proving that the substrate of these CMOS devices is able to detect ionizing particles [9]. In May 2011, wafer bonding and interconnection was performed by Tezzaron; remaining 3D process steps (thinning and backside metallization) are expected to take place soon, so that the first 3D chips can be tested and give the green light for the next 3D-IC MPW run, with the larger structures described above. This new run will be managed by the MOSIS and CMP MPW services [10]. A possible target application for the two 3D devices by the VIPIX collaboration is the Silicon Vertex Tracker in the SuperB particle accelerator that is soon going to begin the construction phase in Italy [9].

Another 3D-related initiative is taking place in the frame of the AIDA project, a EU-funded FP7 program addressing infrastructures for detector development for future particle physics experiments. In AIDA, WorkPackage3 aims to establish a network of groups from European universities and high energy physics research institutes working collaboratively on 3D integration technology for thin pixel sensors with complex pixel-level functionality, with small pixel size and without dead regions. A major goal of AIDA WP3 is to build a demonstrator based on 3D integration. WP3 plans to follow a "via last " approach to 3D integration to build a 2-layer device in heterogeneous technologies (e.g., high-resistivity pixel sensors and CMOS readout chips). In a "via last" 3D process, TSVs are fabricated on fully processed CMOS wafers [11]. The density of vertical interconnections is in this case considerably smaller (more than one order of magnitude) than for a "via middle" process. However, the "via last" approach can be useful when vertical interconnections are needed only in the peripheral regions of the chips, close to bonding pads for external connection.

Conclusions

3D integration is stimulating new concepts in the field of radiation detectors and readout electronics, and substantial performance breakthroughs appear to be achievable with this technology. This extends also to data acquisition systems for large tracking detectors, where 3D associative memories are planned for a very fast and efficient reconstruction of particle tracks [12]. So far, progress in R&D activities is generally slow, also because of industry trends in the semiconductor market. However, the expanding interest of the sensor community and the exploration of different technologies are expected to lead very soon to 3D integrated circuits and radiation sensors working in real applications, especially where there is a need for small pitch pixels that are capable of handling high data rates.

Acknowledgments

The author acknowledges the hard and successful work towards the development of 2D and 3D DNW MAPS and of 3D CMOS readout chips that was carried out by the SLIM5 and VIPIX Italian collaborations funded by INFN.

References

1. Garrou, P., *et al*, Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits, Wiley-VCH (Weinheim, 2008).
2. Demarteau, M. *et al*, "Developments of novel vertically integrated pixel sensors in the high energy physics community", *Proc. 2009 IEEE International Conference on 3D System Integration (3D-IC),* San Francisco, CA, September 28-30, 2009, pp. 1-7.
3. Ratti, L., *et al*, "Monolithic pixel detectors in a 0.13 μm CMOS technology with sensor level continuous time charge amplification and shaping", *Nucl. Instr. Meth.*, vol. A568 (2006), pp. 159-166.
4. Ratti, L., *et al*, "Vertically integrated deep N-well CMOS MAPS with sparsification and time stamping capabilities for thin charged particle trackers", *Nucl. Instr. Meth.*, vol. A624 (2010), pp. 379-386.
5. Patti, R. S., "Three-Dimensional Integrated Circuits and the Future of System-on-Chip Design", *Proceedings of the IEEE*, vol. 94, No. 6 (2006), pp. 1214-1224.
6. Re, V., "Towards a high performance vertex detector based on 3D integration of deep N-well MAPS", *Journal of Instrumentation*, vol. 5, (2010), C06002, doi: 10.1088/1748-0221/5/06/C06002, pp. 1-6.
7. Wermes, N., "Pixel detectors for charged particles", *Nucl. Instr. Meth.*, vol. A604 (2009), pp. 370-379.
8. Yarema, R., "3D design activities at Fermilab – Opportunities for physics", *Nucl. Instr. Meth.,* vol. A627 (2010), pp. 375-377.
9. Re, V., "Advanced pixel sensors and readout electronics based on 3D integration for the SuperB Silicon Vertex Tracker", to be published in *Proc. 2011 Conference on Technology and Instrumentation in Particle Physics*, Chicago, IL, June 9-16, 2011.
10. Torki, K., "Design platforms and tools for 3D IC integration", *Proc. 2010 IEEE International Conference on 3D System Integration (3D-IC),* Munich, Germany, November 16-18, 2010, pp. 1-7.
11. Moser, H.-G., "3D technology developments in Europe and European Union supported efforts", to be published in *Proc. 2011 Conference on Technology and Instrumentation in Particle Physics*, Chicago, IL, June 9-16, 2011.
12. Hoff, J. *et al*, "A new concept to use 3D vertical integration technology for fast pattern recognition", to be published in *Proc. 2011 Conference on Technology and Instrumentation in Particle Physics*, Chicago, IL, June 9-16, 2011.