

# Signal and Noise Performance of a 110-nm CMOS Technology for Photon Science Applications

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**Abstract**—This paper presents a study of the noise behavior of MOSFET devices belonging to a 110-nm CMOS technology in view of applications to the design of low-noise, low-power analog circuits in X-ray detection at free electron lasers (FELs) and the next generation of synchrotrons. The goal of this paper is to provide a valuable and cost-effective option, with respect to more scaled and expensive technology nodes, to designers of the detection systems of FELs and next-generation synchrotron sources. The white component of the noise voltage spectrum and the  $1/f$  noise contribution is experimentally characterized by noise measurements in a wide frequency range. Data extracted from the characterization have been studied as a function of the bias condition and the gate dimensions (length and width). A comparison of the main parameters with less and more scaled CMOS generations is also provided.

**Index Terms**— $1/f$  noise, channel thermal noise, CMOS, device scaling, front-end electronics.

## I. INTRODUCTION

THE investigation of the extremely small and the extraordinarily fast phenomena that take place at the nanometer scale is one of the main trends of modern scientific research. As an example, free electron lasers (FELs) are bound to become the predominant tool for the investigation of natural phenomena in this research field [1]. The minimum wavelength, of the order of one Ångström, and the intensity of the laser beam available in FEL systems make possible to see objects with subnanometer feature size. A number of research centers, in Europe, the United States, and Japan, have started studying, designing, and building FEL facilities [2], [3]. Each of them features several numbers of beamlines, providing photons with wavelengths spanning from atomic level to biological cell size, which can be used as probes for advanced research in material science, physical, and chemical science and in the medical and pharmaceutical fields. Dedicated detection systems, tailored to meet the specific requirements of the respective light source, are under development for photon science at these brilliant XFEL light sources [4]–[9]. Several readout systems under development are based on the 130-nm CMOS technology node. In high energy

physics (HEP), on the contrary, the readout chips for the upgraded tracking pixel detectors at the high-luminosity (HL) LHC are being designed in a 65-nm CMOS technology. In 2013, the RD53 collaboration was established with the purpose of developing pixel readout integrated circuits (ICs) for the next generation of pixel readout chips to be used for the ATLAS and CMS Phase 2 pixel detector upgrades and future CLIC pixel detectors [10]. Tolerance to extremely high levels of ionizing radiation is a key requirement for both application fields (namely, HL-LHC experiment upgrades and photon science at very high-brilliance XFEL machines). It is estimated that during their operational lifetime these pixel readout chips should be able to stand a total ionizing dose (TID) up to 1 Grad(SiO<sub>2</sub>), keeping the essential performance parameters at the required values [11], [12]. These TID levels are unprecedented in the field of readout electronics for particle detectors, and several studies are being carried out to understand how CMOS transistors and ICs behave after the exposure to extremely high doses. These studies pointed out degradation effects that are especially critical for transistors with gate length and width approaching the minimum values allowed by the technology, which are mostly of interest for digital circuits.

A new CMOS technology node, with a minimum channel length of 110 nm, is of interest and it is being used in the design of a detector for FEL experiment applications [13], [14]. It has a higher integration density with respect to the 130-nm process currently used, and with respect to the more scaled 65-nm CMOS node, it provides a better size-over-cost ratio. The reason for this advantage is twofold. First, the analog section does not take advantage as digital circuits from device scaling. Second, front-end circuits, both analog and digital parts, designed in 65 nm avoid using the device with minimum size to improve the radiation hardness and to guarantee the functionality during the entire lifetime [15], [16]. This paper aims at presenting and discussing some of the analog performance of a 110-nm CMOS technology being used for the design of the detection system of FELs and next-generation synchrotron sources. The behavior of the  $1/f$  and white noise term is studied and compared with less and more scaled CMOS nodes. A preliminary radiation hardness study on this technology, not included in this paper, has already been carried out with promising results [17].

## II. EXPERIMENTAL DETAILS

The 110-nm CMOS transistors studied in this paper belong to a process developed by a commercial vendor

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TABLE I  
GATE GEOMETRIES OF THE AVAILABLE n-CHANNEL AND p-CHANNEL  
DEVICES. OPTION AVAILABILITY IS INDICATED WITH \* SYMBOL

$W[\mu m]$	$L[\mu m]$	Core Open		Core ELT	
		N	P	N	P
90	0.120	*	*		
	0.228	*	*		
	0.336	*	*		
	0.660	*	*		
180	0.120	*	*	*	
	0.228	*	*	*	
	0.336	*	*	*	
	0.660	*	*	*	
540	0.120	*	*	*	
	0.228	*	*	*	
	0.318				
	0.336	*	*		
	0.345				
	0.660	*	*	*	

(named Foundry A) for mixed-signal and RF applications, with a maximum allowed supply voltage  $V_{DD}$  of 1.2 V for core devices. For the standard performance (SP) flavor selected in this paper, the electrical gate oxide thickness is 2.64 nm for nMOS and 2.83 nm for pMOS. The corresponding effective gate capacitances per unit area are 13.1 and 12.2 fF/ $\mu m^2$ . Two types of devices are available for measurements as follows.

- 1) *Core Devices With Open Layout*: The MOSFETs are laid out using a standard open structure, interdigitated configuration, with gate finger width of  $W_f = 18 \mu m$ , with the exception of the nMOS with  $W/L = 540/0.12$  which is available also with  $W_f = 9$  and  $36 \mu m$ .
- 2) *Core Devices With Enclosed Layout*: The nMOS devices are designed with an enclosed layout (ELT). Ten parallel devices are used for each geometry. ELT devices have been included to evaluate their performance, together with standard layout transistors, after irradiation with ionizing sources.

For each option, gate dimensions (width  $W$  and length  $L$ ) of devices available for measurements are shown in Table I. This is a 130-nm-shrunk technology node, in which all drawn dimensions are reduced, by means on an optical step, of about 10%. All dimensions reported in this paper are physical dimensions after shrink and not as-drawn dimensions. The MOSFETs have been provided in 44 pins *ceramic leadless chip carrier* (LCC) with taped (removable) lid. A total of eight samples are available in-package. As mentioned in Section I, this paper does not deal with radiation hardness study and, therefore, only measurements on core devices are shown. For comparison purposes, this paper also reports data relevant to other CMOS processes with a minimum gate length of 65 and 130 nm. These technologies are of particular interest for different reasons. The 130-nm node, along with having a minimum channel length comparable to the one of the technologies investigated in this paper, as said previously, has been extensively used in the design of front-end electronics in some of the readout ASICs for imaging applications at the European XFEL. The 65-nm node, instead, is currently the

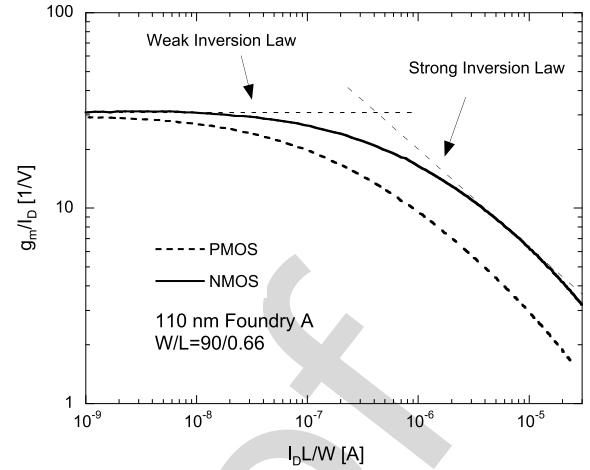


Fig. 1. Transconductance efficiency  $g_m/I_D$  as a function of the normalized drain current  $I_D/L/W$  for an nMOS transistor belonging to the investigated 110-nm CMOS process. The measurement was performed at a drain-to-source voltage  $V_{DS} = 1.2$  V. The theoretical behavior of transconductance efficiency in weak and strong inversion regions is also shown with a dashed line.

workhorse of the development of front-end electronic systems in HEP applications. The 130-nm devices are provided by a second vendor (Foundry B) in a general purpose (GP) flavor. The 65-nm MOSFETs belong to a low power (LP) process developed by a third vendor (Foundry C) and used by the RD53 collaboration for the development of pixel readout ICs for the Phase 2 pixel detector upgrades.

### III. EXPERIMENTAL RESULTS

#### A. Static Measurements

Measurements of static and signal parameters were carried out with an Agilent E5270B Precision Measurement Mainframe with E5281B SMU modules. For core and ELT devices,  $I_D$ - $V_{GS}$  and  $I_D$ - $V_{DS}$  characteristics have been measured with a gate-to-source voltage  $V_{GS}$  ranging from -0.3 to 1.4 V and a drain-to-source voltage ranging from 0 to 1.4 V. Device behavior with a negative gate-to-source voltage has been investigated in order to better evaluate the device leakage current in the OFF-state. Data collected in this leakage current zone are of particular interest for a comparison with data collected after irradiation in order to evaluate the total ionization dose effects on the investigated technology. Moreover, a maximum voltage of 1.4 V, thus exceeding the maximum value recommended by the technology, has been applied because this value is currently used to bias analog circuits in some undergoing designs [13], [14].

The value of the transconductance  $g_m$  was extracted from  $I_D$ - $V_{GS}$  curves to evaluate the devices operating region and the relevant inversion coefficient. The actual inversion level of a MOS transistor primarily controls the transconductance efficiency, which is defined as the ratio between the transconductance  $g_m$  and the drain current  $I_D$ . Fig. 1 shows a comparison of the transconductance efficiency of nMOS and pMOS devices belonging to the 110-nm technology node as a function of the normalized drain current. In the weak inversion region, the transconductance efficiency is maximum and its slope is

TABLE II  
CHARACTERISTIC NORMALIZED DRAIN CURRENT  $I_Z^*$  [ $\mu\text{A}$ ]

	65 nm (LP)	110 nm (SP)	130 nm (GP)
	Foundry C	Foundry A	Foundry B
NMOS	0.49	0.41	0.55
PMOS	0.15	0.11	0.15

zero, because  $g_m$  is proportional to the drain current. In strong inversion, the slope of  $g_m/I_D$  on a log scale is  $-1/2$ , because the transconductance is proportional to the square root of the drain current and drops even faster for short channel devices due to velocity saturation. Between weak and strong inversion regions, one can use the EKV model to describe the ratio between the transconductance and the drain current [18]

$$\frac{g_m}{I_D} = \frac{1}{\sqrt{(I_D/I_Z^*) + 1/2}\sqrt{(I_D/I_Z^*) + 1}} \frac{1}{n\phi_t} \quad (1)$$

where  $n$  is a coefficient proportional to the inverse of the subthreshold slope of  $I_D$  as a function of  $V_{GS}$ ,  $\phi_t = k_B T/q$  is the thermal voltage ( $k_B$  is Boltzmann's constant,  $T$  is the absolute temperature, and  $q$  is the electron charge).  $I_Z^*$ , the normalized drain current, is located at the intersection of the weak and strong inversion asymptotes and can be used to better evaluate the effect of technology variations on the inversion level of MOS devices. This parameter can be defined as [19]

$$I_Z^* = 2\mu C_{OX} n \phi_t^2 \quad (2)$$

where  $\mu$  is the channel mobility, and  $C_{OX} = \epsilon_{OX}/t_{OX}$  is the gate oxide capacitance per unit area ( $\epsilon_{OX}$  is the permittivity of silicon dioxide and  $t_{OX}$  is the oxide thickness).  $I_Z^*$  sets the boundary between weak and strong inversion and, according to (2), is expected to be larger in nMOS and in devices fabricated in processes with smaller minimum feature size. Therefore, the weak and moderate inversion regions extend to higher normalized drain currents in the most advanced CMOS generations. Although the evaluation of the normalized drain current can be affected by several design dependent parameters such as the parasitic series source and drain resistances and by short channel effects, an estimation of  $I_Z^*$  obtained for core devices biased at  $V_{DS} = 1.2$  V is reported in Table II. Starting from  $I_Z^*$ , a numerical method for quantifying the inversion level of the channel at a given current can be worked out by means of the inversion coefficient,  $I_{C0}$ , which is defined as

$$I_{C0} = \frac{I_D}{I_Z^*} \frac{L}{W}. \quad (3)$$

According to (3), at the center of moderate inversion, that is, at  $I_D L/W = I_Z^*$ , the inversion coefficient is equal to 1; under the hypothesis that the moderate inversion region extends one decade before and one decade after  $I_Z^*$ , the weak inversion region can be assumed to take place for devices with an inversion coefficient smaller than 0.1, whereas the strong inversion approximation is valid for devices with an inversion coefficient greater than 10. Both the plots in Fig. 2, which show the inversion coefficient as a function of the drain current obtained from measurements on nMOS and pMOS devices

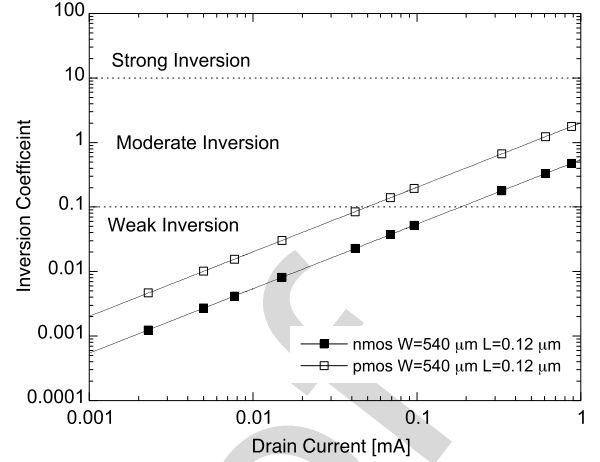


Fig. 2. Inversion coefficient as a function of the drain current of 110-nm transistors with gate width  $W = 540 \mu\text{m}$  and gate length  $L = 0.12 \mu\text{m}$ .

with gate width  $W = 540 \mu\text{m}$  and gate length  $L = 0.12 \mu\text{m}$ , and the values of  $I_Z^*$  reported in Table II show that, under reasonable power dissipation constraints, in the 110-nm node, the preamplifier input device operates in the weak inversion region. For comparison purpose, values obtained for other CMOS processes are also reported in Table II [20]. It can be seen that the normalized drain current does not scale with the technology node as expected. In particular, the 110-nm technology exhibits a lower  $I_Z^*$  with respect to the 130-nm node. This effect can be related to the different flavors of the investigated processes.

## B. Noise Measurements Results

The power spectral density of the noise in the channel current of the device under test was studied by measuring the equivalent noise voltage spectrum referred to the gate. These measurements were carried out with a network/spectrum analyzer (Agilent 4395A) and a purposely developed interface circuit which allows for DUT noise amplification in the 1-kHz–100-MHz frequency range [21]. A large set of noise measurements was carried out to study the behavior of white and  $1/f$  noise components of the spectrum as a function of gate geometry, device polarity, and drain current. All the devices were characterized at  $|V_{DS}| = 0.6$  V and  $V_{BS} = 0$  V. In order to evaluate the impact of the bias conditions on the noise, the MOSFETs were biased at a drain current  $I_D$  ranging from 20 to 500  $\mu\text{A}$  during the noise measurements. This low current density region is of major concern for low-power applications. The plots in Figs. 3–5 compose a typical set of experimental results concerning n-channel and p-channel devices belonging to the 110-nm CMOS technology. The plots in Fig. 3 show noise voltage spectra relevant to nMOS and pMOS devices with fixed gate width  $W$  and a different gate length  $L$ , biased at the same drain current. Since the devices are close to weak inversion, white noise is almost unaffected by  $L$  variations, whereas, at low frequencies,  $1/f$  noise increases with decreasing  $L$ . Fig. 4 shows the dependence of the noise voltage spectrum on the gate width for nMOS and pMOS devices. It can be observed that  $1/f$  noise increases

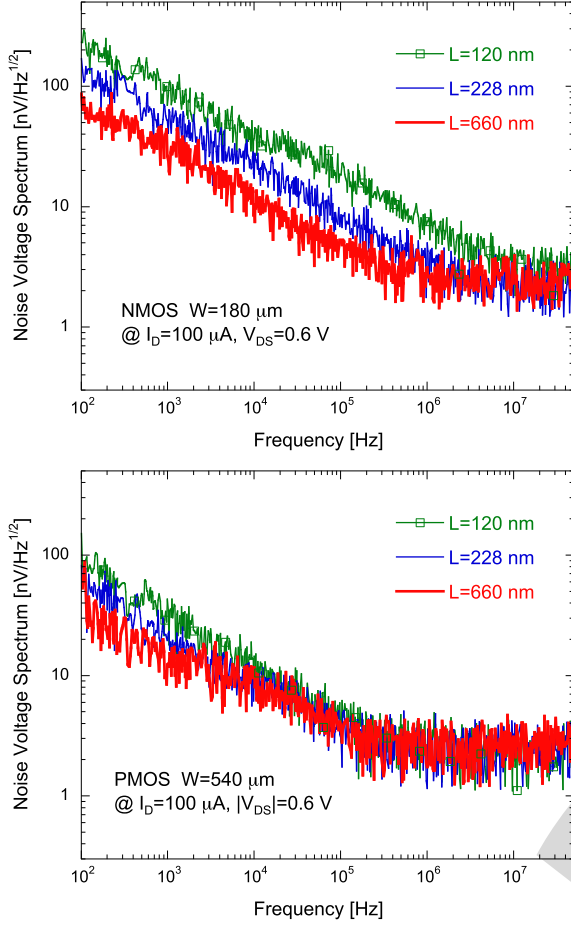


Fig. 3. Noise voltage spectra of nMOS (top) and pMOS (bottom) devices for a different channel length  $L$ .

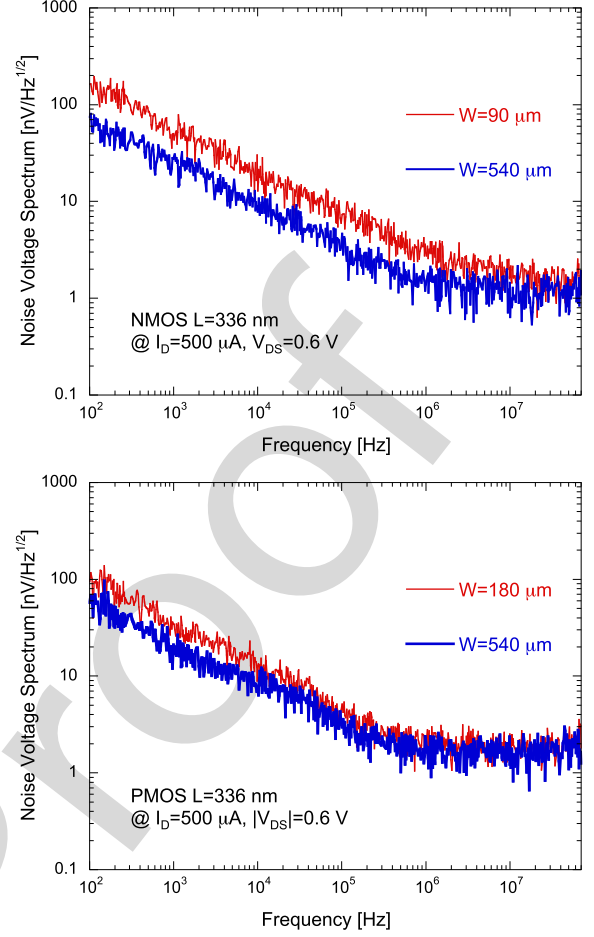


Fig. 4. Noise voltage spectra of nMOS (top) and pMOS (bottom) devices for a different channel width  $W$ .

with decreasing  $W$ , instead, channel thermal noise is not sizably affected by  $W$  variations. The plots of Fig. 5 show the effect of drain current variations on the noise voltage spectra of an nMOS and a pMOS. Channel thermal noise is reduced by increasing  $I_D$  since the transconductance correspondingly increases. On the other hand, the  $1/f$  noise component is not sizably affected by  $I_D$  variations in agreement with the carrier number fluctuation model, proposed by Mc Whorter [22] to describe the origin of the flicker noise in MOS devices.

### C. Analysis of White and $1/f$ Noise Parameters

In this section, the behavior of the  $1/f$  and white noise parameters is studied as a function of the device polarity and of the gate length and width. The gate referred noise voltage spectrum of a CMOS device  $S_e^2(f)$  can be modeled by means of the following equation:

$$S_e^2(f) = S_W^2 + S_{1/f}^2(f). \quad (4)$$

The first term in (4) describes the white component of the spectrum which is determined by channel thermal noise and noise contributions from parasitic resistances (gate, bulk, and source/drain resistance), which also exhibit thermal noise. In the low current density operating region, it can be demonstrated that the white noise voltage spectrum  $S_W^2$  is dominated

by channel thermal noise and can be expressed by means of its equivalent noise resistance [23]

$$R_{eq} = \frac{S_W^2}{4k_B T} = \alpha_W \frac{n\gamma}{g_m} \quad (5)$$

where  $\alpha_W \geq 1$  is an excess noise factor and  $\gamma$  is a coefficient which accounts for the inversion level of the channel and ranges from  $1/2$  in weak inversion to  $2/3$  in strong inversion. Starting from the analysis of the inversion coefficient described in Section III-A,  $\gamma$  can be calculated according to the following relationship for each  $I_D$  value [24]:

$$\gamma = \frac{1}{1 + \frac{I_D L}{I_Z^* W}} \left[ \frac{1}{2} + \frac{2}{3} \frac{I_D L}{I_Z^* W} \right]. \quad (6)$$

The second term in (4) is given by flicker noise in the channel current and is characterized by a power spectral density that is proportional to the inverse of the frequency as described by the following relationship [23]:

$$S_{1/f}^2(f) = \frac{K_f}{C_{OX} W L} \frac{1}{f^{a_f}} \quad (7)$$

where  $K_f$  is an intrinsic process parameter and the exponent  $a_f$  determines the slope of this low-frequency noise term. It has to be noted that, in order to be consistent with the carrier



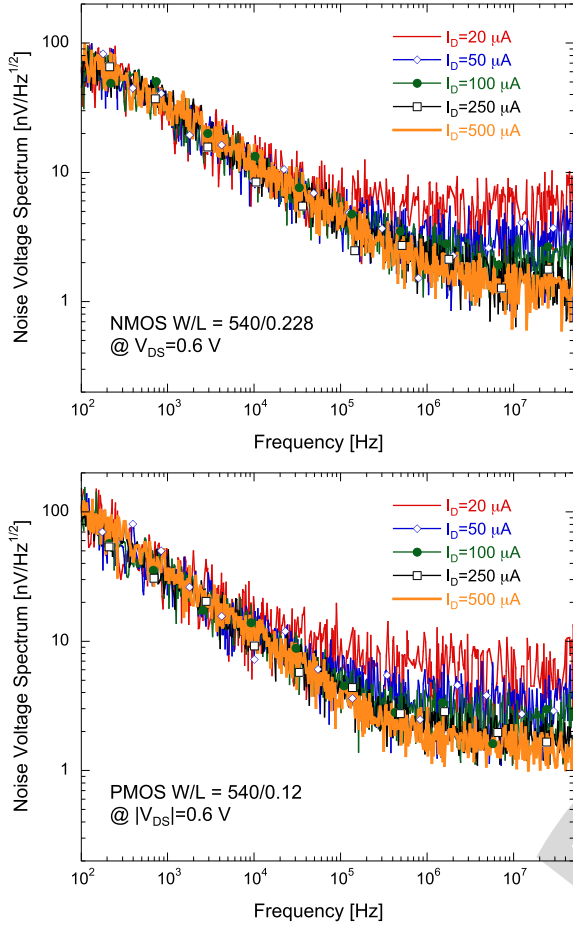


Fig. 5. Noise voltage spectra of nMOS (top) and pMOS (bottom) devices at different values of drain current.

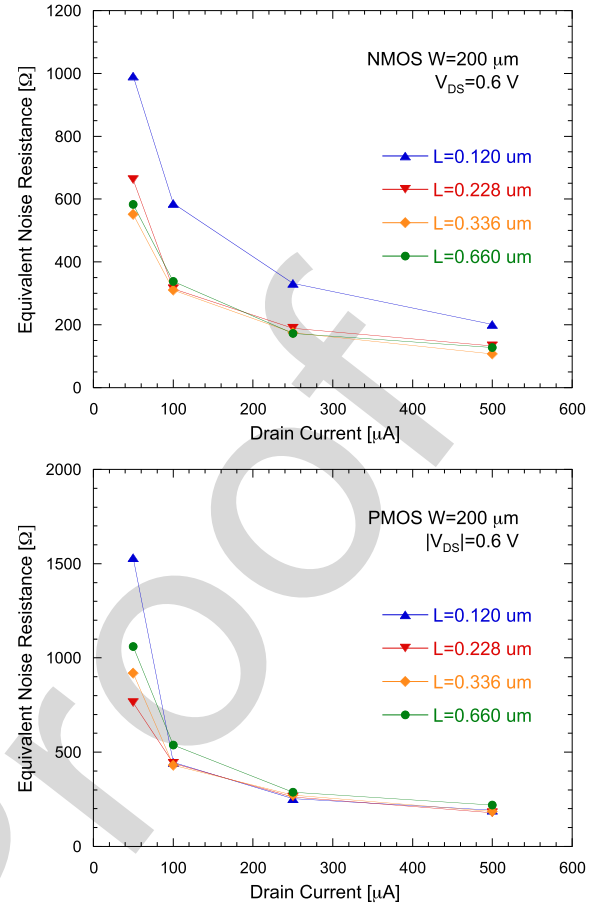


Fig. 6. Equivalent noise resistance  $R_{eq}$  for nMOS (top) and pMOS (bottom) devices with various geometries, as a function of the drain current.

number fluctuation model mentioned earlier, the  $K_f$  parameter in (7) has to be intended as the ratio between the  $K_a$  coefficient defined in the Mc Whorter model and the  $C_{ox}$  [25].

White noise is evaluated in terms of the equivalent channel thermal noise resistance  $R_{eq}$  defined in (5). The plots in Fig. 6 show the equivalent channel thermal noise resistance behavior, obtained for nMOS and pMOS devices with fixed gate width  $W$  and a different gate length  $L$ , as a function of the drain current. White noise decreases with the increase of  $I_D$ , due to the increase of  $g_m$ , whereas it is not sizably affected by  $L$  and  $W$  variations since devices are operated in weak inversion. Only devices with minimum channel length exhibit an excess of channel thermal noise. Fig. 7 shows values of  $R_{eq}$  as a function of  $n\gamma/g_m$  extracted for nMOS and pMOS devices with different gate geometries. A typical value of the subthreshold slope  $n=1.2$  is assumed, whereas the coefficient  $\gamma$  is calculated for each  $I_D$  value by means of (6) and values of  $I_{z,n}^*=0.41 \mu A$  and  $I_{z,p}^*=0.11 \mu A$  are reported in Table II. According to (5), the slope of the linear fit (straight line in the plots) is determined by the coefficient  $\alpha_W$ , whereas the offset is due to contributions from parasitic resistances. Measurements showed values of  $\alpha_W$  close to unity for all the measured devices with the exception of nMOS devices with the minimum feature size allowed by the technology

TABLE III

SLOPE COEFFICIENT OF THE  $1/f$  NOISE TERM EXTRACTED FROM DIFFERENT TECHNOLOGY NODES AND FOUNDRIES

	65 nm (LP) Foundry C	110 nm (SP) Foundry A	130 nm (GP) Foundry B
NMOS	0.93	0.93	0.85
PMOS	1.01	1.02	1.19

where  $\alpha_W \approx 1.35$ . This means that, except for devices with  $L = 120$  nm, no sizeable short channel effects can be detected in the considered operating region.

In nanoscale technologies, the  $\alpha_f$  coefficient, which determines the slope of the low-frequency portion of the noise spectrum, deviates from the typical value of  $\alpha_f=1$ . The same trend has been observed also in the 110-nm CMOS technology investigated in this paper. The analysis of the experimental results shows that the slope of the  $1/f$  noise component of the spectrum  $\alpha_f$  is smaller than 1 in nMOSFETs and close to 1 in pMOSFETs. From the measured noise voltage spectra, it has been found that the  $1/f$  noise parameter  $\alpha_f$  does not exhibit any clear dependence on the channel geometry (length  $L$  and width  $W$ ) nor on the drain current  $I_D$ . Measured values of  $\alpha_f$  obtained for devices of both polarities are reported in Table III. Since flicker noise is strongly dependent on process and technology variations, it is worth to compare coefficients

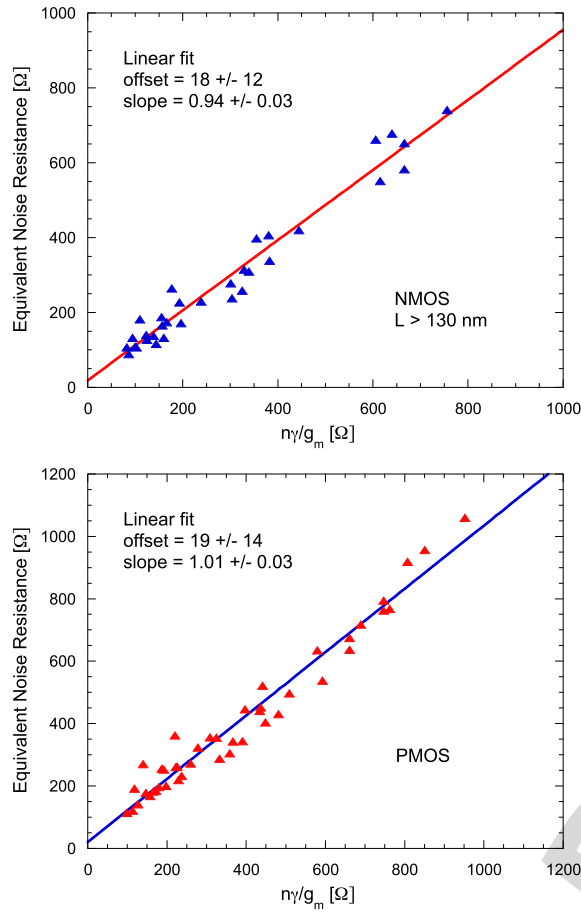


Fig. 7. Equivalent noise resistance  $R_{eq}$  extracted for nMOS (top) and pMOS (bottom) devices with various geometries, as a function of  $n\gamma/g_m$ .

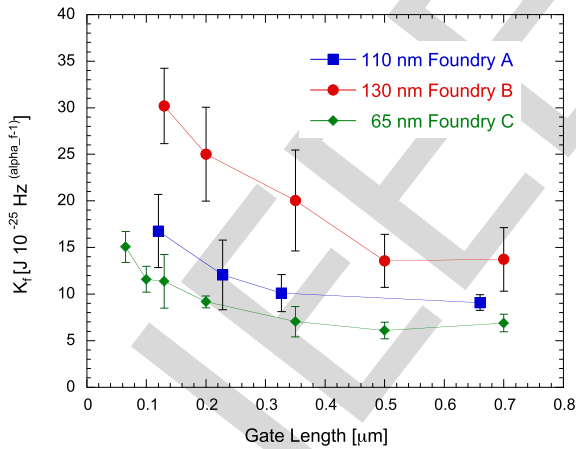


Fig. 8.  $1/f$  noise coefficient  $K_f$  as a function of the gate length  $L$  for nMOS devices.

obtained for devices belonging to different technologies nodes. To this purpose, in the same table, data coming from the two other technology nodes have been reported [20]. It is worth noting that the deviation from the nominal  $\alpha_f = 1$  value is less pronounced in the 65- and 110-nm nodes, more markedly so for the p-channel polarity. Moreover, these two technologies provide almost the same results. In Fig. 8, the behavior of the  $1/f$  noise coefficient  $K_f$  for nMOS devices is reported

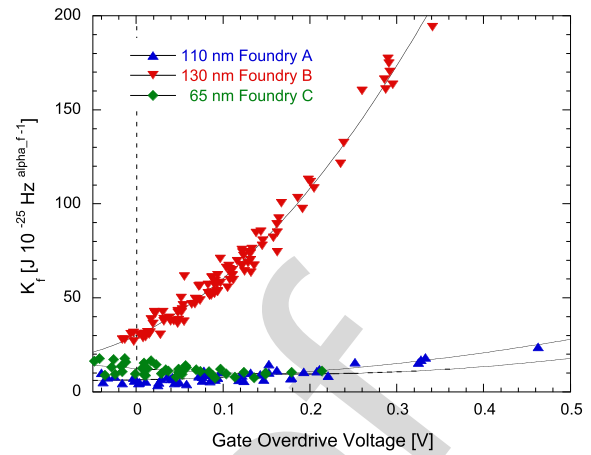


Fig. 9.  $1/f$  noise coefficient  $K_f$  as a function of the overdrive voltage  $V_{ov}$  for pMOS devices.

as a function of the channel length  $L$ . For each  $L$ , the mean value of  $K_f$  is plotted together with the spread across samples with a different gate width  $W$  and tested in different bias conditions.  $K_f$  values have been extracted from the measured noise voltage spectra by using the mean value of  $\alpha_f$  shown in Table III and the gate capacitance per unit area [25]. For comparison, purpose results coming from the 130- and 65-nm CMOS technology are also reported [25], [26]. Although the  $1/f$  noise magnitude at a given frequency is affected by the different values of  $\alpha_f$ , it can be observed that, in all technologies,  $K_f$  of the nMOS transistors is strongly dependent on the channel length, whereas it is almost independent of the device bias conditions, in agreement with the carrier number fluctuation model for the flicker noise in the channel current. Measurements on pMOS devices show a behavior which is in agreement with the mobility fluctuation model. For these devices, the  $1/f$  noise coefficient  $K_f$  shows an increase both with the drain current  $I_D$  and the channel length  $L$  (at constant  $I_D$ ) and, therefore, with the overdrive voltage  $V_{ov}$  which is defined as the difference between the gate-to-source ( $V_{GS}$ ) and the threshold ( $V_{TH}$ ) voltages. This bias dependence of flicker noise coefficient for pMOS devices is highlighted in Fig. 9 (bottom) where values of  $K_f$  obtained for pMOS devices are reported as a function of  $V_{ov}$ . It is interesting to observe that, along with  $\alpha_f$ , also  $K_f$  coefficients exhibit very similar results in the 65- and 110-nm technology.

As a last remark, it is worth to compare the performance of nMOS with respect to pMOS transistors. To this purpose, Fig. 10 compares the noise voltage spectra of both polarities for devices with  $W/L=90/0.336$  biased at a drain current of 500 μA. Since both devices are biased close to the strong inversion region, the nMOS transistor has a slightly better performance in the high-frequency portion of the spectra where the white noise component is dominant. Instead, it is interesting to observe that, as far as the low-frequency noise is concerned, devices exhibit almost the same performance. This result is in contrast with what was observed in less scaled processes where the use of n+ polysilicon gates results in a buried channel operation for pMOS devices, which keeps carrier further from the interface of Si with SiO<sub>2</sub> and likely

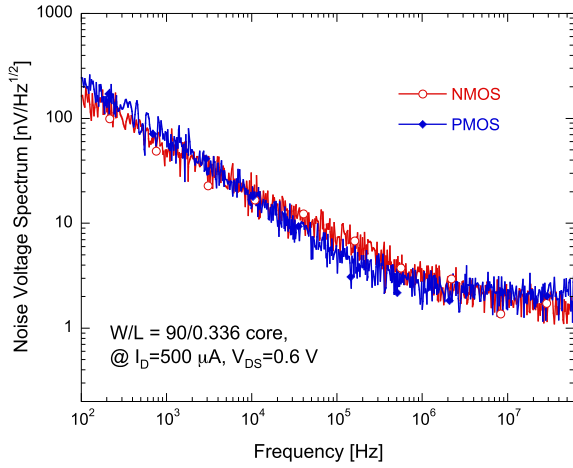


Fig. 10. Noise voltage spectra of nMOS and pMOS with the same gate geometry and drain current belonging to the 110-nm CMOS technology node.

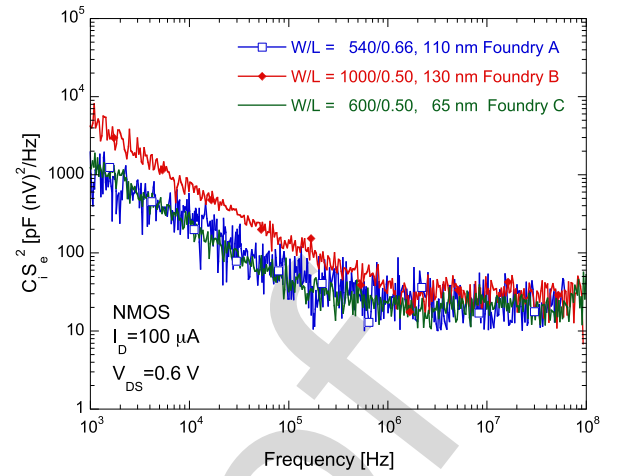


Fig. 11. Normalized spectral power density for nMOS devices belonging to three different technology nodes.

lowers the flicker noise with respect to nMOS. Although process details of the investigated 110-nm technology are not known, the comparable levels of nMOS and pMOS flicker noise can be explained with the use of p+ polysilicon gates for pMOS devices as already observed in other smaller geometry processes, such as the 65 nm [27].

#### D. Effects of Noise in Charge Measurements

As the last step, we compare the noise performance of the investigated 110-nm CMOS technology in a charge measuring system with respect to other technology nodes. In such systems, the gate width  $W$  of the charge amplifier input device is scaled to match the detector capacitance. Since the spectral densities  $S_W$  and  $S_{1/f}$  described in the previous section depend on the gate width of the device, they cannot be considered intrinsic noise parameters and cannot be used to compare the performance of different technology nodes. The comparison can be expressed in terms of the normalized spectral density which is a  $W$ -independent parameter and is expressed as

$$C_i S_e^2(f) = S_W^2 C_i + \frac{K_f}{f^{\alpha_f}} \quad (8)$$

provided that  $S_W^2$  is mostly governed by the channel thermal noise and scaling in  $W$  is done at constant current density [28].  $C_i$  is the input capacitance of the front-end device. In Fig. 11, the normalized spectral density is shown for nMOS devices belonging to the investigated 110-nm CMOS process together with the two other technology nodes. To avoid possible excess white and  $1/f$  noise, the devices have a gate length larger than the minimum allowed by the technology. The comparison is provided at almost the same inversion level with devices biased in weak inversion; as a result, the processes exhibit very similar properties at higher frequencies, where thermal noise is dominant. Therefore, we can conclude that no significant improvement or degradation is expected by moving from a technology node to another, at least in the 65–130-nm range examined in this paper. On the other hand, at low frequency, the contribution of the  $1/f$  noise appears to be larger for the device in the 130-nm technology. This is in agreement with

the larger value of both the slope and the  $K_f$  coefficients shown in Table III and Fig. 8, which results in an enhancement of the  $1/f$  noise term. It is worth pointing out that instead 65 and 110 nm exhibit almost the same behavior also in the low portion of the spectra thus leading to very similar performance for these two nodes.

#### IV. CONCLUSION

In this paper, the static and noise characterization of transistors belonging to a 110-nm CMOS process has been presented. The analysis of the noise parameters shows that, as observed in other fabrication processes, the behavior of the white noise term is consistent with equations valid in weak inversion and except for nMOS devices with minimum feature size, no sizeable short channel effects can be detected in the considered operating region. As already observed on previous CMOS generations,  $1/f$  noise is dependent on the fabrication technology and for low-noise design, it is required to keep it under control by an accurate experimental characterization. In particular, it is worth to point out that the  $\alpha_f$  and  $K_f$  noise coefficients exhibit very similar results observed in the 65-nm technology, and nMOS and pMOS devices exhibit almost the same performance in low-frequency portion of the spectrum. Measurements shown in this paper, together with the promising results obtained after preliminary studies of ionizing radiation effects, make this CMOS technology, together with the more scaled but also more expansive 65-nm node, a valuable candidate for the development of next generation, front-end systems for the readout of X-ray detectors. Moreover, in order to complete the evaluation of this technology, the characterization of ionizing radiation effects on devices up to hundreds of Mrad is planned.

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