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Characterization and verification of the Shunt-LDO regulator and its protection circuits for serial powering of the ATLAS and CMS pixel detectors

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Characterization and verification of the Shunt-LDO regulator and its protection circuits for serial powering of the ATLAS and CMS pixel detectors

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Abstract. The Shunt-LDO regulator has been integrated in the ATLAS and the CMS pixel detector RD53 front-end chip to implement the serial powering scheme which both experiments have chosen as the baseline option for the HL-LHC upgrade. The performance of the integrated regulators has been characterized and specific design challenges have been identified which are related to layout parasitics and shallow trench isolation (STI) stress effects. In addition the functionality of circuits which address crucial system level aspects like the protection against overvoltage/overload has been verified.



1. Introduction

A current based serial powering distribution is the only feasible option for the supply of the CMS and ATLAS HL-LHC pixel detectors, to maintain an acceptable material budget and power cable losses. By connecting the pixel modules in a serial chain the total supply current is defined by the maximum load current of a single module which is a significant advantage compared to the conventional parallel configuration where the supply current rises with increasing numbers of modules. Voltage regulators are integrated in the front end chips which provide a constant supply voltage from a constant input current.

2. ShuntLDO Regulator

The Shunt-LDO Regulator [1] shown in figure 1 combines the functionality of a Low-Drop Out (LDO) linear voltage regulator and a shunt regulator. The LDO generates a constant output voltage for the digital and analog components and is formed by amplifier A1, pass device M1, and the voltage divider formed by R1 and R2. The shunt transistor M4 provides an additional current path to ground or to the next module of the chain and it is controlled to drain all current which is not drawn by the load. In comparison to a conventional shunt regulator, the input voltage would be saturated in the steady-state condition. The advantage of the Shunt-LDO is that the input voltage increases continuously. This ensures a uniform current distribution to parallel regulators for a stable redundant operation. The regulators input impedance is defined by the division of resistance R3 and the current mirror factor k.

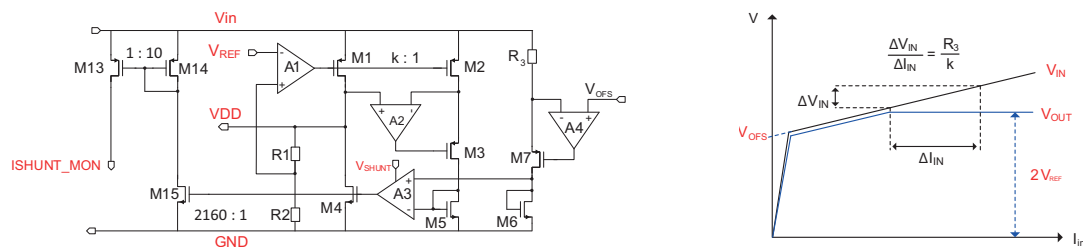


Figure 1. Simplified schematic of the Shunt-LDO (left). Characteristic IV curve for input and output (right).

3. Input impedance variations

Measurements of previous prototypes and RD53A demonstrators showed that the input impedance of the regulator was higher than expected. It could be observed that the current mirror ratio of pass-device M1 to sense-transistor M2 deviates from the ideal value. For the ideal case the mirroring factor between M1 and M2 should be 1000. But on the left side of figure 2 it is shown that the mirror ratio factor deviates from the ideal value and is a function of the gate-source voltages applied to the transistors in the current mirror configuration. It was observed that in the relevant region of the source gate voltage the mirror ratio drops down to a value of 677.

In the original layout the sensing transistor M2 was located at the edge of pass device M1 shown in figure 3. Parasitic effects especially IR drops on the supply metallization lead to different source gate voltages for both transistors which in turn lead also to different current flows. By placing the sensing transistor in the middle of the pass device (figure 4) and by optimizing the top level metallization the current mirror factor could be improved. For the relevant source gate voltage range, the current mirror is always above 938 and therefore very close to the ideal value (figure 2). The improved layout was implemented in RD53B chips and the improvements were effective.

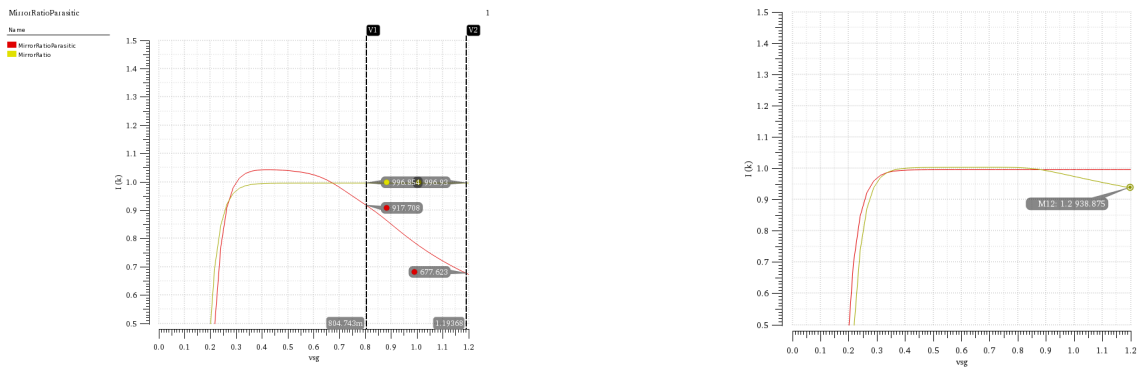


Figure 2. Mirror factor variations due to parasitics vs. ideal case (left). Improved mirror factor vs. ideal case (right).

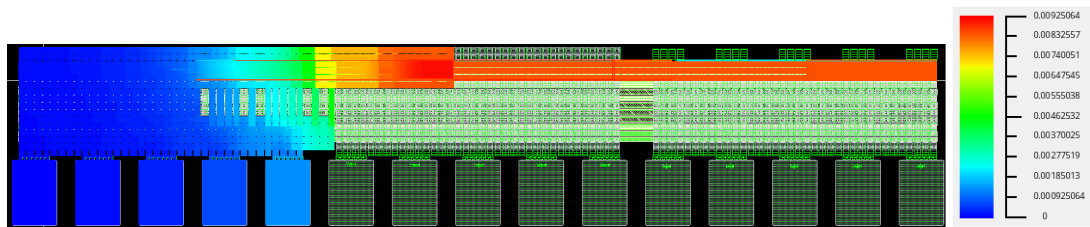


Figure 3. IR drop of pass device given in millivolt.

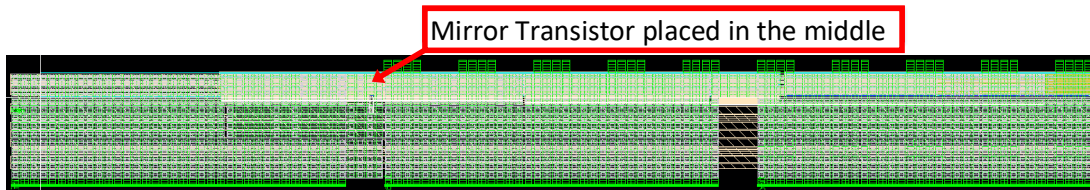


Figure 4. Improved layout of pass transistor M1 where the sense finger transistor is placed in the middle.

4. Variations in monitored shunt current

The circuitry of the ShuntLDO regulator gives the opportunity to check the shunt current in order to verify that the shunt current distributes evenly across the parallel connected regulators for redundant operation. A fraction of the current flow through shunt device M4 can be sensed via the current mirror structure built with the transistors M13, M14 and M15 (figure 1). Measurements of the RD53B-ATLAS (ITkPixV1) chip have shown that the sensed current deviates greatly from the expected current of the shunt device M4 and in addition the current mirror factor depends on the operating point. A deviation of the current mirroring factor from the ideal value could be confirmed by simulations considering parasitic layout effects (see figure 5).

It was observed that the deviation in the current mirror factor was caused by Shallow Trench Isolation (STI) stress effects. The original layout indicates that an outer finger of shunt device M4 was used for current sensing. As shown in figure 6 on the left the outer finger transistors have a different threshold voltage than the other finger transistors, which results in the deviation of the current mirror factor from the expected value.

The STI stress effects and therefore the mismatch of the shunt current and the sensed current

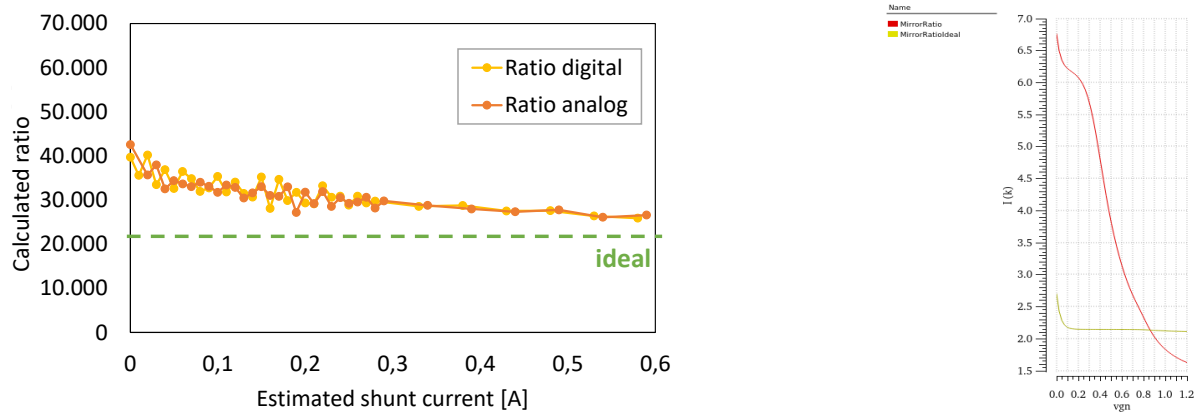


Figure 5. Measured deviations of the current mirror ratio (left). Mirror ratio comparison (simulation result) (right).

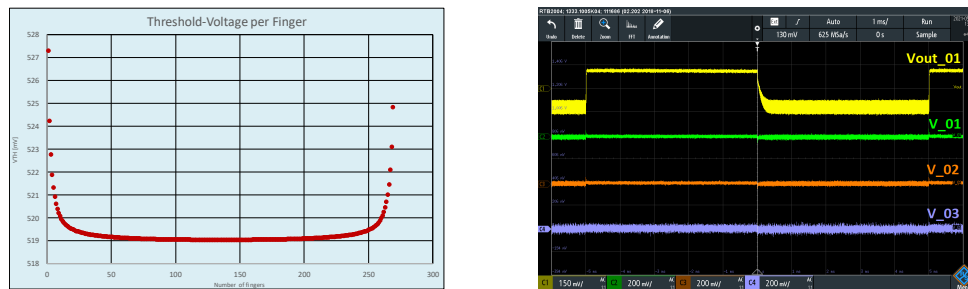


Figure 6. Threshold voltage per finger for shunt device (left) USCP activates in an overload scenario (right).

could be drastically reduced by adding sufficient dummy transistors and by placing the sense fingers in the middle of the power shunt transistor so that the relevant fingers have almost identical parameters. The improvement was implemented in the RD53B-CMS chip recently submitted for fabrication.

5. Under Shunt Current Protection

Measurements showed that the input voltage of a module drops during overload situations which leads to overvoltages in the other modules of a serial chain. This has been addressed in RD53B chips by integrating an overload protection circuit which is detected as an under shunt current scenario [2]. If the current through the shunt transistor M4 gets very low, it indicates that the load is drawing a current that is too high. In the event of an overload, the output voltage is reduced by lowering the reference voltage which in turn reduces the current consumption. This ensures that the input voltage remains stable and the module voltage does not collapse.

For a test setup several regulators were connected in a serial chain and from one regulator a high load current was drawn, which activated the overload protection circuit. Figure 6 on the right shows that the output voltage is decreased during the overload scenario but the input voltages (V_01 and V_02) of the regulators in the series chain remain constant and independent of the overload case.

6. Overvoltage Protection for serial chain

The overvoltage protection (OVP) was designed as a conventional shunt regulator and protects the ShuntLDO regulator against overvoltages greater than 2V [2]. The ShuntLDO is connected in parallel to the OVP and as soon as the input voltage exceeds the limit of 2V the shunt device of the OVP drains all excess current.

Two different test setups were considered to prove the functionality of the OVP circuit. For the first setup a single regulator was supplied with a fast current step. The supply current was increased significantly so that the regulator clearly exceeds the 2V limit in the absence of the protection circuit. Due to the OVP the input voltage is limited to 2.08V (see figure 7 left). The settling time until the regulator voltage goes back to 2V takes about 200 μ s, because of the large RC time constant.

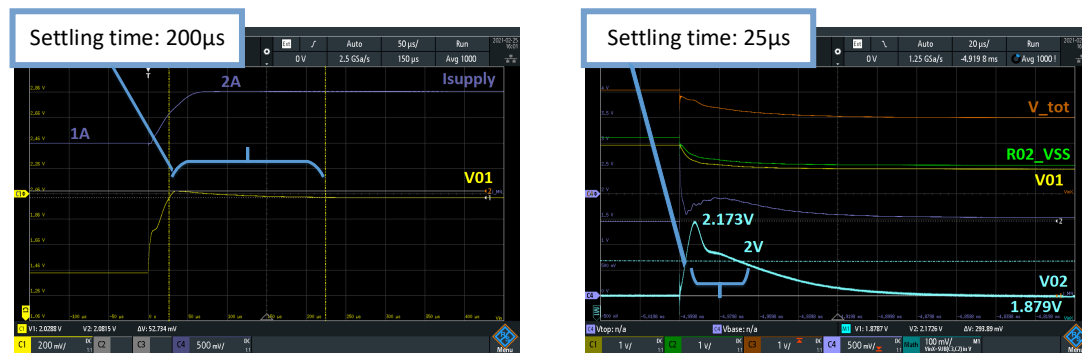


Figure 7. Single Regulator: settling time limited by large RC time (left). Serial chain: OVP limits overvoltage (right).

The second test configuration was built with two regulators connected in series. Measurements in the past have shown that a voltage collapse of one regulator leads to overvoltages in the remaining regulators. An additional circuit makes it possible to recreate the situation and to collapse one of the two regulators. As can be seen in figure 6 right the remaining modules see a voltage peak of 2.17V but thanks to the OVP the voltage settles fast back to 2V.

7. Conclusion

The measured deviations of the ShuntLDO regulators input impedance as well as variations of the monitored shunt current have been determined and improved. It became apparent that STI-Effects and layout parasitic effects were the causes of the deviations. By an adjustment of the layout both observations could be substantially improved. Furthermore, the functionality of the security features which protect the regulator against overload and overvoltage scenarios were also verified for single regulators and for regulators connected in a serial chain.

8. References

- [1] Dimitrevska A, Karagounis M, et. al. 2020 RD53A: A large-scale prototype chip for the phase II upgrade in the serially powered HL-LHC pixel detectors, *Nucl. Instr. and Meth. A* (2020)
- [2] Kampkötter J, Karagounis M, et. al. Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades, *Proceedings of TWEPP* (2019)