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Full Length Article

Design and characterization of a 28 nm CMOS charge sensitive amplifier for harsh radiation environments

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ABSTRACT

This paper discusses the design and the characterization of a charge sensitive amplifier (CSA) for the readout of hybrid pixels detectors in harsh radiation environments. The CSA, designed in a 28 nm CMOS technology, includes a feedback network for detector leakage compensation and requires around 4 μA for standard operation at a nominal voltage of 0.9 V. Test results show that the CSA is fully functional in the presence of a detector emulating leakage current up to 10 nA. The measured equivalent noise charge is close to 70 electrons r.m.s. for a sensor emulating capacitance of 50 fF, in the default bias settings. The Time-over-Threshold (ToT) performance of the CSA has also been investigated, with a maximum integral non-linearity of 3.8% detected in the ToT characteristic. The paper also reports the main performance parameters of the CSA exposed to X-rays, for total ionizing doses up to 1 Grad(SiO_2).

1. Introduction

Charge sensitive amplifiers are key components in the design of front-end channels for the readout of pixellated sensors in high energy physics (HEP) and advanced X-ray imaging applications. They represent the very front-end core of the analog processor, as their input is directly connected to the detector, releasing a given amount of charge upon particle interaction within the sensing volume [1]. Charge sensitive amplifiers (CSAs), also referred to as preamplifiers, can be used both for hybrid and monolithic active pixel sensors [2,3]. In the first topology, the detector lies in a depleted substrate, separated from the one hosting the readout electronics. For this kind of detectors, and for a sensor thickness close to 100 μm (e.g. the one foreseen for the sensors to be adopted in the phase-II upgrades of the main experiments at the Large Hadron Collider (LHC) [4,5]), the delivered charge for a minimum ionizing particle is of the order of thousands of electrons. The detector is connected to the CSA input by means of bump bonding techniques, which may have an impact on the parasitic capacitance shunting the preamplifier input. On the other hand, in monolithic active pixels, the sensor shares the substrate with the readout electronics, and the collecting electrode is routed to the CSA input with the metals available in the standard metal stack. While providing the basic charge-to-voltage conversion of the signal delivered by the sensor, the charge sensitive amplifier plays a crucial role in determining the overall performance of the front-end system. The noise properties of the readout electronics are indeed mainly dictated by the noise performance of the CSA itself, ultimately affecting the minimum stable threshold at which the front-end can be operated and, therefore, its sensitivity. Moreover, the overall power consumption of the analog front-end channel is mostly contributed by the preamplifier stage. In particular for HEP applications, minimizing the current consumption in the CSA while keeping the noise at acceptable levels, is of paramount importance to relax the constraints of the cooling systems and to keep the material budget at a minimum.

The current state-of-the-art hybrid pixel readout chips for HEP applications are being developed by the RD53 collaboration [6], hosted by CERN, and specifically targeting the upcoming phase-II upgrades of the CMS and ATLAS detectors at the LHC. Fabricated in a 65 nm CMOS process, the RD53 ASICs feature an equivalent noise charge below 100 electrons, with a moderate noise increase when the detector is bump-bonded to the readout chip [7]. The RD53 readout circuits feature a power density around 0.4 W/cm^2, and are expected to cope with a total ionizing dose (TID) of 1 Grad (SiO_2), roughly corresponding to a decade of operation in the LHC environment.

While being a mature technology for consumer electronics, the 28 nm process has been just recently adopted by the HEP designers' community for future developments. A number of IP (intellectual property) blocks are being devised by different research groups, as shown in [8,9], together with readout electronic circuits that can be

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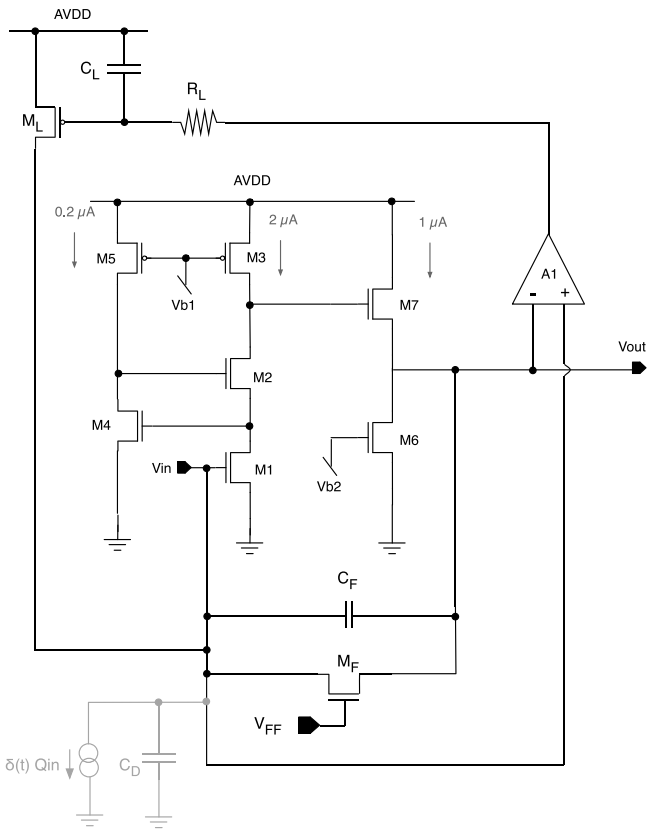

Fig. 1. Schematic diagram of the developed charge sensitive amplifier.

potentially included in post phase-II upgrades of the LHC experiments. Different studies, mainly focused on the performance of single transistors fabricated in the 28 nm process, show very promising results in terms of radiation hardness [10–12]. Nonetheless, for the best of authors' knowledge, the radiation tolerance of analog front-end circuits in 28 nm CMOS, to be integrated in a pixel cell area comparable to or smaller than the one of RD53 chips (2500 μm^2), has still to be demonstrated.

This paper discusses the design of a charge sensitive amplifier in a 28 nm CMOS process, and presents the first results from the test of a small prototype chip including, amongst other structures, a standalone CSA, which has been exposed to a TID up to 1 Grad(SiO_2) of X-rays.

2. The charge sensitive amplifier

The schematic diagram of the developed charge sensitive amplifier is shown in Fig. 1. It includes a gain stage based on a regulated cascode structure, featuring transistors $M1$–$M5$, and a source follower implemented by means of $M6$ and $M7$. The regulated cascode architecture provides a moderate DC open loop gain (close to 57 dB from simulations) in a rather compact structure (around 22 μm^2), which is a key feature in designing front-end channels for fine pitch pixel sensors. The preamplifier includes two independent feedback loops: the first one, featuring the capacitor C_F (around 4.5 fF) and the transistor M_F (whose source terminal is connected to the CSA input), is intended for charge signal processing, whereas a second, slow loop, including M_L and the amplifier A_1, is exploited to compensate for the detector leakage current. Low frequency operation of this second loop is ensured by the presence of the large capacitance C_L (around 450 fF), connected to the gate of the M_L transistor, and by the resistor R_L, implemented by means of an NMOS transistor with the gate and source terminals tied together. In the presence of a detector leakage current, the CSA output voltage, V_{out}, tends to rise, unbalancing the A1 input terminals and forcing the output of the operational amplifier to decrease. This, in turn, increases the drain current of the transistor M_L, which ultimately compensates for the detector leakage. In Fig. 1, the signal from the detector is modeled as a current source providing a current $Q_{in}\delta(t)$, where Q_{in} is the charge collected by the sensor and $\delta(t)$ is the Dirac Delta function. The detector capacitance is modeled by means of the C_D capacitor. The actual value of such a capacitance depends on the type of sensor connected to the preamplifier and on its geometry (a typical value for planar pixels sensors to be used in the Phase-II upgrades of CMS and ATLAS experiments is 50 fF). Upon signal arrival, the feedback capacitor, C_F, is discharged through M_F, which acts as a current source (controlled by the voltage V_{FF} and providing a constant current I_F in the nanoAmp range) when the input charge is large enough to push M_F in the saturation region. In particular, at room temperature this happens when the preamplifier peak amplitude is larger than around 52 mV (two times the thermal voltage), which corresponds to an input charge around 2000 electrons (considering, as shown in the following Section, a charge sensitivity of 23 mV/ke^-). In this case, the output signal of the CSA can be modeled by means of the following equation [13]:

$$V_{out}(t) = \frac{Q_{in}}{C_F}\left(1 - e^{-t/\tau_r}\right) - \frac{I_F}{C_F}t, \tag{1}$$

where

$$\tau_r = \frac{\tau_p}{A_0}\frac{C_D + C_F}{C_F}. \tag{2}$$

In (2), A_0 is the DC gain of the preamplifier forward gain stage, which can be modeled by means of a dominant-pole approximation with time constant τ_p. For $t > t_e$ the preamplifier output signal returns to the baseline, t_e being such that

$$\frac{Q_{in}}{C_F}\left(1 - e^{-t_e/\tau_r}\right) - \frac{I_F}{C_F}t_e = 0. \tag{3}$$

On the other hand, the small signal response of the CSA is ruled by the following [13]:

$$V_{out}(t) = U(t)\frac{Q_{in}}{C_F}\left(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}\right), \tag{4}$$

where U(t) is the Heaviside step function and

$$\tau_f = \frac{C_F}{g_{ds_F}}, \tag{5}$$

g_{ds_F} being the drain-to-source conductance of transistor M_F.

The described structure has been integrated in a prototype ASIC (2 mm × 1 mm, also including additional test structures), shown in Fig. 2, fabricated in a 28 nm process and including a CSA (featuring a size of 10 × 25 μm^2, fully compatible with the integration into pixel readout channels to be used in future experiments like the ones that will take place at the HL-LHC) equipped with auxiliary circuits (shown in Fig. 3) meant to emulate the presence of the detector capacitance and leakage current. In the actual implementation of the chip, three different capacitance values can be emulated (namely 0, 50 and 75 fF) by connecting two different Metal-oxide-Metal (MoM) capacitors to the preamplifier input through CMOS switches. Leakage currents up to 10 nA can be generated by means of an NMOS transistor, shunting the CSA input and providing a DC current when properly biased. In the prototype ASIC, the output of the CSA is sent to a two-stages source follower driving a PAD wire-bonded to a carrier board. Such a board is hosted by a mother board, including biasing circuits for the CSA and an additional buffer stage for the preamplifier output, which is then detected by means of a digital scope.

3. Test results

The main analog performance parameters of the charge sensitive amplifier described in the previous section have been evaluated before and after exposure to X-rays from a Seifert RP149 machine, for a total ionizing dose up to 1 Grad(SiO_2). The results from the characterization of the prototype chip are discussed in the following two subsections.

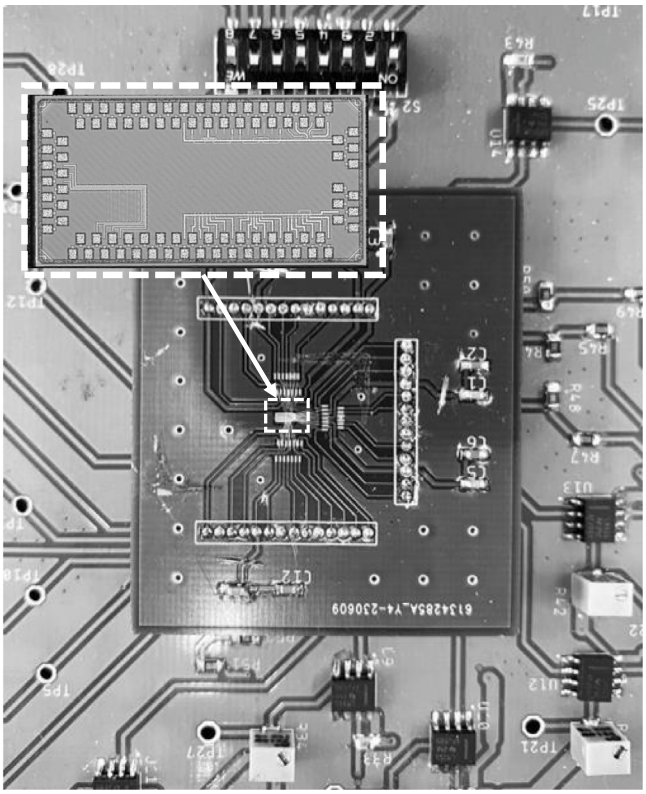

Fig. 2. The prototype chip wire bonded to the carrier board.

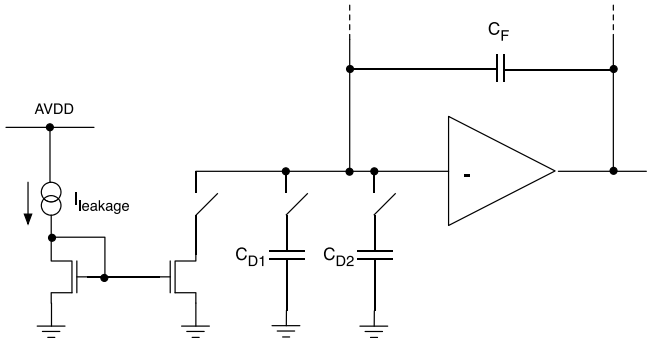

Fig. 3. Auxiliary circuits connected to the CSA input: two detector emulating capacitors (C_{D1} = 25 fF and C_{D2} = 50 fF) and leakage current generator, enabled through standard CMOS switches.

3.1. Results before irradiation

The preamplifier output signal in response to an input charge ranging from 640 to 13 440 electrons is shown in Fig. 4, for a V_{FF} of 600 mV and a detector emulating capacitance of 50 fF. The test charge is fed to the preamplifier input by means of a voltage step signal, provided by a waveform generator, across an injection capacitor (with a nominal value of 5.5 fF), not shown in Fig. 1. In the following, the voltage-to-charge conversion of the input signal is based on the nominal value of the injection capacitance, as no direct measurements have been carried out to precisely determine the actual value of such a capacitance. In Fig. 4, it is possible to notice that the preamplifier peak amplitude increases almost linearly with the injected charge up to around 8000 electrons. On the other hand, for larger input charges, the CSA tends to saturate to a peak value slightly exceeding 200 mV. According to (1), and provided that the M_F transistor is operated in the saturation region

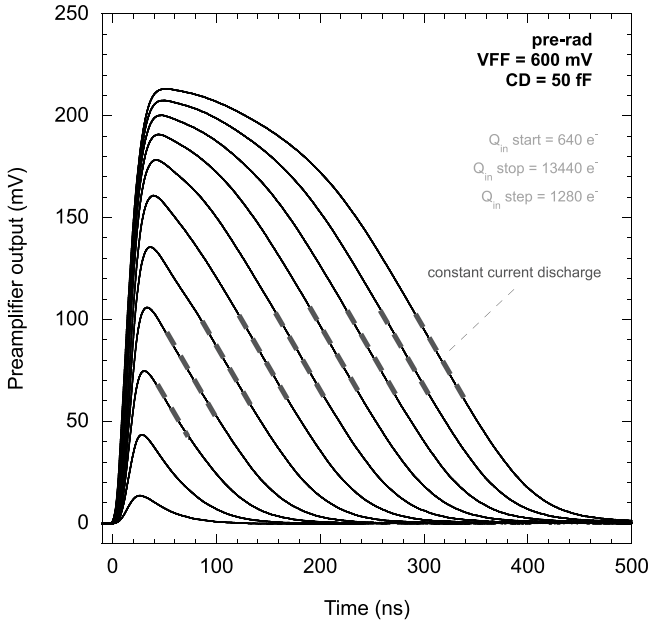

Fig. 4. Measured preamplifier output signal for an input charge ranging from 640 to 13 440 electrons.

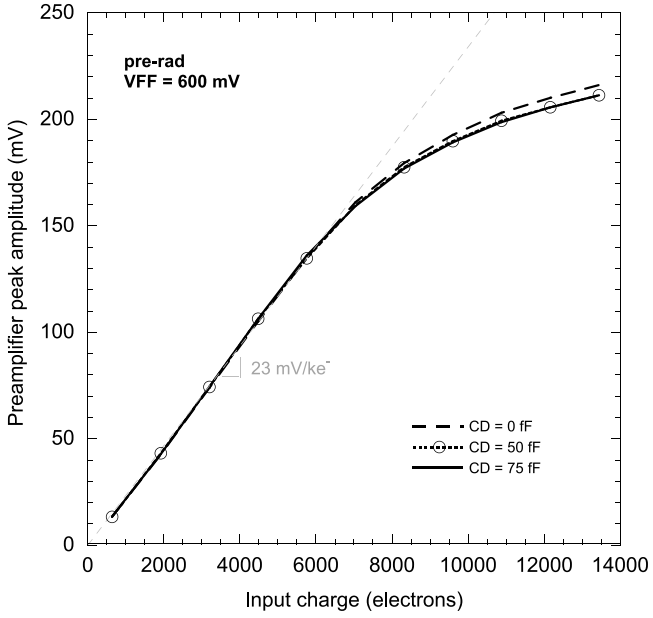

Fig. 5. Measured preamplifier peak amplitude as a function of the input charge.

and that the CSA is not saturated, for large input signals the return to the baseline features a slope ideally equal to $-I_F/C_F$. For small input signals the output of the preamplifier forces the M_F transistor to operate in the triode region, and the discharge of the feedback capacitance is slower that the one taking place at larger Q_{in} values. The peak amplitude of the preamplifier response as a function of the injected charge is shown in Fig. 5, for three different configurations of the emulating detector capacitance. The value of such a capacitance does not significantly affect the input–output characteristic of the CSA, while the saturation effect is clearly visible, as mentioned before, for an input charge approaching 8000 electrons.

The noise properties of the CSA have been assessed in terms of equivalent noise charge (ENC), defined as the input charge resulting

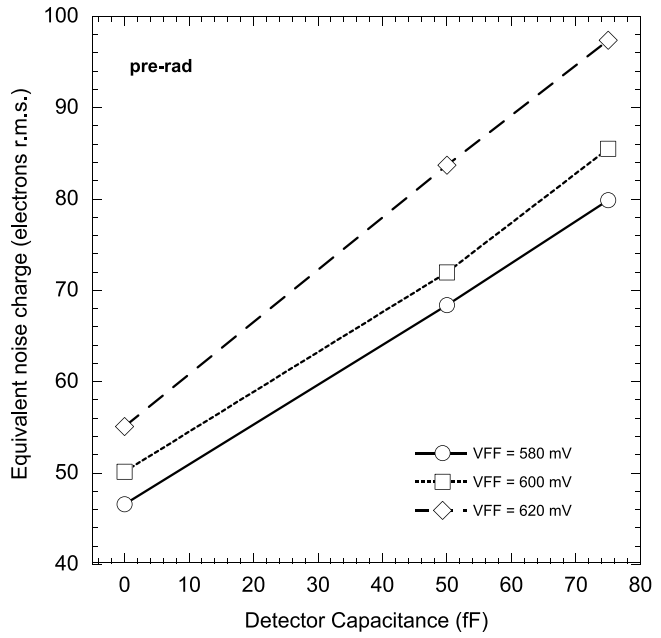

Fig. 6. Measured equivalent noise charge as a function of the detector emulating capacitance.

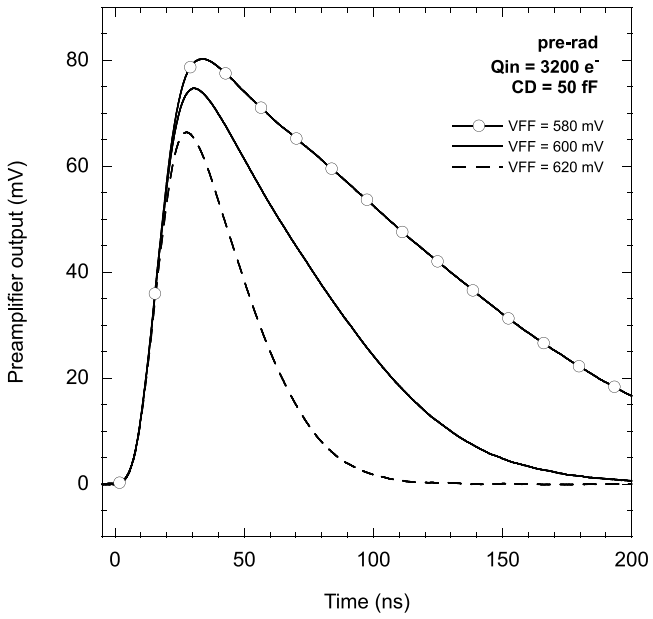

Fig. 7. Preamplifier output as a response to an input signal of 3200 electrons, for different V_{FF} values.

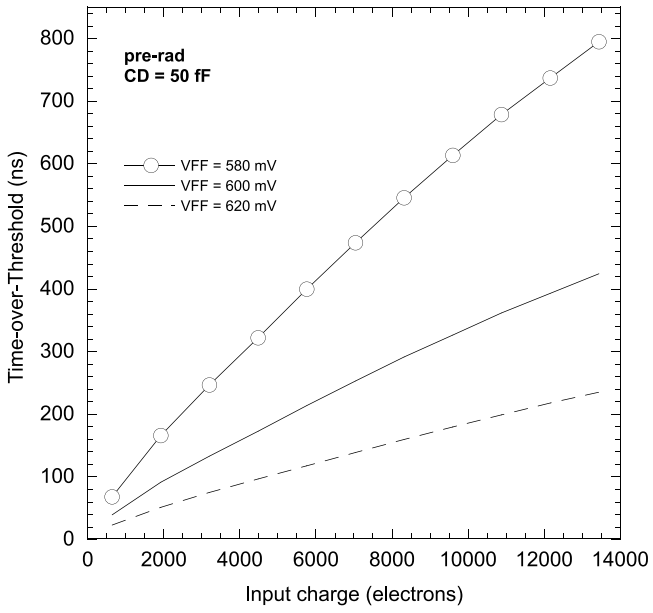

Fig. 8. Measured Time-over-Threshold (ToT) as a function of the input charge for different values of the V_{FF} voltage.

in a unity signal-to-noise ratio. According to such a definition, the ENC has been computed by means of the following equation,

$$ENC = \frac{\sqrt{\bar{v_n^2}}}{G_Q}, \tag{6}$$

with $\bar{v_n^2}$ being the mean square value of the noise detected at the CSA output by means of a digital oscilloscope. The charge sensitivity, G_Q, can be extracted by fitting the linear region of the CSA transfer characteristic of Fig. 5, and was found to be 23 mV/ke$^-$, corresponding to about 144 mV/fC, for V_{FF} = 600 mV. Fig. 6 shows the measured ENC as a function of the detector emulating capacitance, for different values of the V_{FF} voltage controlling the discharging transistor M_F. An increase in the noise is detected for larger V_{FF} values (that is for larger C_F discharge currents), which is more noticeable for the largest detector capacitance. This, on one hand, is related to an increased parallel noise contribution (associated with M_F) which, from simulations, is the main contributor to the ENC when the sensor emulating capacitor is not connected to the preamplifier input. On the other hand, for larger capacitance values, the channel thermal noise associated with the CSA input transistor becomes the dominant noise source. The equivalent noise charge contribution, ENC_{IN}, related to the channel thermal noise of M_1, can be shown to be [13]:

$$ENC_{IN}^2 = \frac{\frac{k_B T \Gamma_{IN}}{g_{m_{IN}}} \frac{A_0}{\tau_p} \frac{C_F}{C_D} (C_D + C_F)^2}{\eta}, \tag{7}$$

with k_B being the Boltzmann's constant, T the absolute temperature, $g_{m_{IN}}$ the transconductance of the CSA input transistor and Γ_{IN} its channel thermal noise coefficient. η is a coefficient ($\leq$1 in the actual implementation of the preamplifier) which depends on the CSA rising and falling time constants, τ_r and τ_f, and is found to be:

$$\eta = \left(\frac{\tau_r}{\tau_f}\right)^{2\frac{\tau_r}{\tau_f}}. \tag{8}$$

It is worth noticing that η is a monotonic decreasing function of g_{ds_F}, provided that $\tau_r \ll \tau_f$. Since g_{ds_F} increases by increasing the V_{FF} voltage, larger values of V_{FF} translate to an increased equivalent noise charge. It is also useful investigating the effect of such a voltage on the time response of the CSA, which is shown in Fig. 7 for an input charge of 3200 electrons and a detector emulating capacitance of 50 fF. As expected, a faster return to the baseline is associated with larger V_{FF} values. It is also interesting to notice that a reduced peaking time, together with a reduced peak amplitude, is achieved by increasing V_{FF}, both degrading the noise performance of the preamplifier. An equivalent noise charge close to 70 electrons r.m.s. was detected for the default bias setting (i.e. V_{FF} = 600 mV) for a detector capacitance of 50 fF, in fairly good agreement with circuit simulations.

The Time-over-Threshold characteristics has also been evaluated for the analog processor. Time-over-Threshold (ToT — namely the time interval during which the output signal of the CSA is above a given threshold level) is a technique which is widely adopted in pixel readout

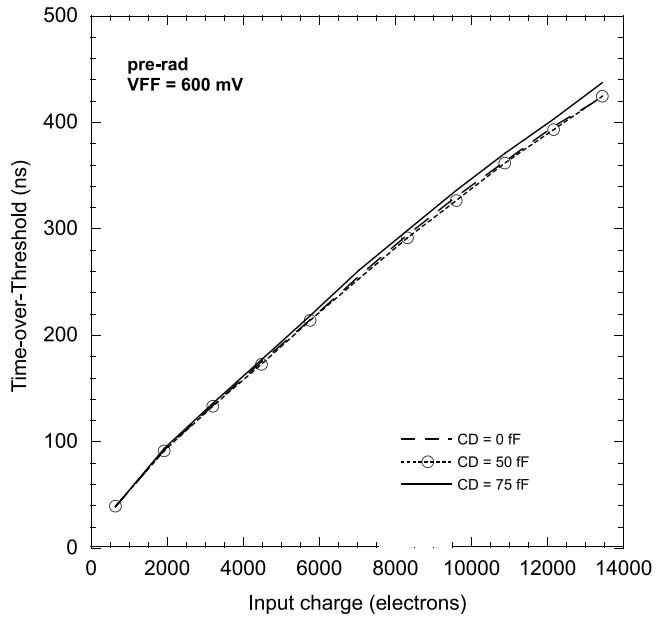

Fig. 9. Measured Time-over-Threshold (ToT) as a function of the input charge for different detector emulating capacitance and V_{FF} = 600 mV.

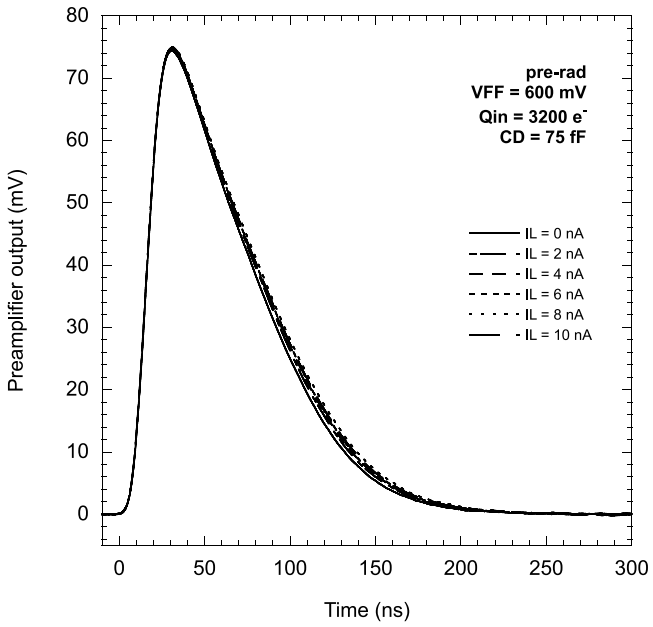

Fig. 10. Measured preamplifier output as a response to an input charge of 3200 electrons, for a detector emulating leakage current ranging from 0 to 10 nA.

circuits for high energy physics experiments, as an effective and simple way to digitize the amount of charge released by the detector. In several implementations, the ToT is found to be an almost linear function of the input charge [14,15]. While not being equipped with a threshold discriminator stage, the CSA discussed in this work has been qualified from the standpoint of ToT performance by means of a digital scope, which was used to compute the ToT with a fixed threshold equivalent to 500 electrons. The Time-over-Threshold as function of the input charge is shown in Fig. 8 for different values of the V_{FF} voltage. The integral non-linearity, evaluated for an input charge ranging between around 2000 up to 13 440 electrons, was found to be a decreasing function of V_{FF}, with a maximum value of 3.8% obtained for V_{FF} = 580 mV. As shown in Fig. 9, the detector emulating capacitance, C_D, does not significantly affect the ToT characteristic of the analog processor. The main effects of the detector leakage current on the CSA behavior are shown in Figs. 10 and 11. In particular, Fig. 10 shows the preamplifier output as a response to an input charge of 3200 electrons, in the presence of a detector emulating leakage current ranging from 0 up to 10 nA (for C_D = 75 fF), where it is possible to notice that the output waveform is basically insensitive to the leakage current: both the preamplifier peaking time and amplitude are indeed preserved, together with the pulse duration, exploited for Time-over-Threshold measurements as already explained in this section. As far as the noise performance is concerned, a slight increase in the ENC was detected for an increasing detector leakage current, as shown in Fig. 11. This is related to an additional noise contribution associated to transistor M_L, which turns on when compensating for the leakage current, and to the contribution given by the NMOS transistor generating the leakage current I_L, discussed in the previous section.

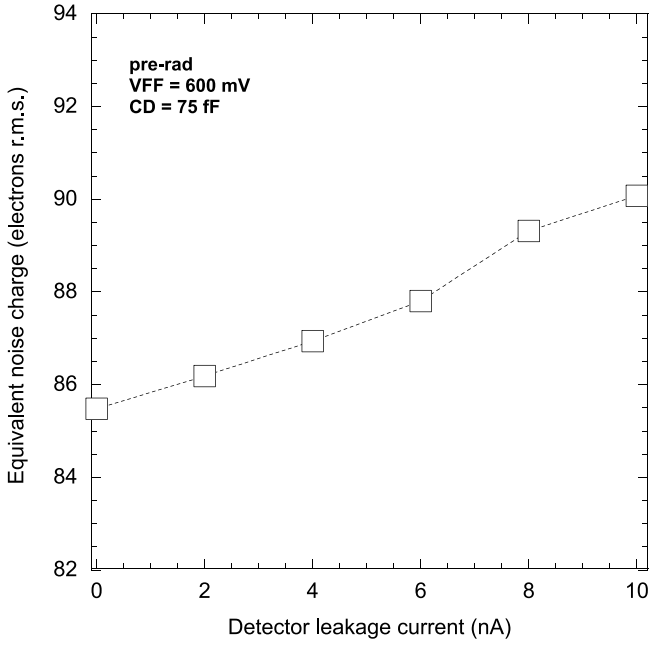

Fig. 11. Measured equivalent noise charge as a function of the detector emulating leakage current.

3.2. Results after irradiation

One sample of the prototype chip has been exposed to a TID up to 1 Grad(SiO_2) with a 10 keV X-ray source. During the irradiation, performed at room temperature with a dose rate close to 5.4 Mrad/h, the CSA has been biased with the default current settings highlighted in Fig. 1. While not being tested, the sample chip was kept at a temperature close to −18 °C. The results from the characterization of the prototype chip after irradiation are discussed in this section.

The preamplifier output in response to an input signal of 3200 electrons is shown in Fig. 12, for a detector emulating capacitance of 75 fF. The plot shows the CSA output waveform as measured before irradiation (solid black curve) with the nominal bias settings – in particular with a voltage V_{FF} set to 600 mV – together with the waveform obtained in the same nominal conditions at a TID of 1 Grad(SiO_2) (dashed black curve). The CSA output pulse duration is significantly reduced after irradiation, due to a likewise increase of the drain leakage current of the transistor M_F. The faster return to the baseline, in turn, is associated with a decreased peak amplitude of the CSA response, due

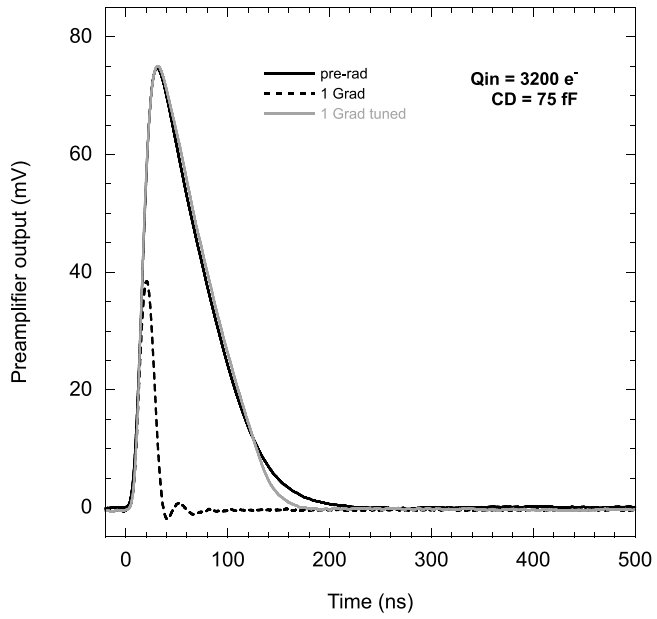

Fig. 12. Measured preamplifier output as a response to an input signal of 3200 electrons before irradiation (solid black) and after irradiation at 1 Grad (SiO_2), before (dashed black) and after (solid gray) V_{FF} tuning.

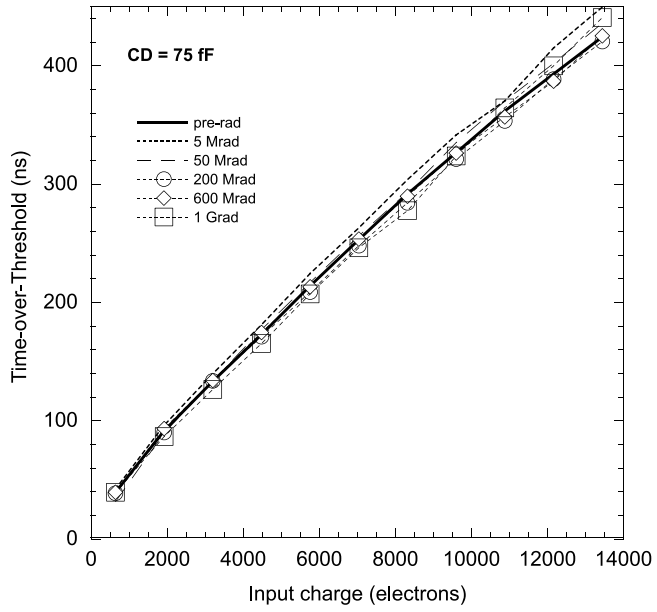

Fig. 13. Measured Time-over-Threshold as a function of the input charge for different TIDs.

to the interaction of poles associated with rise and fall time constants of the preamplifier.

To restore the ToT achieved before irradiation (around 130 ns), the V_{FF} voltage needs to be tweaked. The tuned CSA output is shown in Fig. 12 (gray solid curve), where it is possible to notice that both the pulse duration and the peak amplitude are properly restored. Fig. 13 shows the measured Time-over-Threshold as a function of the input charge after V_{FF} tuning, which was only performed for an input of 3200 electrons, for different TID steps. After tuning, no significant changes in linearity, slope or dynamic range in the ToT characteristic were detected for the irradiated device. The tuned V_{FF} value (i.e. the value for which the ToT is found to be 130 ns for an input charge of 3200 electrons) is shown in Fig. 14 as a function of the total dose.

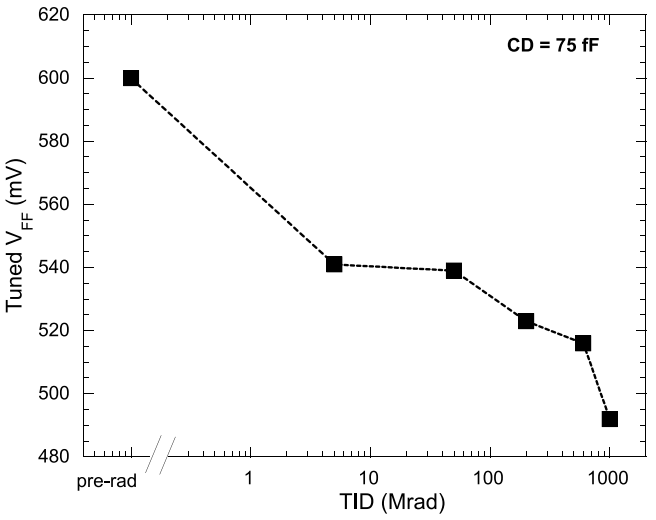

Fig. 14. Tuned value of the V_{FF} voltage as a function of the TID. The tuned value is the V_{FF} voltage needed to obtain a ToT of 130 ns for an input charge of 3200 electrons.

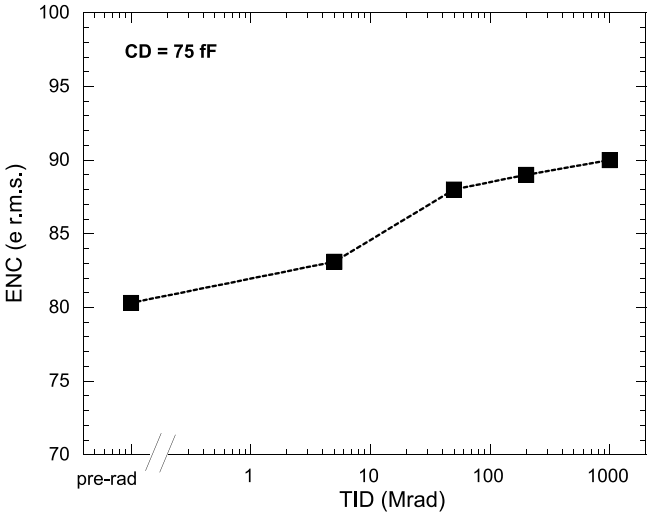

Fig. 15. Measured equivalent noise charge as a function of the TID, for a detector emulating capacitance of 75 fF.

As far as the noise performance is concerned, a moderate increase in the equivalent noise charge has been detected, as visible in Fig. 15, which shows the ENC as a function of the TID, for a detector emulating capacitance of 75 fF. The noise increase is close to 12% for a TID of 1 Grad(SiO_2), and might be only partially ascribed, according to the data reported in [16], to a marginal decrease of the transconductance of M_1, resulting in a slight increase in the input-referred channel thermal noise contribution of transistors M_1 and M_3. The results reported in [16] also show a non negligible increase in the 1/f noise. Nonetheless, the flicker noise contribution to the ENC, for both the transistors, is negligible in this design, as confirmed from circuit simulations. An additional noise contribution may also be related to the radiation-induced drain leakage current of the NMOS transistor emulating the detector leakage.

4. Conclusions

A continuous reset, charge sensitive amplifier for the readout of hybrid pixel detectors in harsh radiation environments has been designed and fabricated in a 28 nm CMOS technology. The preamplifier

consists of a forward gain stage, implemented by means of a single-ended regulated cascode amplifier, surrounded by two independent feedback loops, which are used for signal discharge and for detector leakage compensation. Test results show that the circuit can operate properly, with a marginal noise increase, for a detector leakage current up to 10 nA. The equivalent noise charge was found to be an increasing function of the detector capacitance and of the current discharging the CSA feedback capacitance, with an ENC close to 70 electrons r.m.s. for a sensor emulating capacitance of 50 fF and the CSA biased in the default configuration (i.e. 2 μA bias current for the CSA input branch and $V_{FF} = 600$ mV). Such a noise value is fully compatible with the one measured in analog front-end channels for the readout of pixel sensors for the phase-II upgrades of the CMS and ATLAS experiments at the High-Luminosity Large Hadron Collider [17]. The Time-over-Threshold performance of the CSA has been investigated by means of a digital scope, where the signal from the preamplifier has been compared with a fixed threshold level. A maximum integral non-linearity of 3.8% has been measured for the ToT characteristic. One sample of the CSA has been irradiated with X-rays for TIDs up to 1 Grad(SiO_2). The CSA is fully functional at the maximum total dose investigated in this work, with a significant change in the CSA feedback discharge current, which needs to be tuned to restore optimal operation of the preamplifier. A marginal increase in the equivalent noise charge is observed after tuning.

CRediT authorship contribution statement

L. Gaioni: Writing – review & editing, Writing – original draft, Project administration, Methodology, Formal analysis, Data curation, Conceptualization. **A. Galliani:** Writing – review & editing, Validation, Investigation, Data curation. **L. Ratti:** Writing – review & editing, Supervision. **V. Re:** Writing – review & editing, Supervision. **G. Traversi:** Writing – review & editing, Data curation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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