Recent progress of RD53 Collaboration towards next generation Pixel Read-Out Chip for HL-LHC

2016 JINST 11 C12058

(http://iopscience.iop.org/1748-0221/11/12/C12058)

Published by IOP Publishing for Sissa Medialab

Received: *October 27, 2016*
Accepted: *December 13, 2016*
Published: *December 21, 2016*

Pixel 2016 International Workshop
September 5 – September 9, 2016
Sestri Levante, Genova, Italy

Recent progress of RD53 Collaboration towards next generation Pixel Read-Out Chip for HL-LHC

The RD53 collaboration

N. Demaria,[a,1] M.B. Barbero,[b] D. Fougeron,[b] F. Gensolen,[b] S. Godiot,[b] M. Menouni,[b] P. Pangaud,[b] A. Rozanov,[b] A. Wang,[b] M. Bomben,[c] G. Calderini,[c] F. Crescioli,[c] O. Le Dortz,[c] G. Marchiori,[c] D. Dzahini,[d] F.E. Rarbi,[d] R. Gaglione,[e] L. Gonella,[f] T. Hemperek,[f] F. Huegging,[f] M. Karagounis,[f] T. Kishishita,[f] H. Krueger,[f] P. Rymaszewski,[f] N. Wermes,[f] F. Ciciriello,[g] F. Corsi,[g] C. Marzocca,[g] G. De Robertis,[h] F. Loddo,[h] F. Licciulli,[h] A. Andreazza,[i] V. Liberali,[i] S. Shojaii,[i] A. Stabile,[i] M. Bagatin,[l] D. Bisello,[l] S. Mattiazzo,[l] L. Ding,[l] S. Gerardin,[l] P. Giubilato,[l] A. Neviani,[l] A. Paccagnella,[l] D. Vogrig,[l] J. Wyss,[l] N. Bacchetta,[m] F. De Canio,[n] L. Gaioni,[n] B. Nodari,[n] M. Manghisoni,[n] V. Re,[n] G. Traversi,[n] D. Comotti,[o] L. Ratti,[o] C. Vacchi,[o] R. Beccherle,[p] R. Bellazzini,[p] G. Magazzu,[p] M. Minuti,[p] F. Morsani,[p] F. Palla,[p] S. Poulios,[p] L. Fanucci,[q] A. Rizzi,[q] S. Saponara,[q] K. Androsov,[r] G.M. Bilei,[s] M. Menichelli,[s] E. Conti,[t] S. Marconi,[t] D. Passeri,[t] P. Placidi,[t] G. Della Casa,[a] G. Mazza,[a] A. Rivetti,[a] M.D. Da Rocha Rolo,[a] E. Monteil,[v] L. Pacher,[v] D. Gajanana,[z] V. Gromov,[z] N. Hessey,[z] R. Kluit,[z] V. Zivkovic,[z] M. Havranek,[aa] Z. Janoska,[aa] M. Marcisovsky,[aa] G. Neue,[aa] L. Tomasek,[aa] V. Kafka,[ab] P. Sicho,[ab] V. Vrba,[ab] I. Vila,[ac] E. Lopez-Morillo,[ad] M.A. Aguirre,[ad] F.R. Palomo,[ad] F. Muñoz,[ad] D. Abbaneo,[ae] J. Christiansen,[ae] D. Dannheim,[ae] D. Dobos,[ae] L. Linssen,[ae] H. Pernegger,[ae] P. Valerio,[ae] N. Alipour Tehrani,[ae] S. Bell,[af] M.L. Prydderch,[af] S. Thomas,[af] D.C. Christian,[ag] F. Fahim,[ag] J. Hoff,[ag] R. Lipton,[ag] T. Liu,[ag] T. Zimmerman,[ag] M. Garcia-Sciveres,[ah] D. Gnani,[ah] A. Mekkaoui,[ah] I. Gorelov,[ai] M. Hoeferkamp,[ai] S. Seidel,[ai] K. Toms,[ai] J.N. De Witt,[aj] A. Grillo[aj] A. Paternò[ak]

[a] *INFN Torino, v.P.Giuria 1, 10125 Torino, Italy*
[b] *Aix Marseille Université, CNRS/IN2P3, CPPM UMR 7346, 13288, Marseille, France*
[c] *Laboratoire de Physique Nucléaire et de Hautes Energies (LPNHE) Paris, France*
[d] *Laboratoire de Physique Subatomique et de Cosmologie (LPSC), Grenoble, France*
[e] *Laboratoire d'Annecy-le-Vieux de Physique des Particules (LAPP), Annecy-le-Vieux, France*
[f] *Rheinische Friedrich-Wilhelms-Universität Bonn Physikalisches Institut, Bonn, Germany*

[1] Corresponding author.

doi:10.1088/1748-0221/11/12/C12058

2016 JINST 11 C12058

[g] *Politecnico di Bari, Bari, Italy*
[h] *INFN Sezione di Bari, Bari, Italy*
[i] *INFN Sezione di Milano and Università degli Studi di Milano, Milano, Italy*
[l] *INFN Sezione di Padova and Università di Padova, Padova, Italy*
[m] *INFN Sezione di Padova, Padova, Italy*
[n] *INFN Sezione di Pavia and Università di Bergamo, Bergamo, Italy*
[o] *INFN Sezione di Pavia and Università di Pavia, Pavia, Italy*
[p] *INFN Sezione di Pisa, Pisa, Italy*
[q] *INFN Sezione di Pisa and Università di Pisa, Pisa, Italy*
[r] *INFN Pisa and Università di Siena, Siena, Italy*
[s] *INFN Sezione di Perugia, Perugia, Italy*
[t] *INFN Sezione di Perugia and Department of Engineering, Università di Perugia, Italy*
[v] *INFN Sezione di Torino and University of Torino, Torino, Italy*
[z] *National Institute for Subatomic Physics (NIKHEF), Amsterdam Netherlands*
[aa] *Faculty of Nuclear Sciences and Physical Engineering of the Czech Technical University (FNSPE-CTU)*
[ab] *Institute of Physics of the Academy of Sciences of the Czech Republic (IP-ASCR)*
[ac] *Instituto de Fisica de Cantabria (IFCA, CSIC-UC), Santander, Spain*
[ad] *Electronic Engineering Dept, School of Engineering, Sevilla University, Spain*
[ae] *European Organization for Nuclear Research (CERN), Geneva, Switzerland*
[af] *Science and Technology Facilities Council, Rutherford Appleton Laboratory, Chilton, Didcot, United Kingdom*
[ag] *Fermi National Accelerator Laboratory (FNAL) Batavia, U.S.A.*
[ah] *Lawrence Berkeley National Laboratory (LBNL), Berkeley, U.S.A.*
[ai] *University of New Mexico (UNM), Albuquerque, U.S.A.*
[aj] *University of California Santa Cruz (UCSC), Santa Cruz, U.S.A.*
[ak] *INFN Sezione di Torino and Politecnico di Torino, Torino, Italy*

E-mail: demaria@to.infn.it

Abstract: This paper is a review of recent progress of RD53 Collaboration. Results obtained on the study of the radiation effects on 65 nm CMOS have matured enough to define first strategies to adopt in the design of analog and digital circuits. Critical building blocks and analog very front end chains have been designed, tested before and after 5–800 Mrad. Small prototypes of 64×64 pixels with complex digital architectures have been produced, and point to address the main issues of dealing with extremely high pixel rates, while operating at very small in-time thresholds in the analog front end. The collaboration is now proceeding at full speed towards the design of a large scale prototype, called RD53A, in 65 nm CMOS technology.

Keywords: Front-end electronics for detector readout; Particle tracking detectors (Solid-state detectors); Radiation-hard electronics; VLSI circuits

2016 JINST 11 C12058

Contents

2016 JINST 11 C12058

1 Introduction

The CERN laboratory has approved in 2016 the High Luminosity LHC project, HL-LHC, that will allow the detailed exploration of the TeV scale up to nearly 10 TeV. HL-LHC will increase substantially the rate of pp collision in order to reach 3000 fb^{-1} integrated luminosity in a decade period: precision measurement in the Higgs sector, searches of new particle at high masses and studies of rare B-decays will be possible.

Several experimental challenges have to be addressed in order to have fully performant experiments at HL-LHC, and therefore CMS and ATLAS have started since few years vigorous upgrades programs. In particular the particle fluxes, radiation dose and data bandwidth become more and more important when moving closer to the interaction point and the pixel detectors have to work in extreme conditions that require a vigorous R&D program both for electronics and sensors.

The CERN RD53 collaboration [1–4] was constituted in 2013 with the purpose to develop pixel readout Integrated Circuits (IC) for the next generation of pixel readout chips to be used for the ATLAS and CMS Phase 2 pixel detector upgrades and future CLIC pixel detectors. The IC challenges include: smaller pixels to resolve tracks in boosted jets, very high hit rates due to unprecedented particle fluence, much higher output bandwidth, radiation and large IC format with low power consumption in order to instrument large areas while keeping the material budget low. Nineteen institutes from nine countries, for a total of about 120 members are part of RD53, with almost equal contributions from CMS and ATLAS experiments.

This paper describes the main achievements of RD53 and in particular the steps towards a large scale prototype (about 2 cm^2), called RD53A readout chip(ROC). The main choices of the collaboration can be seen in the specification of RD53A, details can be found in [5] but the main ones are described in table 1. The maximum pixel rate has been derived from full simulation of ATLAS and CMS pixel detectors, assuming an inner layer at around 3 cm radius and a pile-up of 200. The ROC has been considered to be connected to a silicon detector with characteristics taken from the current R&D, in term of thickness (100–150 μm), pixel aspect ratio, capacitance and leakage current.

2 Analog Very Front End electronics and IP-blocks

Four different analog very front-ends (VFE) (CSA,[1] discriminator, signal processing) have been developed [6, 7]. All designs are: compact with area below $35 \times 35\, mu\mathrm{m}^2$; low-noise with ENC below 100 electrons for a value of input capacitance of 50 fF typical for a silicon sensor; low power; fast, allowing correct time-stamp with 25 ns accuracy. Three designs use 4-bit Time Over Threshold technique (ToT) for signal digitisation, while one using a flash-ADC per pixel is limited to 3-bit in order to limit power consumption. All VFE are capable to provide to each pixel 10 nA leakage current to a silicon sensor. The main characteristics of the VFE are listed in table 2. A total of

Table 1. Summary of RD53A main specifications.

SPECIFICATION	VALUE
Pixel cell	$50 \times 50\ \mu\mathrm{m}^2$
leakage current	< 10 nA per Pixel
Pixel hit rate	3 GHz/cm^2
Dead Time loss	< 1 %
Trigger rate / latency	1 MHz/12.5 μs
Low In-time Threshold	< 1200 e$^-$
Total Ionizing Dose (TID)	500 Mrad
Hit charge resolution	≥ 4-bit
Total power per pixel	< 9–10 μW

Table 2. Analog Very Front End designs of RD53.

	VFE Characteristics
1	CSA with continuous current feedback DC-coupled pre-comparator stage Threshold trimming with two 4-bit DAC 4-bit ToT at 40 MHz
2	CSA with Krummenacher feedback current comparator Threshold trimming with 4-bit DAC 4-bit ToT at 40 MHz
3	CSA with Krummenacher feedback AC-coupled synchronous comparator Auto-zeroing every 100 μs 4-8 bit with Fast ToT at 40–500 MHz
4	CSA with leakage current feedback Synchronous comparator Auto-zeroing every 25 ns 3-bit flash ADC

Table 3. List of Building blocks.

BLOCK	Characteristics
Band-Gap	a) DTNMOS design b) Bipolar design c) NMOS design
DAC	a) 10-bit current steering b) 12-bit voltage
ADC for Bias monitoring	a) 12-bit SAR ADC 100 kSample/s b) 12-bit Wilkinson ADC 5 kSample/s
Temp sensor	based on BJT, MOS
Analog Buffer	
PLL-CDR	PLL and clock data recovery
SER	a) serialiser 1–3 Gbits/s b) serialiser 5 Gbits/s
DES	deserialiser 2 Gbits/s
Cable Driver	programmable emphasis
sLVS-Tx	1–2 GBits/s SLVS-400 mV
sLVS-Rx	1–2 Gbits/s SLVS-400 mV
Memory cells	a) DICE Latch b) DICE SRAM
Power On reset	
Shunt LDO	needed to allow serial powering

15–20 building blocks [8–11] have been identified of interest for future pixel chips and have been developed by RD53 institutes and are listed in table 3.

3 Small demonstrators and RD53A prototype

Two small size demonstrators, consisting of a matrix of 64×64 pixels of dimension $50 \times 50\ \mu\mathrm{m}^2$ have been designed as intermediate step before moving to the design of a large scale prototype, and

[1]Charge Sensitive Amplifier

Table 4. Small Demonstrator and RD53A main differences.

Characteristics	FE65P2	CHIPIX65-FE0	RD53A
Pixel Matrix	64×64	64×64	400×192
Matrix Organization	(2×2) analog islands Pixel Regions (4×64) CORES	(2×2) analog islands Pixel Regions (4×4) CORES	(2×2) analog islands Pixel Regions (8×8) CORES
Pixel Regions	(2×2) pixels distributed data buffer trigger matching	(4×4) pixels centralized data buffer trigger matching	(2×2) or (4×4) pixels tbd trigger matching
VFE	VFE-1	VFE-2 VFE-3	VFE-1, VFE-2 VFE-3, VFE-4
Analog-Digital Isolation	Analog triple well Digital triple well	Analog triple well	Analog triple well Digital triple well
Signal Digitisation	4-bits	binary or 5-bits	4 or 8 bits
. Building Blocks	few not RD53	. BandGap, DAC, ADC SER, sLVS-Tx/Rx	BandGap, DAC, ADC Ana-Buffer, PON-reset, Shunt-LDO sLVS-Tx/Rx, Cable Driver, PLL-CDR, Temp Sensor
Bias-Distribution	DAC, current mirror for all pixels (Single stage mirroring)	DAC, current mirror for column bias-cells (Double stage mirroring)	DAC, current mirror for double-column bias-cells (Double stage mirroring)
Radiation hard design	Analog	Analog	Analog and Digital
Powering	Standard	Standard	Serial-Powering

point to address in a complementary way: low noise, low in-time threshold ($1000\,e^-$) performance; integration of different analog front end chains and of several building blocks; a complex digital architecture with high efficiency at the extreme pixel rate of 3 GHz/cm^2 foreseen in the inner layer of HL-LHC pixel detectors. Main characteristics of the demonstrators are shown in table 4. together with a comparison to RD53A. The pixel matrix digital architecture is distributed in single pixel regions providing hit local storage: only data relative to events trigger by the experiment are sent to the chip periphery (trigger matching). Additional sharing of digital circuitry comes with the adoption of digital cores that include several pixel regions. In order to allow this sharing, both in the horizontal and in the vertical direction, the VFE's have been organized into analog islands of (2×2) pixels.

The FE65-P2 demonstrator has been produced in the end of 2015. It is an evolution of the FEI4 chip, with a strong contribution from the institutes that designed it. The higher granularity is achieved thanks to the use of the CMOS 65 nm: the digital architecture in the pixel matrix is in particular strongly based on the (2×2) pixel regional architecture and the distributed latency buffers. Particular care has been taken to separate analog and the digital circuitry, placing them in separate triple wells isolated from the silicon substrate, to prevent pick-up from spoiling the analog noise performance. The triple well separation has been extended also to the chip pads. Early results have been obtained with bare chip and after the bump-bonding with planar silicon sensors. Preliminary measurements results on bare and bump-bonded devices show $40\,e^-$ ENC and $800\,e^-$ minimum threshold.

The CHIPIX65-FE0 demonstrator [12] has recently arrived from production in September 2016 and therefore has integrated several building blocks of the collaboration. The design has been developed independently from FE65P2, with different design team and exploring other solutions to

2016 JINST 11 C12058

solve similar challenges: only analog circuitry has been placed in triple well, while the digital is directly on the substrate; the concept of pixel region has been extended to (4×4) pixel, in order to share digital circuitry to a larger number of pixels, and to do so the local data storage is centralized. The CHIPIX65-FE0 integrates several RD53 building blocks and other two VFEs. This has allowed the development of the bias distribution of the whole chip together with a monitoring scheme of all current and voltage needed to the VFE, that has been eventually adopted and extended to RD53A. Early results show that the CHIPIX65-FE0 works correctly and the bare devices show 85 e^- ENC and 500 e^- minimum threshold.

The design of a large prototype of about 2 cm^2 and 400×192 pixels (columns and rows), called RD53A, is progressing well, with the effort of a focused team of about ten designers working together, merging the FE65-P2 and the CHIPIX65-FE0 design team plus additional designers. The floor-planning of the chip has been defined identifying several blocks with the chip periphery subdivided in the Analog-Chip-Bottom (ACB), the Digital-Chip-Bottom (DCB) and the I/O-frame.

The pixel matrix will consist of a matrix of (8×8) pixels cores and will be subdivided into the four VFE designs: their integration in RD53A is well advanced, since three designs have already been working in the demonstrators. The area reserved for the digital architecture in the pixel region is rather full, due to the long trigger latency and the high particle flux. Moreover requiring a more radiation hard design implies increasing the total area, as it forces to use larger than minimum size transistors and also larger buffers to preserve fast transitions and good timing. Solutions are under study and are evaluated for the two different architectures that have been used in the demonstrators.

In the periphery, the ACB includes all the biasing blocks and the monitoring, plus additional building blocks like the CDR/PLL generating the high frequency clock and recovering the data for the chip, the Power-on-Reset (POR) and the temperature sensors. The DCB, shown in figure 1, includes a Ch-Synch that generates the 40 MHz clock, synchronizes all the data input and sends it to the Command Decoder (CMD) to broadcast in-time commands and configuration data to the chip. Alternatively a JTAG can be used for the configuration of the chip. The pixel matrix data go to the Data Builder, then to an output FIFO and are encoded using an Aurora64/66 algorithm [13]. The data will be serialised either with four outputs at 1,28 Gbits/s or with a unique 5 Gbits/s and then sent to the I/O.

A fundamental feature of RD53A is the implementation of serial powering: for this reason the chip includes two Shunt-LDOs [14], one dedicated to analog and the other to digital power, providing stable voltage to the chip while requiring a constant current and a constant output voltage. A maximum power consumption is defined and variations from it are absorbed by the shunt resistor. It is important to analyse the variation in time of current consumption, specially for the digital circuitry, that is strongly dependent on the particle flux and has a clocked activity. For this reason a sophisticated simulation and verification environment [15] of the digital architecture has been used.

4 Radiation effects

The degradation of the performance of 65 nm MOSFETs upon radiation exposure was investigated, using 10-keV X-rays as in previous studies but also using 3-MeV protons. X-rays provide a good way to compare old with new data, even though very long exposure times are needed to reach TID levels up to 1 Grad: a review of the results can be found in [16]. The results show significant degradation above 100 Mrad, particularly in core minimum size pMOSFETs. In order to obtain

2016 JINST 11 C12058

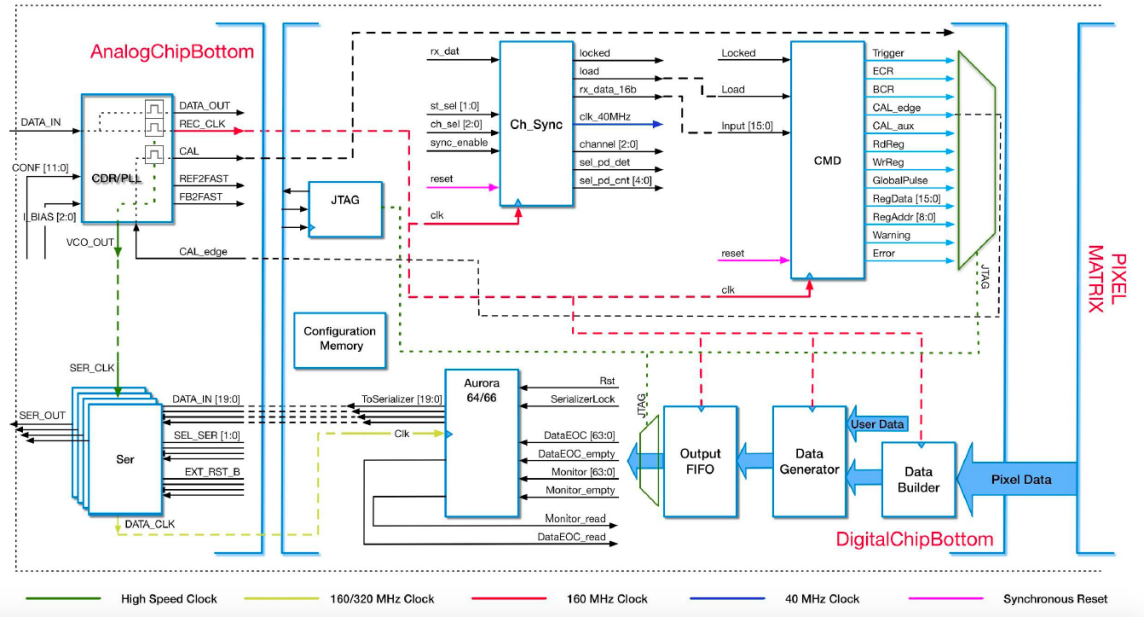

Figure 1. Digital-Chip-Bottom block scheme with connections to ACB and to the Pixel Matrix.

increased radiation hard tolerance, minimum size MOS have to be avoided. Models that parametrize the effect of TID on MOS performance have been defined according to the measurements made, in particular for 200 and 500 Mrad.

In the design of analog circuitry and of building blocks, the use of very small MOS has been avoided: in case of need a set of custom digital cells has been designed. All crucial building blocks and very front end analog chains needed for RD53A production have been designed and sent for production: most of those have been successfully tested before and after 5–800 Mrad total dose. In particular an irradiation up to 6-800 Mrad for VFE-2 and VFE-3 showed a slight decrease (below 5%) in the gain of the pre-amplificaiton stage, an increase of 10–20% in the noise and a higher peak time, but without a substantial compromise of the performance.

A chip has been designed to study the effect of TID on several different types of standard cell libraries provided by the foundry (Digital-RAD, DRAD chip). In particular ring oscillators have been designed in different flavors, so to measure how much the digital transitions are slowed down by irradiation. The intention is to evaluate how the radiation models describe correctly the degradation of performance, so that the digital design can be implemented with more robust cells. The modification of digital standard cells, with larger dimension where needed, is also an on-going activity of RD53. Early results show for 200 Mrad an average increase of 5–15% in gate delay or speed reduction, depending on the dimension of the cell.

5 Conclusions

The pixel detectors for the future upgrade of HL-LHC require a new generation readout chip (ROC), to provide higher granularities and extraordinary performance in term of noise, speed, data storage and readout, including to survive to unprecedented levels of radiation fluence and dose.

2016 JINST 11 C12058

The RD53 collaboration is a common effort of experts from ATLAS and CMS communities focused on the deliverable of a large scale prototype of a pixel chip satisfying the main specification of the CMS and ATLAS experiments for the HL-LHC. Building blocks, VFE, and small demonstrators showed very promising results. The important deliverable of RD53A, with an area of about 2 cm^2, is progressing very well and is planned for spring of year 2017. RD53A will be fully characterized as bare chip, after the bump-bonding to different silicon detectors defined by the sensor R&D and after irradiation.

References

[1] RD53 web site, http://rd53.web.cern.ch/rd53/.

[2] J. Christiansen and M. Garcia-Sciveres, *RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation*, CERN-LHCC-2013-008.

[3] N. Demaria et al., *RD53 Collaboration and CHIPIX65 Project for the development of an innovative Pixel Front End Chip for HL-LHC*, PoS(IFD2014)010.

[4] RD53 collaboration, P. Valerio, *65 nm Technology for HEP: Status and Perspective*, PoS(Vertex2014)043.

[5] RD53 collaboration, M. Garcia-Sciveres, *RD53A Integrated Circuit Specifications*, CERN-RD53-PUB-15-001.

[6] L. Pacher, E. Monteil, A. Rivetti, N. Demaria and M. Da Rocha Rolo, *A low-power low-noise synchronous pixel front-end chain in 65 nm CMOS technology with local fast ToT encoding and autozeroing for extreme rate and radiation at HL-LHC*, in proceedings of *IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, 2015, pp. 1–4.

[7] L. Ratti, F. De Canio, L. Gaioni, M. Manghisoni, V. Re and G. Traversi, *An asynchronous front-end channel for pixel detectors at the HL-LHC experiment upgrades* in proceedings of *IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, 2015, pp. 1–5.

[8] G. Traversi, F. De Canio, L. Gaioni, M. Manghisoni, S. Mattiazzo, L. Ratti et al., *Characterization of bandgap reference circuits designed for high energy physics applications*, *Nucl. Instrum. Meth.* **A 824** (2016) 371.

[9] G.D. Robertis, F. Loddo, S. Mattiazzo, L. Pacher, D. Pantano and C. Tamma, *Design of a 10-bit segmented current-steering digital-to-analog converter in CMOS 65 nm technology for the bias of new generation readout chips in high radiation environment*, 2016 *JINST* **11** C01027.

[10] J. Shojaii, A. Stabile and V. Liberali, *A radiation hardened static RAM for high-energy physics experiments* in proceedings of *29th IEEE International conference on Microelectronics Electronics (MIEL 2014)*, Belgrade, 2014, pp. 359–362

[11] N. Demaria et al., *CHIPIX65: Developments on a new generation pixel readout ASIC in CMOS 65 nm for HEP experiments*, in proceedings of *6th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Gallipoli, 2015, pp. 49–54.

[12] E. Monteil et al., *A prototype of a New Generation Readout ASIC in 65 nm CMOS for Pixel Detector at HL-LHC*, in proceedings of *Pixel 2016 International Workshop*, Sestri Levante, Genova, Italy, September 5 – September 9 2016.

[13] https://www.xilinx.com/products/intellectual-property/aurora64b66b.html.

2016 JINST 11 C12058

[14] M. Karagounis, D. Arutinov, M. Barbero, F. Huegging, H. Krueger and N. Wermes, *An integrated Shunt-LDO regulator for serial powered systems*, in *Proceedings of ESSCIRC '09*, Athens, 2009, pp. 276–279.

[15] E. Conti, S. Marconi, J. Christiansen, P. Placidi and T. Hemperek, *Simulation of digital pixel readout chip architectures with the RD53 SystemVerilog-UVM verification environment using Monte Carlo physics data*, 2016 *JINST* **11** C01069.

[16] M. Menouni, M. Barbero, F. Bompard, S. Bonacini, D. Fougeron, R. Gaglione et al., *1-Grad total dose evaluation of 65 nm CMOS technology for the HL-LHC upgrades*, 2015 *JINST* **10** C05009.

2016 JINST 11 C12058