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Article

Design of the ANTARES4 Readout ASIC for the Second Flight of the GAPS Experiment: Motivations and Requirements

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Abstract

The General AntiParticle Spectrometer is a balloon-borne experiment designed to search for low-energy cosmic-ray antinuclei as a potential indirect signature of dark matter. Over the course of at least three long-duration flights over Antarctica, it will explore the sub-250 MeV/ n energy range with sensitivity to antideuterons and antihelium, while also extending antiproton measurements below 100 MeV. The instrument features a tracker built from more than one thousand lithium-drifted silicon detectors, each read out by a dedicated custom integrated circuit. With the first flight scheduled for the austral summer of 2025, a new prototype chip, ANTARES4, has been developed using a commercial 65 nm complementary metal-oxide semiconductor process for use in the second flight. It integrates eight independent analog channels, each incorporating a low-noise charge-sensitive amplifier with dynamic signal compression, a CR–RC shaping stage with eight selectable peaking times, and on-chip calibration circuitry. The charge-sensitive amplifier uses metal-oxide semiconductor feedback elements with voltage-dependent capacitance to support the wide input energy range from 10 keV to 100 MeV. Four alternative feedback implementations are included to compare performance and design trade-offs. Leakage current compensation up to 200 nA per detector strip is provided by a Krummenacher current–feedback network. This paper presents the design and architecture of ANTARES4, highlighting the motivations, design drivers, and performance requirements that guided its development.

Keywords: GAPS experiment; spectrometer; Si(Li) strip detectors; readout ASIC; charge-sensitive amplifier (CSA); dynamic signal compression; Krummenacher feedback; 65 nm CMOS technology; balloon-borne cosmic-ray detection; antideuteron and antihelium search



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1. The GAPS Instrument

The General AntiParticle Spectrometer (GAPS) is a NASA, INFN, ASI, and JAXA funded balloon-borne experiment designed to search for low-energy cosmic-ray antiparticles as an indirect signature of dark matter [1]. Cosmological measurements indicate that non-baryonic dark matter constitutes about 27% of the total energy density of the universe, whereas baryons contribute only 5% [2]. Among indirect probes, low-energy antinuclei, particularly antideuterons, and antihelium are especially compelling because the expected astrophysical background below 250 MeV/ n is strongly suppressed, enhancing the potential for discovery of new physics [3–6].

GAPS targets this low-background regime using a detection technique based on the formation and decay of exotic atoms in lithium-drifted silicon (Si(Li)) detectors. Incoming antiparticles are slowed and captured into atomic orbits, emit characteristic X-ray de-excitation lines, and then annihilate to produce charged secondaries that generate a distinctive event topology [7,8]. This approach complements magnetic-spectrometer experiments such as AMS-02 on the International Space Station and balloon missions like BESS while extending sensitivity to the lowest kinetic energies for antideuterons and improving coverage for antiprotons [9–13].

Figure 1 provides an overview of the GAPS instrument. The payload consists of a large-area time-of-flight (ToF) system surrounding a modular Si(Li) tracker, operated at about $-40\text{ }^{\circ}\text{C}$ using an oscillating heat-pipe (OHP) cooling system coupled to a radiator for passive thermal control [14–16]. The ToF subsystem, composed of the Cube, Umbrella, and Cortina panels, provides timing information and generates the trigger for the internal Si(Li) tracker [17], while the tracker performs simultaneous X-ray spectroscopy and charged particle tracking. The electronics bay, radiator, and solar panels are also visible, highlighting the integration of the main subsystems within the payload.

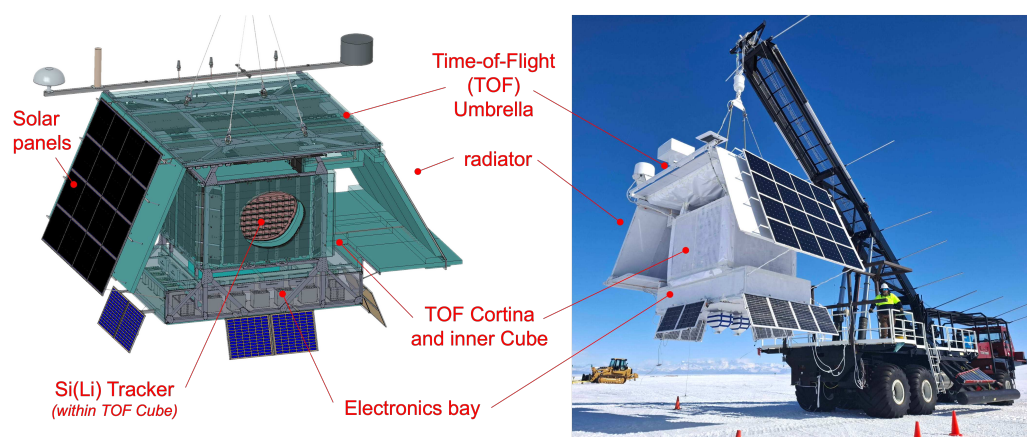


Figure 1. Schematic overview and photograph of the GAPS instrument. **(Left):** Rendering of the science payload highlighting the main subsystems, including the Si(Li) tracker enclosed within the ToF Cube, the ToF Umbrella and Cortina panels, the radiator, the electronics bay, and the solar panels. **(Right):** The flight-ready GAPS instrument integrated at the NASA Long Duration Balloon (LDB) facility at McMurdo Station, Antarctica, during the commissioning campaign.

The readout of the silicon-strip tracker requires low-noise, low-power front-end electronics with dynamic-range coverage from 10 keV to 100 MeV. For the first flight, the readout was based on SLIDER32 (32-channels Si-LI DEtector Readout), an ASIC implemented in a 180 nm CMOS process, which enabled full-system integration and calibration [18–20]. For the second flight, development has shifted to the new ANTARES4 (ANTiparticle Asic REadout for Si(Li) detectors) prototype, fabricated in a 65 nm CMOS process. ANTARES4 targets improved noise performance, extended leakage current compensation, and reduced per-channel power consumption [21].

2. Scientific Motivations and Design Drivers

The GAPS tracker comprises more than 1000 Si(Li) detectors, each segmented into eight strips, yielding approximately 8000 readout channels [22]. During flight, the detectors operate at about $-40\text{ }^{\circ}\text{C}$, maintained by the OHP-based passive cooling system. Given the high channel count, the readout architecture must satisfy a strict per-channel power budget of $\leq 10\text{ mW}$ —corresponding to a total tracker power consumption of $\sim 80\text{ W}$ —to remain compatible with the thermal design, the available battery system, and the solar array.

For the first GAPS flight, seven tracker layers are instrumented. Each layer comprises a 6×6 grid of modules, with each module housing four detectors, for a total of just over 1000 Si(Li) detectors. The remaining three layers at the bottom of the tracker are equipped with mechanical dummies that act as thermal mass and emulate the power consumption of fully populated modules. Given the high channel density of the tracker, the performance of the front-end ASIC directly impacts the overall instrument capabilities. Improvements in noise, power consumption, and dynamic range propagate across thousands of channels, influencing the tracker’s data quality as well as its thermal and power budgets.

The detection strategy simultaneously measures two distinct energy regimes: low-energy X-rays from exotic-atom de-excitation in the 10 keV to 100 keV range and high-energy charged-particle deposits up to 100 MeV. Accommodating both within a single readout chain demands an effective dynamic range exceeding four orders of magnitude while preserving keV-level resolution in the X-ray band. This requirement motivates the use of dynamic signal compression in the front-end, implemented via non-linear MOS feedback capacitors in the charge-sensitive amplifier (CSA) [23,24].

The main design targets for the front-end electronics are:

- **Input energy dynamic range:** 10 keV to 100 MeV.
- **Energy resolution:** ≤ 5 keV FWHM below 100 keV for ~ 40 pF strip capacitance.
- **Noise performance:** Equivalent Noise Charge (ENC) $\leq 480 e^-$ rms at 40 pF.
- **Power consumption:** ≤ 10 mW/channel.
- **Operating temperature:** -40 °C to -35 °C.

Detector leakage current further constrains the architecture. Under nominal flight conditions at -40 °C, Si(Li) strip leakage currents typically range from 2.5 nA to 10 nA [22]. However, during on-ground integration and calibration at higher temperatures (up to about -10 °C), it can rise to hundreds of nA per strip. To ensure operability under these conditions, the front-end must provide leakage compensation up to at least 200 nA per strip.

Tracker Module Architecture

Each tracker module (Figure 2) measures roughly 24×24 cm² and integrates four lithium-drifted silicon (Si(Li)) detectors, each segmented into eight strips, for a total of 32 channels per module. The detectors are mounted within a machined aluminum frame that provides both mechanical support and a shared ground through the guard rings.

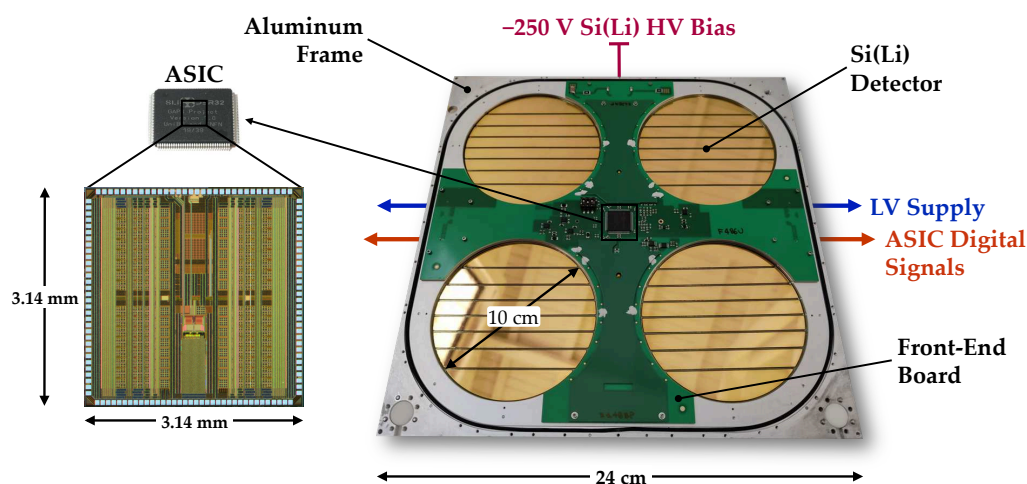


Figure 2. Layout of a GAPS tracker module [19]. Four Si(Li) detectors are mounted in an aluminum frame and connected to a central FEB hosting the 32-channel readout ASIC. The FEB provides high-voltage bias distribution, low-voltage supply and digital control, as well as detector readout via the ASIC. Thermal coupling to the OHP cooling system occurs through the aluminum frame.

A front-end board (FEB), centrally mounted on the module, hosts the SLIDER32 readout ASIC [19], fabricated in a 180 nm CMOS technology, together with passive components required for biasing, calibration injection, and signal routing. The Si(Li) strips are wire-bonded directly to the ASIC inputs. The FEB also manages low-voltage power distribution, detector biasing, and control signals within the module.

Each module is enclosed between two aluminized polypropylene windows that shield the detectors from stray light and contamination. The aluminum frame includes thermal interface ports for coupling to the OHP cooling system, which maintains the detector operating temperature between $-35\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ during flight.

Modules are assembled into vertical tracker rows, each comprising six aligned modules connected via custom flex-rigid printed circuit boards, as shown in Figure 3. These distribute low-voltage power, ASIC digital signals, and control lines along the row, while high-voltage bias is supplied through dedicated connectors on each module. At one end of each row, an additional flex interface board connects the modules to the tracker interface board, enabling data readout and communication with the dedicated flight computer. The rows are stacked to form multiple tracker planes, giving the GAPS tracker its modular architecture.

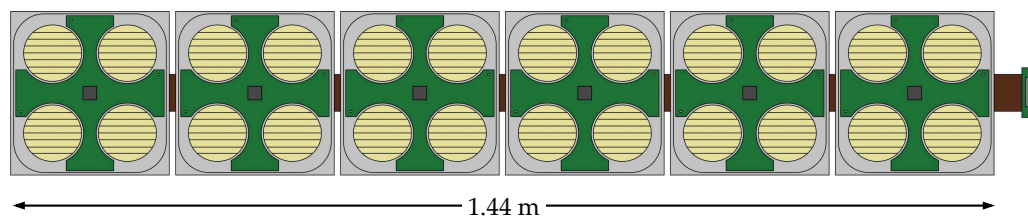


Figure 3. Schematic of a tracker row comprising six modules connected in series. Low-voltage power, ASIC digital signals, and control lines are distributed along the row via a custom flex-rigid printed circuit board. An additional flex interface board connects the module row to the interface board, enabling data readout and communication with the dedicated flight computer.

3. Front-End Requirements for the GAPS Tracker

The wide input energy range of the GAPS tracker, from low-energy X-rays in the 10 keV to 100 keV region to charged-particle deposits up to 100 MeV, requires a front-end capable of handling over four decades of dynamic range while preserving keV-level resolution in the X-ray band. To achieve this, the ANTARES4 ASIC employs a dynamic signal compression scheme implemented in the CSA stage [23,24].

The CSA gain is determined by the feedback capacitance according to $G = 1/C_f(V_{out})$, where the effective capacitance depends on the output voltage. The technique exploits an inversion-mode MOS capacitor in the feedback path, whose capacitance varies with V_{out} relative to the threshold voltage V_{th} . For small signals ($V_{out} \ll V_{th}$), the device operates in depletion, yielding a minimal feedback capacitance $C_{f,min}$ and, therefore, a high low-energy gain suitable for keV-scale X-ray resolution. For larger signals ($V_{out} > V_{th}$), the device enters strong inversion, and the capacitance increases toward $C_{f,max}$. As $C_f(V_{out})$ grows with the integrated charge, the corresponding gain decreases, preventing CSA saturation and enabling the measurement range up to 100 MeV.

This architecture provides a continuous transition between two operating regimes:

- High-gain response in the X-ray range (10 keV to 100 keV);
- Gain compression for high deposited energies, enabling measurements in the charged particle regime without saturating the front-end.

Beyond dynamic range, the design is subject to several additional constraints. Some inherited from the first-flight ASIC, while others reflect lessons learned from the extensive on-ground calibration carried out during instrument commissioning:

- **Detector capacitance:** approximately 40 pF per strip.
- **Power budget:** limited to ≤ 10 mW/channel, corresponding to less than 80 W total for the full tracker instrument with seven active layers.
- **Leakage current compensation:** during flight at -40 °C, typical leakage currents range from 2.5 nA to 10 nA per strip; during on-ground calibration at higher temperatures (up to -10 °C), the ASIC must compensate currents up to at least 200 nA to maintain operability.
- **Integration density:** one 32-channel ASIC per FEB, fully compatible with the existing module design.
- **Performance metrics:** low-energy gain $G_{le} > 250$ μ V/keV, high-energy gain $G_{he} > 2$ μ V/keV; the compression factor $k = G_{le}/G_{he}$ quantifies the transition from the high-gain X-ray regime to the compressed charged-particle regime, with $k > 80$; the kink energy, defined as the point where the linear regime transitions from low-energy X-ray detection to high-energy particle detection, is required to lie above 1.5 MeV.

4. ANTARES4 ASIC Overview

The ANTARES4 ASIC was developed as a research and development prototype using a commercial 65 nm CMOS process. Unlike SLIDER32, which provided a flight-qualified solution for the first GAPS mission, ANTARES4 is not intended for direct flight use. Instead, it serves as a platform to evaluate circuit topologies and design solutions to be integrated into the next-generation flight ASIC.

The transition from the 180 nm CMOS node of SLIDER32 to 65 nm was motivated by several factors. First, long-term availability of the 180 nm process has become uncertain, with multi-project wafer (MPW) service providers gradually discontinuing support for this technology. Second, the 65 nm node offers higher integration density, reduced silicon area per channel, and lower nominal supply voltage (1.2 V versus 1.8 V), which together enable improved power efficiency and potentially better noise performance. Finally, adopting a modern, widely supported technology mitigates obsolescence risks and ensures the long-term sustainability of the readout electronics for future GAPS flights.

The main design objectives are as follows:

- Replace approximately 360 SLIDER32 chips in the upgraded tracker while maintaining full compatibility with the existing FEBs and mechanical module layout.
- Reduce the per-channel power consumption below 10 mW to comply with the strict overall tracker power budget.
- Improve noise performance and energy resolution at a nominal detector capacitance of 40 pF, achieving a signal-to-noise ratio of approximately 15.39 dB at the lowest X-ray detection limit of 10 keV.
- Extend leakage-current compensation up to 200 nA per strip to guarantee operability during on-ground calibration at elevated temperatures.
- Implement dynamic signal compression using MOS-based feedback capacitors, enabling an input energy range from 10 keV to 100 MeV while preserving keV-level resolution for low-energy X-ray spectroscopy [23,24].

Each of the eight prototype channels integrates the following building blocks:

- A low-noise CSA with a MOS-capacitor-based feedback network implementing dynamic signal compression.

- A CR–RC semi-Gaussian shaper with eight selectable peaking times to optimize the signal-to-noise ratio.
- A calibration charge-injection circuit to emulate charge deposits and evaluate the input–output channel transcharacteristic under controlled leakage-current and temperature conditions during characterization.
- A Krummenacher feedback network providing both continuous charge restoration and leakage-current compensation.
- Dedicated test outputs giving direct access to the CSA and shaper waveforms for characterization.

Figure 4 shows a simplified block diagram of a single ANTARES4 readout channel. The detector signal is DC-coupled to the input of a CSA, which integrates the collected charge on a MOS-based feedback capacitor. This element implements dynamic signal compression by providing voltage-dependent feedback capacitance. A Krummenacher network in the feedback path ensures continuous charge restoration and leakage-current compensation.

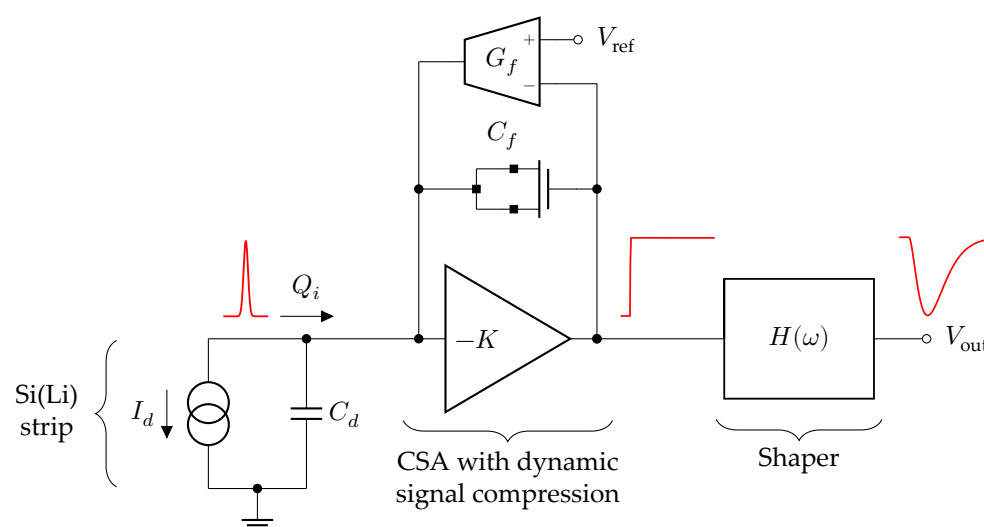


Figure 4. Simplified block diagram of a single ANTARES4 readout channel, including the CSA with MOS-based feedback capacitance C_f , the CR–RC shaper, the calibration injection circuit, and the Krummenacher leakage-current compensation with transconductance G_f . The red traces respectively indicate: detector current pulse (left), CSA output (center), and shaper output (right); the three traces are purely illustrative and not to scale.

The CSA output is then processed by a CR–RC semi-Gaussian shaper with eight selectable peaking times, allowing optimization of the signal-to-noise ratio and mitigation of pile-up at the nominal event rate. A dedicated calibration charge-injection circuit is included to emulate charge deposits and evaluate the input–output channel transcharacteristic under controlled leakage-current and temperature conditions during characterization. Additionally, test outputs at both the CSA and shaper stages provide direct access to intermediate waveforms for evaluation during ASIC characterization.

4.1. Detector Leakage Current Compensation

Although nominal leakage currents for Si(Li) strips are typically 2.5 nA to 10 nA at $-40\text{ }^\circ\text{C}$, they can exceed several hundred nA during ground calibration near $-10\text{ }^\circ\text{C}$. Since all tracker calibration and performance validation activities are carried out on the ground, ensuring channel operability under these conditions is essential. During these procedures, the OHP-based cooling system is coupled to a cold metal plate with circulating ethanol chilled at $-80\text{ }^\circ\text{C}$, but this setup cannot maintain the nominal flight temperature of $-40\text{ }^\circ\text{C}$ across the entire tracker. To address this, ANTARES4 integrates an improved Krumme-

nacher feedback network within the CSA, designed to compensate leakage currents up to at least 200 nA, maximizing the number of channels that remain operational during calibration and enabling comprehensive detector characterization prior to launch.

Figure 5 summarizes the post-layout transcharacteristic of the CSA obtained at the output of the CR–RC shaper for different detector leakage currents, ranging from $I_{\text{leak}} = 0$ nA up to 264 nA. Figure 6 reports the extracted CSA gain and the equivalent feedback capacitance, illustrating the effect of dynamic compression across decades of input charge. Both simulations were performed at -40 °C under the typical–typical (TT) process corner, with an input detector capacitance $C_d = 40$ pF, an n -type MOS feedback capacitor, and a shaping peaking time of $t_p = 0.2$ μ s.

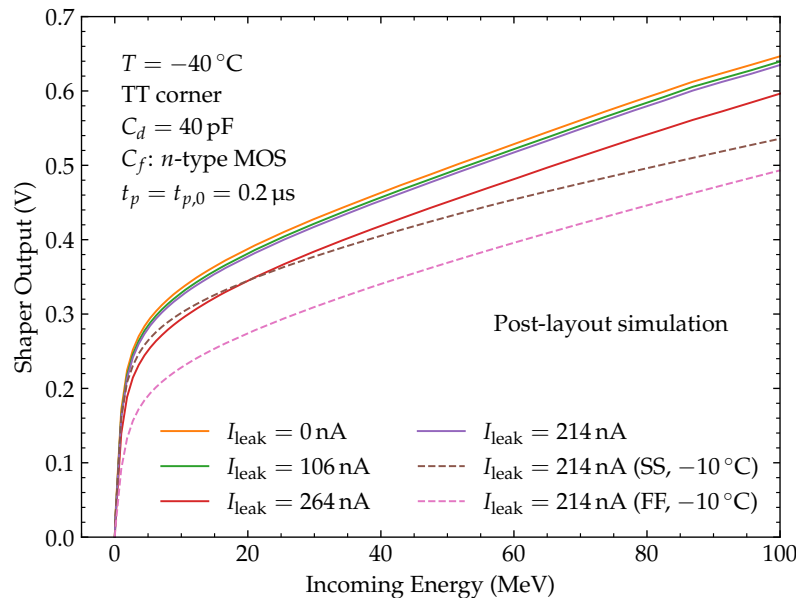


Figure 5. Channel transcharacteristic at the output of the CR–RC shaper for different leakage currents, illustrating the impact of detector leakage on dynamic signal compression in ANTARES4. Post-layout simulations were performed at -40 °C under the typical–typical (TT) process corner, with an input detector capacitance $C_d = 40$ pF, an n -type MOS feedback capacitor, and a peaking time $t_p = 0.2$ μ s. The curves are shown for leakage currents ranging from $I_{\text{leak}} = 0$ nA up to 264 nA. Additional simulations at $I_{\text{leak}} = 214$ nA were performed at -10 °C under the slow-slow (SS) and fast-fast (FF) process corners, highlighting the combined effect of temperature and process variations on the channel energy-to-voltage transcharacteristic.

Two additional simulations were carried out for $I_{\text{leak}} = 214$ nA at -10 °C under the slow-slow (SS) and fast-fast (FF) process corners. In these cases, the low-energy gain decreases to 133 μ V/keV $^{-1}$ and 152 μ V/keV $^{-1}$, respectively, while the output dynamic range is reduced by 15.6% and 22.1% with respect to the case at -40 °C under the typical corner with the same leakage current. The reduced gain at low energy is attributable both to the higher operating temperature and to the degradation induced by process variations in non-typical process corners.

Table 1 summarizes the variation in low-energy gain, high-energy gain, compression factor, and INL (index of non-linearity, defined as the relative deviation of the measured output voltage from the ideal linear response) as a function of leakage current and input capacitance at -40 °C. The compression factor k is defined as the ratio between the low-energy and high-energy gains, i.e., $k = G_{\text{le}}/G_{\text{he}}$, and quantifies the strength of dynamic signal compression in the CSA. The kink corresponds to the energy where the linear regime transitions from low-energy X-ray detection to high-energy particle detection.

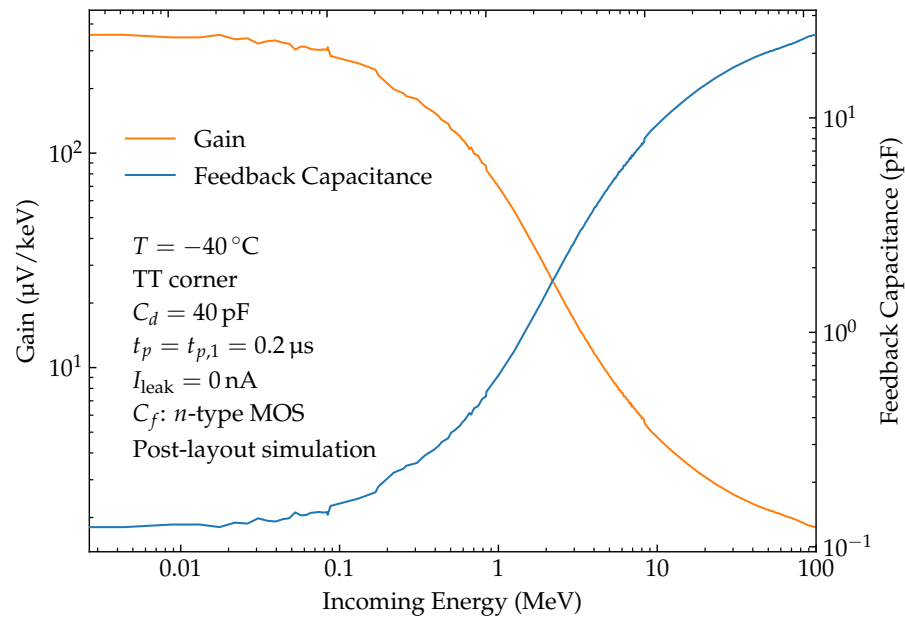


Figure 6. Channel transcharacteristic analysis at zero leakage current, showing the extracted gain and equivalent feedback capacitance as a function of input energy. Simulations were carried out at $-40\text{ }^{\circ}\text{C}$ under the typical–typical (TT) process corner, with $C_d = 40\text{ pF}$, an n -type MOS feedback capacitor, and a peaking time $t_p = 0.2\text{ }\mu\text{s}$. The simulation results highlight the effective compression behavior of the CSA for $I_{\text{leak}} = 0\text{ nA}$.

Table 1. Linearity, gain, and compression factor versus detector leakage current at $-40\text{ }^{\circ}\text{C}$ for a representative channel. G_{le} and G_{he} denote low- and high-energy gains, respectively; INL_{le} and INL_{he} are the indices of non-linearity in the low- and high-energy regions. The compression factor $k = G_{\text{le}}/G_{\text{he}}$ quantifies the transition from the high-gain X-ray regime to the compressed charged particle regime. The kink corresponds to the energy where the linear regime transitions from low-energy X-ray detection to high-energy particle detection.

I_{leak} (nA)	C_d (pF)	G_{le} ($\mu\text{V keV}^{-1}$)	INL_{le} (%)	G_{he} ($\mu\text{V keV}^{-1}$)	INL_{he} (%)	k –	Kink (keV)
0	0	305	0.31	3.21	1.78	95	1104
0	40	300	0.44	3.17	2.02	94	1129
106	40	268	0.49	3.16	1.93	84	1246
214	40	251	0.57	3.15	1.90	79	1312
264	40	208	0.39	3.05	2.07	68	1439

The simulation results show that under nominal flight conditions at $-40\text{ }^{\circ}\text{C}$, the low-energy gain G_{le} is approximately $300\text{ }\mu\text{V/keV}^{-1}$, with an index of non-linearity below 0.5% in the 10 keV to 100 keV X-ray region. As the leakage current increases to 214 nA, corresponding to on-ground calibration scenarios, the low-energy gain decreases by less than 20%, while the INL remains within 0.6%. Even at 264 nA, which exceeds the nominal design target, the channel remains functional, with the kink energy shifting towards higher values. These results confirm that the CSA architecture supports operation under both nominal flight conditions and elevated leakage currents during system integration and calibration.

4.2. Readout Channel Layout

Figure 7 shows the complete layout of a single ANTARES4 readout channel. The design fits within the $100\text{ }\mu\text{m}$ channel height constraint, with a total width of $363\text{ }\mu\text{m}$

and integrates the charge-injection circuit, leakage-current generator, CSA with dynamic signal compression (implemented here with the n -type MOS feedback variant), Krummenacher network, and programmable CR–RC shaper. In this configuration, the shaper output is selected for readout and routed to the corresponding ASIC pad through the analog output driver. Across the full ASIC, eight channels are implemented, four of which also include a dedicated leakage-current emulator for testing the extended-range compensation circuit during ASIC characterization.

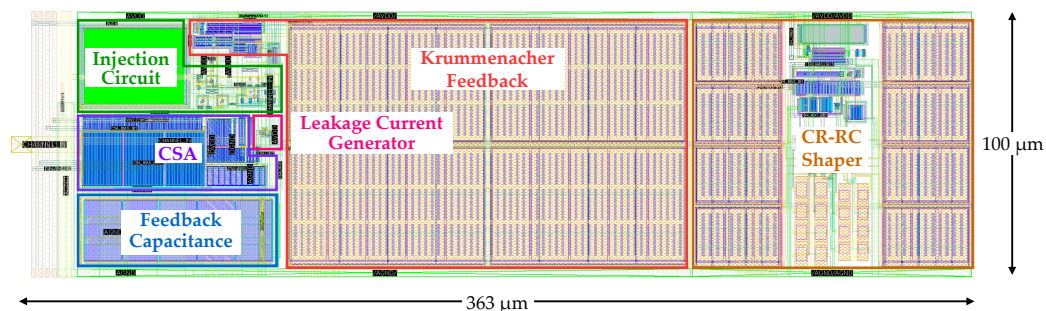


Figure 7. Layout of a single ANTARES4 readout channel, showing the charge-injection circuit, leakage-current generator, CSA with dynamic signal compression (implemented here with the n -type MOS feedback variant), Krummenacher network, and programmable CR–RC shaper with eight selectable peaking times. The shaper output is routed to the corresponding ASIC pad through the analog output driver. The layout fits within the 100 μm channel height constraint, with a total width of 363 μm .

5. Conclusions

The ANTARES4 prototype ASIC, implemented in a 65 nm CMOS process, has been developed as an R&D platform to evaluate circuit topologies for upgrading the GAPS Si(Li) tracker readout electronics for the second flight. The design introduces MOS-based dynamic signal compression in the CSA feedback network, extended-range leakage-current compensation, and a more compact channel layout compared to the previous SLIDER32 ASIC.

Post-layout simulation results show that the low-energy gain remains around 300 $\mu\text{V}/\text{keV}^{-1}$ under nominal flight conditions, with an INL below 0.5% in the X-ray region and below 2.1% at higher energies. The compression factor $k = G_{\text{le}}/G_{\text{he}}$ reaches about 95 under nominal leakage conditions and decreases with increasing leakage current, confirming the ability to handle input charges spanning nearly four decades. All key performance metrics, including low- and high-energy gains, compression factor, and kink energy, satisfy the design requirements.

The channel layout achieves a reduction in per-channel area of approximately 30% compared to SLIDER32, improving integration density while maintaining compatibility with the existing FEB and module footprint.

The ANTARES4 architecture scales to the full tracker channel count and is designed to replace approximately 360 SLIDER32 ASICs in the second-flight configuration. It features improved area efficiency, enhanced dynamic signal compression, and performance that fully satisfies the design requirements. Compared with the previous SLIDER32 implementation, the leakage-current compensation capability has been extended from appropriately 50 nA to more than 200 nA in the new 65 nm design. These advances provide a solid basis for optimizing the integration strategy and selecting the most suitable front-end design for future GAPS missions. The design has been submitted for fabrication, with full ASIC characterization planned on the fabricated prototypes.

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Abbreviations

The following abbreviations are used in this manuscript:

AMS-02	Alpha Magnetic Spectrometer-02
ASIC	Application-Specific Integrated Circuit
ASI	Agenzia Spaziale Italiana
BESS	Balloon-Borne Experiment with a Superconducting Spectrometer
CMOS	Complementary Metal-Oxide-Semiconductor
CSA	Charge-Sensitive Amplifier
ENC	Equivalent Noise Charge
FEB	Front-End Board
FWHM	Full Width at Half Maximum
GAPS	General AntiParticle Spectrometer
INFN	Istituto Nazionale di Fisica Nucleare
INL	Index of Non-Linearity
ISS	International Space Station
JAXA	Japan Aerospace Exploration Agency
LDB	Long Duration Balloon (Facility)
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NASA	National Aeronautics and Space Administration
OHP	Oscillating Heat Pipe
Si(Li)	Lithium-drifted Silicon Detector
ToF	Time-of-Flight

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