

# A 1 Grad TID-Tolerant Bandgap Voltage Reference for HEP Applications in 28 nm CMOS Node

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**Abstract**—This work presents the design and characterization of a radiation-hardened bandgap voltage reference circuit, fabricated using a commercial 28 nm CMOS technology, for applications in high-energy physics (HEP) experiments. The circuit was engineered to ensure stable performance under extreme radiation environments and wide temperature variations. Measurement results show a temperature coefficient of 11 ppm/°C at best over a temperature range of 100 °C (from −40 °C to 60 °C) and a line regulation of 2.5 mV at room temperature. The mean value of the output voltage is around 480 mV, with a maximum variation of 2% when exposed to a total ionizing dose (TID) of up to 1 Grad(SiO<sub>2</sub>). The power consumption is 325 μW at room temperature, and the circuit operates correctly with a supply voltage ranging from 0.65 to 1 V. The core area of the bandgap reference is 0.015 mm<sup>2</sup>. These results demonstrate the robustness of the proposed design for use in extreme radiation environments.

**Index Terms**—Bandgap voltage reference, CMOS technology, low-voltage, radiation-hardness, total ionizing dose (TID) effects.

## I. INTRODUCTION

THE high-luminosity upgrade of the Large Hadron Collider (HL-LHC) will contribute to extending the physics research and increasing its discovery potential for physics beyond the standard model. In addition to this, new research studies are being carried out for the so-called post-LHC era. In particular, a feasibility study for a next-generation hadron collider is underway at CERN to assess the technical and financial viability of such a facility. This facility, consisting in a first step of an electron-positron collider (FCC-ee) and a second machine, colliding protons (FCC-hh) in the same tunnel, would extend the high-energy physics (HEP) research to the end of the century [1].

In this context, powerful electronic circuits for future detectors in HEP experiments must improve the efficiency, speed, and accuracy of signal processing and data acquisition systems. In these years, the designers in the HEP microelectronics community are moving from the 65 nm technology node, used to implement the electronics in the high-luminosity upgrades of ATLAS and CMS [2], to the 28 nm process. This

process, which is the last planar microelectronics node, allows a remarkable increase in the density of digital circuits and the speed of the I/O circuits. From the radiation hardness point of view, it has been thoroughly studied and offers a better performance with respect to the 65 nm node [3], [4], [5], [6], [7].

For these reasons, several research groups worldwide are working on it to design the next generation of particle physics experiments [8]. Nonetheless, it is important to stress that the scaling from the 65 nm process to the 28 nm one brings along the reduction of the core supply voltage, from 1.2 to 0.9 V, which is not associated with a proportional scaling of the device threshold voltage. This limits the number of architectures that can be used in the design of analog building blocks and, in general, it makes designing circuits with the 28 nm node more complicated due to a reduced voltage headroom. Moreover, the manufacturing process of the 28 nm node is associated with more complex design rules, such as those related to transistor orientation and wafer density requirements. In particular, only vertical and straight transistor gates are allowed in the 28 nm process, which prevents the use of closed-layout techniques that in the past have helped to manage and increase the radiation hardness of circuits in HEP experiments. These difficulties result in longer design and characterization times. To alleviate this problem, workpackage 5 (WP5) of the Experimental Physics R&D program is developing several building blocks such as analog to digital converter (ADC), digital to analog converter (DAC), phase locked loop (PLL), bandgap reference, and some others to be made available to the HEP designers' community.

This work, carried out in collaboration among CERN, Italian Institute for Nuclear Physics (INFN), and the University of Bergamo, aims to develop a radiation-hard bandgap voltage reference using the 28 nm CMOS node to benefit the HEP community [9]. The design methodology and simulation results of the proposed circuit were previously presented in [10]. This present article focuses on the complete characterization of the circuit, with measurement results obtained from tests conducted in a climatic chamber and under ionizing radiation up to 1 Grad(SiO<sub>2</sub>). The novelty of this work lies in the demonstration that, through appropriate bias-current sizing, operating-point selection, and architectural simplicity, a standard commercial 28 nm CMOS technology can be exploited to implement a bandgap voltage reference with a limited output-voltage variation under extreme total-ionizing-dose irradiation, up to 1 Grad(SiO<sub>2</sub>), without relying on dedicated radiation-hardening-by-design techniques. This article is organized as

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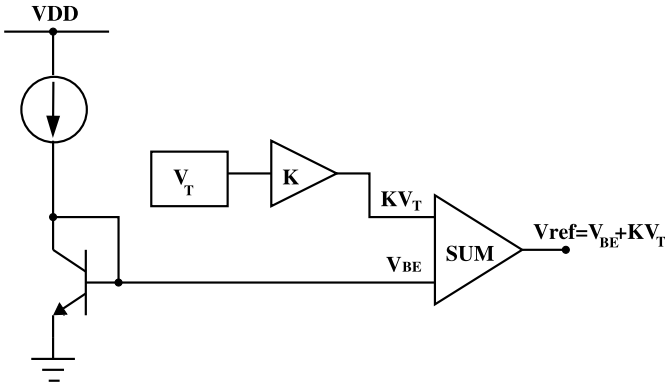


Fig. 1. Principle diagram of a bandgap voltage reference circuit.

follows. Section II provides an overview of the operating principle of bandgap voltage References, Section III details the proposed circuit, Section IV presents the experimental results, and Section V draws the conclusions.

## II. PRINCIPLE OF OPERATION

Bandgap voltage references are found in many electronic circuits such as flash memories, dynamic random access memories (DRAMs), current sources, ADCs, and DACs, and their performance is greatly affected by the accuracy of the reference voltage provided.

In general, as shown in Fig. 1, the reference voltage is obtained as the sum of a voltage proportional to the absolute temperature (PTAT) and a voltage with a negative temperature coefficient, complementary to the absolute temperature (CTAT) [11]. The latter is usually obtained from the voltage across a forward biased p-n junction or the base-emitter voltage ( $V_{BE}$ ) of a diode-connected bipolar junction transistor (BJT), while the PTAT voltage is obtained by taking the difference between the  $V_{BE}$ s of two bipolar transistors. This type of voltage reference, also known as voltage mode bandgap [12], produces an output voltage close to the intrinsic bandgap voltage ( $\approx 1.25$  V) of silicon.

Over the past few decades, CMOS transistors have undergone a rapid miniaturization process, as predicted by Moore's law [13], resulting in a progressive increase in performance in terms of functional density and processing speed [14]. This has led to a reduction in transistor dimensions and supply voltage. From the 130 nm CMOS node, the maximum supply voltage is 1.2 V, which limits the applicability of voltage mode bandgaps. Some design techniques that have been proposed to overcome this problem are based on the following.

- 1) Generating a fraction of the material bandgap by resistive subdivision (but at the cost of significant area consumption in low power applications) [15].
- 2) Using a low bandgap material such as germanium (expensive option and not available in a standard CMOS process) [16].
- 3) Using a dynamic threshold MOS transistor (DTMOST) with gate, drain, and substrate connected together, which behaves as a conventional diode but with a low operating voltage [17].

- 4) Using a current mode approach where two currents, one PTAT and one CTAT, are summed in the output branch, where a resistor produces an output voltage of less than 1 V and independent of temperature [18].

## III. RADIATION-TOLERANT APPROACH FOR BANDGAP REFERENCE CIRCUITS

In applications such as HEP experiments, nuclear medicine, or in the space environment, where electronic circuits are exposed to ionizing radiation or highly charged energetic particles, bandgap voltage references must be radiation-tolerant in addition to the characteristics described above. In CMOS processes, diodes are fabricated with a p-diffusion to a grounded n-well, while vertical parasitic pnp transistors are formed from a p-diffusion to n-well junction over a grounded p-substrate. Vertical pnp transistors are not well characterized in CMOS process design kits (PDKs) and offer limited robustness to process variations. In addition, these junctions are surrounded by shallow-trench-isolation regions, characterized by thick field oxides placed adjacent to the p-n junction. The positive trapped charge in these oxides degrades the  $I$ - $V$  characteristics of the p-n junction diode [19], [20]. Moreover, in the presence of highly charged energetic particles, displacement damage may also contribute to the performance degradation of diodes or bipolar transistors [21].

Some design strategies have been proposed in the literature to improve the tolerance of bandgap voltage references to ionizing radiation. Among them, two representative approaches have demonstrated effective mitigation of radiation-induced leakage and parameter shifts.

- 1) The first one, proposed in [22], introduces a dynamic base leakage compensation (DBLC) technique, which dynamically cancels the leakage current generated in the bandgap core under irradiation. This circuit-level compensation allows maintaining a stable reference voltage up to total-ionizing-dose levels of several MGy, without relying on any process modification. However, while the DBLC technique effectively compensates the leakage current, it does not address the displacement-damage effects that mainly affect the bipolar transistors used in traditional bandgap cores.
- 2) The second approach, developed in [23], replaces the conventional bipolar or diode core with a p-channel DTMOS-diode structure that can be implemented in any standard CMOS process. The device exhibits the exponential current-voltage characteristic of a diode while achieving the radiation hardness typical of enclosed-layout MOS transistors [22], [23], thanks to the thin-oxide region surrounding the source. This solution combines functional equivalence with enhanced robustness to oxide-trapped-charge accumulation and has been validated in 180 [24], 130 [23], and 65 nm CMOS technologies [25].

In the 28 nm CMOS node, the stringent design-rule constraints prevent the use of enclosed-layout geometries. Therefore, the design of a radiation-hard bandgap reference must rely on the intrinsic radiation hardness of the technology

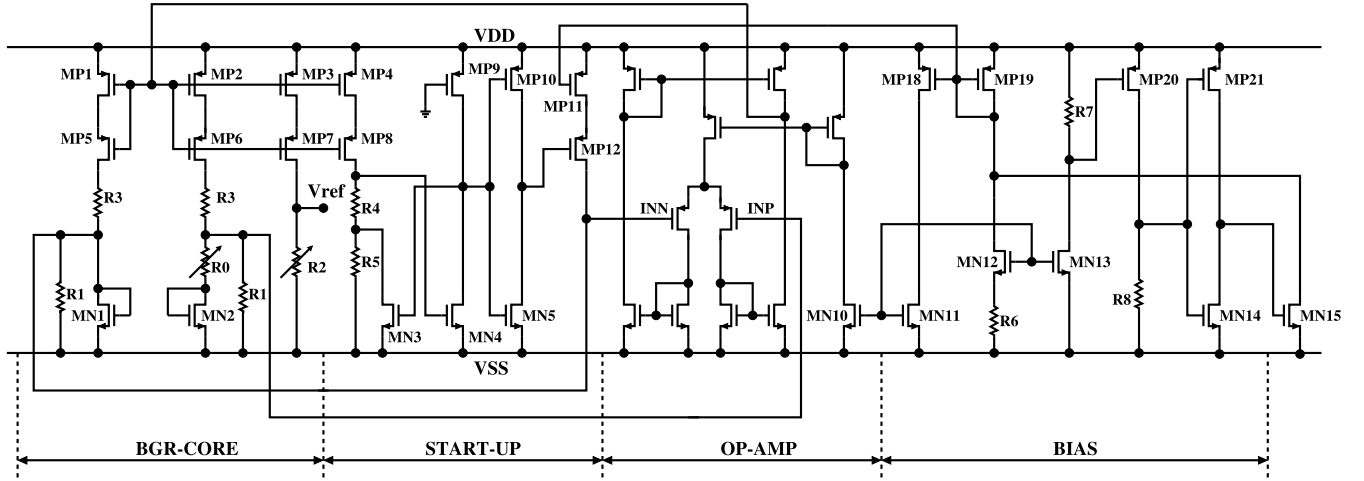


Fig. 2. Schematic of the proposed bandgap voltage reference circuit.

itself. In this article, for the first time to the best of the authors' knowledge, a bandgap voltage reference is designed without using ELT devices, due to the layout constraints imposed by the 28 nm process.

#### IV. CIRCUIT DESCRIPTION

The bandgap reference circuit proposed in this work and shown in Fig. 2 targets applications where tolerance to extremely high levels of ionizing radiation, total ionizing dose (TID  $\approx 1$  Grad and fluences  $\approx 10^{16}$  n<sub>eq</sub>/cm<sup>2</sup>), is a mandatory requirement. The core part of the bandgap consists of three branches connected to MP1–MP3, three pMOS transistors with the same aspect ratio ( $W/L$ ). Since they share the same gate contact, they supply the same current. Part of this current flows in R2, while the rest flows in MN1 and MN2, two nMOS transistors biased in the weak inversion region, emulating the p-n junction commonly used in bandgap voltage references.

The drain current of nMOS operating in the weak inversion region (with source and substrate connected) has an exponential characteristic with a temperature dependence similar to that of the BJT, which is given by the following equation [26]:

$$I_D = \mu C_{OX} \frac{W}{L} V_T^2 \cdot e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)} \cdot \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \quad (1)$$

where  $\mu$  is the mobility of carriers in the channel,  $C_{OX}$  is the oxide capacitance per unit area,  $W/L$  is the aspect ratio of the transistor,  $n$  is the sub-threshold slope factor,  $V_T$  is the thermal voltage, and  $V_{th}$  is the threshold voltage of the transistor. For  $V_{DS} > 5V_T$ , the equation can be approximated as follows:

$$I_D = I_0 \cdot e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)} \quad (2)$$

where [27]

$$I_0 = \mu C_{OX} \frac{W}{L} (n-1) V_T^2. \quad (3)$$

It is possible to demonstrate that the temperature coefficient of  $V_{GS}$  of an MOS biased in weak inversion is negative and that the difference between two  $V_{GS}$  is positive as the BJT case. Therefore, it is possible to replace a BJT with an MOS in a classical bandgap reference voltage design.

#### A. Operational Amplifier

The operational amplifier design is optimized for noise and offset minimization. The first stage is a classic operational transconductance amplifier based on a differential input pair whose generated differential current is sent to the second stage by a current mirror. The mirror also performs the differential to single-ended conversion. Due to the low headroom available, the cascode configuration was avoided at the cost of a lower gain (but sufficient for this application). The input pair has been designed with a large area and interdigitated layout to minimize mismatch effects leading to increased offset. During the design, the bandwidth of the amplifier was considered less important than gain and offset, as the temperature effects will be at very low frequencies, and therefore, the amplifier was loaded with a capacitor at the output to ensure stability (not present in Fig. 2). The input pair was chosen as pMOS mainly because of the need for a relatively low common mode, about 0.3 V. In the past, this had the advantage of lower  $1/f$  noise [28], but this is no longer the case for this technology [29].

#### B. Start-Up Circuit

A bandgap reference requires a start-up circuit to prevent the circuit from falling into the stable operating point where all currents and voltages are zero. At start-up, when there is no current flowing in the branches, transistor MN4 is off because its gate is at zero voltage. As a result, the input of the inverter, made up of transistors MP10 and MN5, is high, and therefore, the gate of MP12 is low. Accordingly, MP11 is on, injecting current into the negative input of the operational amplifier (INN). When the circuit reaches the steady state, the current flowing in MP4, R4, and R5 turns on MN4 and turns off MP12 (via the MN5–MP10 inverter), which stops the current injection in INN. A hysteresis loop is formed using transistor MN3 (which is on at start-up). When the circuit reaches steady state, MN3 is turned off and resistor R5 is added to R4 to prevent MN4 from being turned off by some voltage fluctuation.

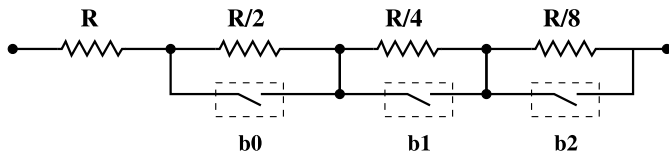


Fig. 3. Schematic of the trimming resistor network. Each resistor is implemented as a series of four resistors, three of which can be short-circuited by a pass gate.

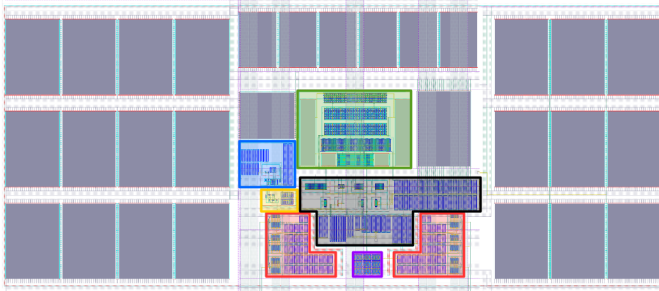


Fig. 4. Bandgap layout with functional blocks highlighted: red - trimming resistors, yellow - start-up, blue - bias, green - error amplifier, black - resistors and current sources, purple - diodes, and gray - decoupling capacitors.

### C. Programmability

With the deterioration in accuracy brought about by the shrinking of the minimum channel dimensions in advanced CMOS technologies, some programmability of the bandgap characteristics has been introduced through resistors R0 and R3. The spread of the two resistors was obtained from Monte Carlo simulations. The former controls the slope of the bandgap output voltage versus temperature characteristic, while the latter sets the absolute output voltage (it is worth pointing out that, if the bandgap is used to generate a trimmable reference current, the trimming of R3 can be ignored). Given the limited number of trimming bits (3 bits being a reasonable compromise between correction capability and the complexity of the associated control circuitry), defining the correct trimming range is essential: an excessively small R0 range would not compensate for larger process-induced drifts, while an excessively large range would degrade the effective trimming resolution. As a design rule, we extracted from Monte Carlo simulations the maximum positive and negative slopes of  $V_{OUT}$  as a function of temperature and set the trimming span to approximately  $1.5\times$  these extreme slopes, providing an adequate safety margin. As shown in Fig. 3, where the trimming resistor scheme is detailed, both programmable resistors have been implemented as a series of binary-weighted resistors, each provided with a pass-gate in parallel to short its terminals. To reduce the ON-resistance of the switches, MOSFETs with large width have been used.

### D. Layout

The layout of the bandgap, shown in Fig. 4, occupies  $360 \times 160 \mu\text{m}^2$  of the silicon area or  $130 \times 115 \mu\text{m}^2$ , excluding decoupling capacitors. To provide separation from the noise coming from neighboring blocks, the layout was surrounded using a native silicon ring, which offers higher resistance per square in comparison to p-well. Several best practices have

been implemented, in particular, increased spacing to the n-well edges to mitigate proximity effects and guard rings to minimize the probability of single event latchups (SELs). As mentioned above, enclosed layout transistors were not used due to polysilicon shape restrictions in the CMOS technology used.

### E. Operating Principle

The schematic of the bandgap also includes a self-cascode configuration that maintains the same  $V_{DS}$  for MP1–MP3, hence improving the performance of the current mirror and therefore the line regulation of the circuit. These results can also be achieved by adding to the output branch an active cascode configuration but at the expense of a larger area occupied by an operational amplifier. In the circuit, thanks to the high gain of the amplifier ( $\approx 45$  dB), the currents that flow in the resistors connected between its inputs and ground are about the same. Assuming the resistor values not affected by temperature, these currents are complementary and proportional to the temperature. In transistor, MP2, on top of this contribution, flows a current (proportional to the temperature) given by the ratio of the voltage drop across resistor R0 divided by its resistance. This voltage drop is given by the difference of the gate-to-source voltages of MN1 and MN2, which are biased with the same current (MP1 and MP2 are equal), but with different current densities (MN2 has a  $W/L$  ratio eight times larger than MN1). Thus, the output voltage of the circuit can be calculated as follows:

$$V_{OUT} = \left[ \frac{V_{GS_{MN1}}}{R_1} + \frac{\Delta V}{R_0} \right] \cdot R_2 \quad (4)$$

where  $V_{GS_{MN1}}$  is the gate-to-source voltage of MN1 and  $\Delta V$  is the voltage drop across the resistor R0. It is worth noting that, assuming the same temperature dependence for all the resistors, the output voltage is not influenced by the temperature coefficient of the resistors. The supply voltage is 0.9 V and the output voltage targets 480 mV.

## V. EXPERIMENTAL RESULTS

The bandgap circuit was fabricated in a commercial 28 nm CMOS technology. Its current consumption is  $360 \mu\text{A}$  ( $335 \mu\text{A}$  by the bandgap core and  $25 \mu\text{A}$  by the op-amp and bias section). The chip (shown in Fig. 5) was mounted on a carrier board connected to a motherboard, which has the purpose of biasing and controlling the circuit. The bandgap voltage reference was evaluated inside a climatic chamber to confirm its expected response to changes in temperature and supply voltage ( $V_{DD}$ ). The temperature behavior has been measured between  $-40^\circ\text{C}$  and  $60^\circ\text{C}$  with a step of  $10^\circ\text{C}$ . The temperature coefficients of these samples are defined as follows:

$$TC = \left[ \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{T_{MAX} - T_{MIN}} \cdot \frac{10^6}{V_{OUT}(20^\circ\text{C})} \right]. \quad (5)$$

Fig. 6 shows the output voltage variation as a function of temperature of three different circuits from the same wafer obtained before and after trimming of resistor R0 and R3. The

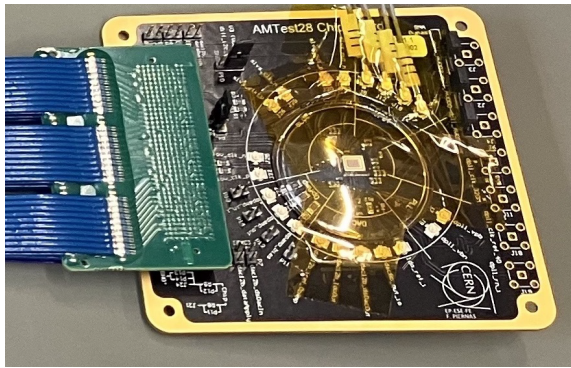


Fig. 5. Photograph of the ASIC on a carrier board with a flex cable connection to a motherboard (not in the picture).

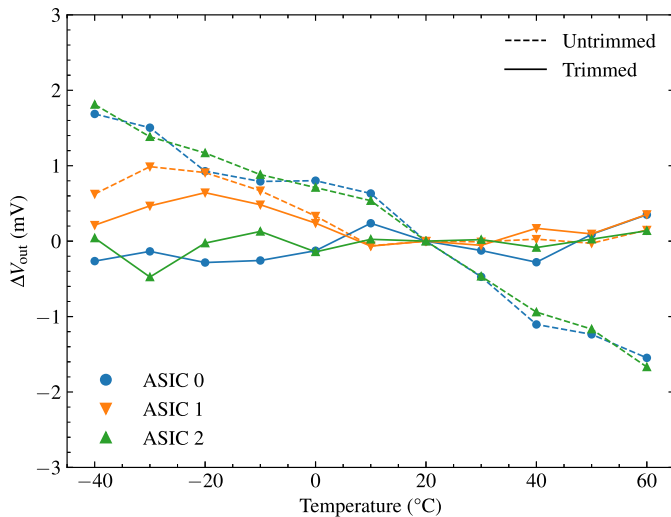


Fig. 6. Measured output voltage variation as a function of temperature for three ASICs from the same wafer. For each device, both the untrimmed (dashed lines) and trimmed (solid lines) responses are shown.

measured  $V_{OUT}$  variation after trimming is well below 1 mV, which corresponds to a temperature coefficient of 12, 14, and 11 ppm/ $^{\circ}\text{C}$  for ASIC 0, 1, and 2, respectively. The untrimmed values, which would have been obtained using fixed resistors equal to those corresponding to the 011 configuration, are 66, 21, and 71 ppm/ $^{\circ}\text{C}$  for ASIC 0, ASIC 1, and ASIC 2, respectively, demonstrating the importance of trimming in improving the temperature coefficient. The samples were also tested for variations in  $V_{DD}$ , ranging from 500 mV (the minimum voltage that can be applied by the voltage regulator on the test board) to 990 mV (nominal supply voltage plus 10%). As a representative case, the results for ASIC 2, shown in Fig. 7, indicate that the knee of the circuit shifts with temperature. However, even in the worst case, it operates at voltages significantly lower than the nominal supply voltage minus 10%. It is important to note that the circuit must be capable of operating within a supply voltage range that includes both the rated value and a 10% tolerance.

Focusing on the reference voltage range (0.81–0.99 V), we observe that for the three measured samples, configured with the same trimming configuration for R0 and R3, the output voltage shows a monotonic variation of less than  $\pm 1.5\%$  (Fig. 8).

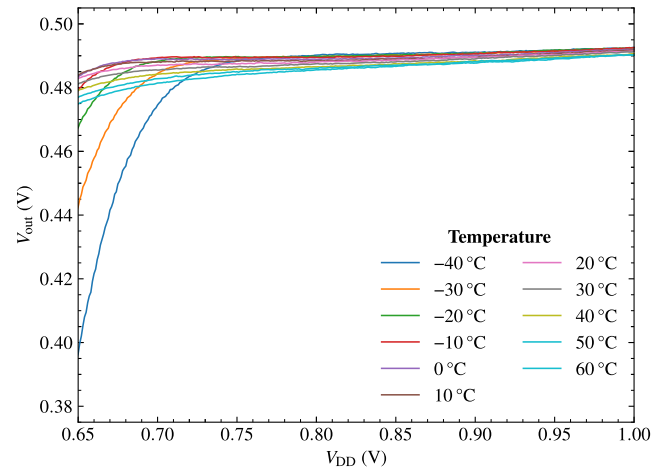


Fig. 7. Measured output voltage as a function of the supply voltage for different temperatures.

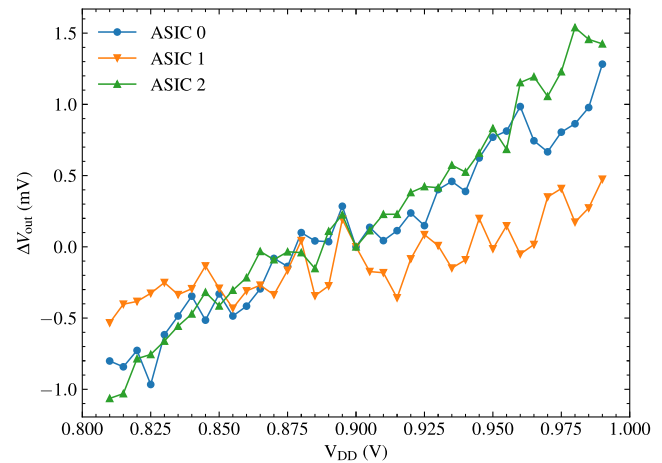


Fig. 8. Measured variation of the output voltage as a function of the supply voltage of three different samples with the same trimming configuration.

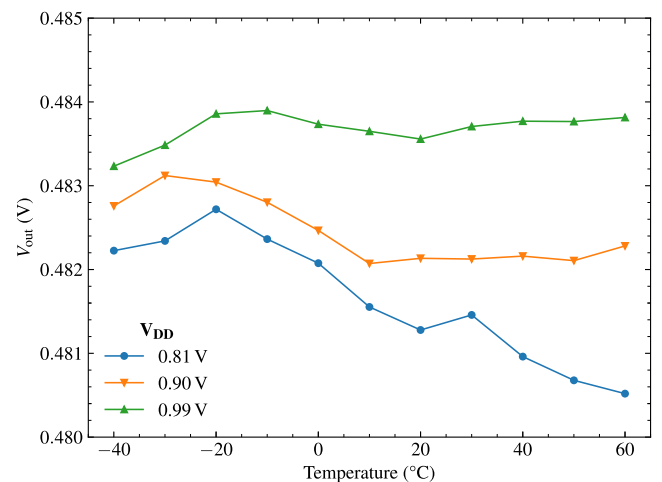


Fig. 9. Measured output voltage versus temperature of a trimmed sample at different supply voltages.

Fig. 9 shows the temperature behavior of a bandgap at three different supply voltages. The bandgap's temperature response is only slightly affected by variations in the supply voltage. The performance of the designed bandgap, compared

TABLE I  
PERFORMANCE SUMMARY OF THE PROPOSED BANDGAP CIRCUIT AND COMPARISON

| Parameter                           | This work      | Gromov [23]       | Vergine [25]      | Cao [22]                            | Boufouss [30]    | Chen [31]        | Bin [32]                        |
|-------------------------------------|----------------|-------------------|-------------------|-------------------------------------|------------------|------------------|---------------------------------|
| Supply voltage [V]                  | 0.9            | 1.2               | 1.2               | 1.2                                 | 2.5              | 1.8              | 1.8, 2.5, 2.5                   |
| Operating voltage range [V]         | 0.81 ÷ 0.99    | 0.85 ÷ 1.4        | 1.08 ÷ 1.32       | 0.85 ÷ 1.5                          | 1.08 ÷ 1.32      | 1.71 ÷ 1.89      | -                               |
| Nominal reference voltage [V]       | 0.48           | 0.405             | 0.33              | 0.6                                 | 1.5              | 0.66             | 0.69 – 0.72                     |
| Temperature coefficient [ppm/°C]    | 11             | 30.5              | 130               | 15                                  | 470              | -                | -                               |
| Temperature range [°C]              | -40 ÷ 60       | 0 ÷ 80            | -40 ÷ 80          | -40 ÷ 125                           | -40 ÷ 200        | -40 ÷ 125        | -60 ÷ 130                       |
| Power consumption @ 25°C [ $\mu$ W] | 325            | -                 | 240               | 60                                  | 50               | 450              | -                               |
| Radiation induced $\Delta V_{REF}$  | 2%<br>@ 1 Grad | 0.8%<br>@ 44 Mrad | 10%<br>@ 800 Mrad | $\pm 3\%$ (5 samples)<br>@ 450 Mrad | 5%<br>@ 1.5 Mrad | 4.5%<br>1.2 Mrad | 1.28%, 0.56%, 5.76%<br>1.2 Mrad |
| Layout Area [mm <sup>2</sup> ]      | 0.015          | 0.064             | 0.018             | 0.056                               | 0.09             | 0.02162          | -                               |
| CMOS Technology                     | 28 nm          | 130 nm            | 65 nm             | 130 nm                              | 130 nm SOI       | 28 nm            | 28, 40, 65 nm                   |

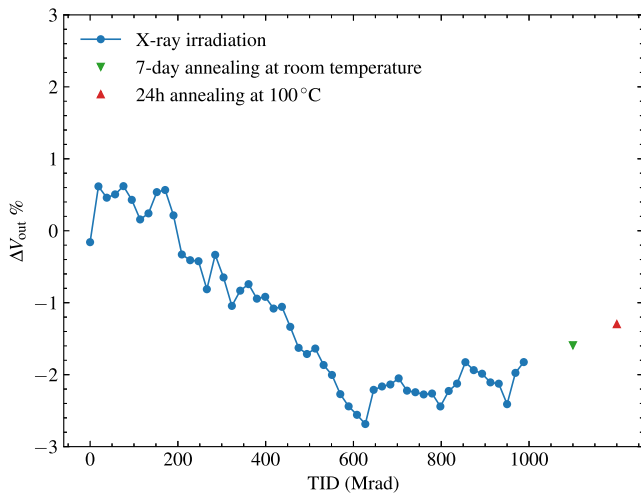


Fig. 10. Percentage variation of the output voltage as a function of the absorbed dose of 10 keV X-rays and after annealing at room (downward triangle) and at high (upward triangle) temperature.

with other works available in the literature, is summarized in Table I.

One sample has been irradiated up to a final dose of 1 Grad( $\text{SiO}_2$ ) with X-rays (10 keV average energy from a 40 keV tungsten tube). The dose rate was about 3.8 Mrad( $\text{SiO}_2$ )/h. Such TID is compatible with the vertex detector operation of the ATLAS and CMS experiments, High Luminosity LHC. During irradiation, the bandgap was biased as in real applications. After irradiation, two types of annealing were performed: one at room temperature and one at high temperature. Room temperature annealing, commonly used in radiation experiments, simulates long-term real operating conditions and was carried out for seven days to observe changes in the electrical parameters due to radiation damage and subsequent spontaneous recovery. The 100 °C annealing for 24 h, less common but useful for accelerating thermal recovery, helps to separate the effects of irreversible damage from transient ones. After both annealing treatments, the output voltage of the bandgap showed a modest recovery, remaining largely unchanged. Fig. 10 shows the variation of the output voltage as a function of the TID and after annealing. A shift of the output voltage of about 2% at 1 Grad( $\text{SiO}_2$ ) is apparent.

It is worth emphasizing that the aim of this article is not to study the degradation mechanisms induced by ionizing radiation, but to validate the designed circuit under this critical profile. Nevertheless, some qualitative considerations about the limited output shift can be made. A detailed analysis of the degradation mechanisms occurring in the circuit is not possible since the bandgap includes a large number of transistors operating under different bias conditions and geometries. However, the observed radiation hardness is consistent with the limited degradation of static and small-signal parameters reported for the same 28 nm CMOS technology in [7], where devices with dimensions comparable to those used in the bandgap exhibited threshold-voltage shifts of about 20–25 mV for nMOS devices and 15–20 mV for pMOS devices, and transconductance variations of roughly 5% for both at 1 Grad. As for the threshold-voltage variations, a possible explanation of the observed behavior is the following. Assuming, as a first approximation, that the current through the pMOS devices remains constant thanks to the amplifier's feedback loop, an increase in the nMOS threshold voltage increases the voltage across resistor R1, thereby stealing current from R0. This reduces the second term in (4) and consequently decreases the current flowing through the two nMOS transistors. This reduction in current leads to a smaller increase in the gate-to-source voltage of the nMOS devices than would have occurred at constant current as a result of the threshold-voltage shift. The combination of these two effects results in a post-irradiation output voltage that is lower than the pre-irradiation value, but only to a limited extent (about 2% and 3%). The relatively small variation in threshold voltage exhibited by the 28 nm CMOS technology, therefore, appears to be the key factor underlying the radiation hardness of the bandgap. In light of the results reported in [7], it may be beneficial, in a future version, to further improve the radiation tolerance by using MOS transistors with minimum channel length, which, at least for nMOS devices, show a smaller threshold-voltage shift under irradiation.

## VI. CONCLUSION

In this article, a bandgap voltage reference circuit in a 28 nm CMOS process for the high luminosity upgrades of the Large Hadron Collider has been designed. The proposed circuit, to be operated in the range from -40 °C to 60 °C,

has been characterized in a climatic chamber with good results in terms of temperature coefficient and line regulation. Given the foreseen application, its radiation hardness has been assessed with X-rays up to 1 Grad(SiO<sub>2</sub>) yielding up to 2% voltage variation at the final dose. Its ability to face very high radiation doses keeping a reasonable output voltage accuracy, a relatively small area, and a simple architecture, makes this circuit a candidate for integrated circuits that will be designed using 28 nm CMOS technology in the coming years.

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#### REFERENCES

- [1] A. Abada et al., "FCC-HH: The hadron collider: Future circular collider conceptual design report volume 3," *Eur. Phys. J. Special Topics*, vol. 228, no. 4, pp. 755–1107, Jul. 2019, doi: [10.1140/epjst/e2019-900087-0](https://doi.org/10.1140/epjst/e2019-900087-0).
- [2] N. Demaria et al., "Recent progress of RD53 collaboration towards next generation pixel read-out chip for HL-LHC," *J. Instrum.*, vol. 11, no. 12, Dec. 2016, Art. no. C12058.
- [3] C.-M. Zhang et al., "Characterization of GigaRad total ionizing dose and annealing effects on 28-nm bulk MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 10, pp. 2639–2647, Oct. 2017.
- [4] S. Mattiazzo et al., "Total ionizing dose effects on a 28 nm Hi-K metal-gate CMOS technology up to 1 Grad," *J. Instrum.*, vol. 12, no. 2, Feb. 2017, Art. no. C02003, doi: [10.1088/1748-0221/12/02/c02003](https://doi.org/10.1088/1748-0221/12/02/c02003).
- [5] S. Bonaldo et al., "Influence of halo implantations on the total ionizing dose response of 28-nm pMOSFETs irradiated to ultrahigh doses," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 82–90, Jan. 2019, doi: [10.1109/TNS.2018.2876943](https://doi.org/10.1109/TNS.2018.2876943).
- [6] S. Bonaldo et al., "Ionizing-radiation response and low-frequency noise of 28-nm MOSFETs at ultrahigh doses," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1302–1311, Jul. 2020.
- [7] G. Traversi, L. Gaioni, M. Manghisoni, L. Ratti, V. Re, and E. Riceputi, "Ionizing radiation effects of 3-Grad TID on analog and noise performance of 28-nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 72, no. 10, pp. 3343–3350, Oct. 2025, doi: [10.1109/TNS.2025.3542230](https://doi.org/10.1109/TNS.2025.3542230).
- [8] M. Pillar et al., "Generic analog 8 bit DAC IP block in 28 nm CMOS for the high energy physics community," in *Proc. Austrochip Workshop Microelectron. (Austrochip)*, Oct. 2022, pp. 5–8.
- [9] F. Bandi et al., "Analog IP blocks in 28 nm CMOS for the high energy physics community: SLVS transmitter and receiver," *J. Instrum.*, vol. 18, no. 1, Jan. 2023, Art. no. C01039.
- [10] G. Traversi, L. Gaioni, R. Ballabriga, D. Ceresa, and S. Michelis, "Design of a radiation-tolerant bandgap voltage reference for HEP applications," presented at the IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC), Nov. 2022, doi: [10.1109/nss/mic44845.2022.10398970](https://doi.org/10.1109/nss/mic44845.2022.10398970).
- [11] R. J. Widlar, "New developments in IC voltage regulators," *IEEE J. Solid-State Circuits*, vol. SSC-6, no. 1, pp. 2–7, Feb. 1971.
- [12] K. E. Kuijk, "A precision reference voltage source," *IEEE J. Solid-State Circuits*, vol. SSC-8, no. 3, pp. 222–226, Jun. 1973.
- [13] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 1965.
- [14] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a (1/4) micrometer MOSFET design," *IEEE Trans. Electron Devices*, vol. ED-31, no. 4, pp. 452–462, Apr. 1984.
- [15] H. Neuteboom, B. M. J. Kup, and M. Janssens, "A DSP-based hearing instrument IC," *IEEE J. Solid-State Circuits*, vol. 32, no. 11, pp. 1790–1806, Nov. 1997, doi: [10.1109/4.641702](https://doi.org/10.1109/4.641702).
- [16] J. W. Kim, B. Murmann, and R. Dutton, "Hybrid integration of bandgap reference circuits using silicon ICs and germanium devices," presented at the 9th Int. Symp. Quality Electron. Design (ISQED), Mar. 2008, doi: [10.1109/isqed.2008.4479770](https://doi.org/10.1109/isqed.2008.4479770).
- [17] A.-J. Annema, "Low-power bandgap references featuring DTMOSTs," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 949–955, Jul. 1999.
- [18] H. Banba et al., "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.
- [19] P. Moreira. (Feb. 2004). *Radiation Effects on the CERN Bandgap Circuit*. [Online]. Available: <http://proj-qpll.web.cern.ch/proj-qpll/images/bandgapRadEffects.pdf>
- [20] G. Traversi et al., "Characterization of bandgap reference circuits designed for high energy physics applications," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 824, pp. 371–373, Jul. 2016.
- [21] B. G. Rax, "Degradation of precision reference devices in space environments," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 1939–1944, Dec. 1997, doi: [10.1109/23.658965](https://doi.org/10.1109/23.658965).
- [22] Y. Cao, W. De Cock, M. Steyaert, and P. Leroux, "A 4.5 MGy TID-tolerant CMOS bandgap reference circuit using a dynamic base leakage compensation technique," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2819–2824, Aug. 2013.
- [23] V. Gromov, A. J. Annema, R. Kluit, J. L. Visschers, and P. Timmer, "A radiation hard bandgap reference circuit in a standard 0.13 μm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2727–2733, Dec. 2007.
- [24] B. M. McCue et al., "A wide temperature, radiation tolerant, CMOS-compatible precision voltage reference for extreme radiation environment instrumentation systems," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 2272–2279, Jun. 2013, doi: [10.1109/TNS.2013.2257850](https://doi.org/10.1109/TNS.2013.2257850).
- [25] T. Vergine, M. De Matteis, S. Michelis, G. Traversi, F. De Canio, and A. Baschiroto, "A 65 nm rad-hard bandgap voltage reference for LHC environment," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 3, pp. 1762–1767, Jun. 2016.
- [26] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed., New York, NY, USA: Mc Graw-Hill, 1999.
- [27] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 2002.
- [28] K. O. Kenneth, N. Park, and D.-J. Yang, "1/f noise of NMOS and PMOS transistors and their implications to design of voltage controlled oscillators," in *Proc. IEEE Radio Freq. Integr. Circuits (RFIC) Symposium. Dig. Papers*, Seattle, WA, USA, Aug. 2002, pp. 59–62, doi: [10.1109/RFIC.2002.1011510](https://doi.org/10.1109/RFIC.2002.1011510).
- [29] G. Traversi, L. Gaioni, L. Ratti, V. Re, and E. Riceputi, "Characterization of a 28 nm CMOS technology for analog applications in high energy physics," *IEEE Trans. Nucl. Sci.*, vol. 71, no. 4, pp. 932–940, Apr. 2024.
- [30] E. Boufouss, P. Gérard, P. Simon, L. A. Francis, and D. Flandre, "High temperature and radiation hard CMOS SOI sub-threshold voltage reference," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2013, pp. 1–2.
- [31] J. Chen et al., "ASET and TID characterization of a radiation hardened bandgap voltage reference in a 28-nm bulk CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 5, pp. 1141–1147, May 2022.
- [32] L. Bin, W. Yi, C. Jianjun, C. Yaqing, and Y. Xiaohu, "Technology dependency of TID response for a custom bandgap voltage reference in 65 nm to 28 nm bulk CMOS technologies," *Chin. J. Electron.*, vol. 32, no. 6, pp. 1286–1292, Nov. 2023.