GENERAL CHAIR'S WELCOME

Welcome to San Francisco and the 43rd Design Automation Conference! San Francisco is an excellent venue for DAC, with its proximity to many high-tech companies, its beautiful location, and a wide variety of activities and sights. DAC's return to San Francisco after eight years of absence promises a lively and especially well-attended event. Thousands of executives, managers, designers, academics, journalists, and others are converging here during DAC, the largest and most prestigious event focused on the design of electronic circuits and systems.

The technical program, which received a record 865 regular paper submissions, includes hot topics such as low power, DFM, and ESL among many others. This year, it sees an increase in design papers and includes two new topics: beyond-the-die, and emerging technologies. Overall, the program contains more than 200 technical presentations in 11 tracks, eight technical program panels, seven special sessions, and seven full-day tutorials – all led by widely respected industry experts. Full-day tutorials are being held Monday and Friday, and cover a wide range of topics including DFM, verification, ESL, embedded systems, chip-package co-design, and test.

DAC is highlighting a special MEGa theme – Multimedia, Entertainment, and Games – found throughout the program in all three keynotes, several pavilion sessions, and in a full day of technical sessions on Wednesday. Topics will range from issues faced in the design of the iPod, to technology requirements for 3D graphics in feature films, to power management for next-generation media applications. This promises to be an exciting part of the program as the topic is timely, exposes cutting-edge problems, and touches everyone's lives.

Three keynote addresses will be held this year. Monday's keynote is Joe Costello, appearing nearly 10 years after leaving his post as Cadence's CEO. His recent endeavor has been serving as Chairman of Orb Networks, Inc., a company working to bring media to mobile devices, and his talk will focus on today's macro consumer trends. Tuesday's keynote is Hans Stork, Senior Vice President and CTO of Texas Instruments Inc., who brings a wealth of experience and knowledge in process technologies. He will address issues in the sub-50nm processes that enable SoCs in mobile communication devices of the future. On Thursday, DAC welcomes Alessandro Cremonesi, VP of Strategy and System Technology and General Manager of Advanced System Technology at STMicroelectronics, who has been leading ST's efforts in SoC design. He will deliver a keynote on the challenges of convergence – handling the increased complexity at the system, embedded software, and silicon implementation level.

DAC has again organized Management Day to be held Tuesday, offering mid- and senior-level design managers a forum for sharing information on technology trends and decision-making processes.

The exhibit floor is crowded and will be lively with more than 240 exhibitors. On the floor, be sure to visit the DAC pavilion which returns with a full schedule of 18 panels, the MEGa theme booth with exciting demos, and the networking opportunities at the Monday exhibit floor happy hour. Hands-on tutorials given by exhibitors are scheduled throughout the week, all covering low-power design.

DAC promises to be a great learning experience. Advancements, research and insights that the global design community brings to this year's event has something to interest everyone.

It is the contributions of many people that make DAC the success that it has been for over four decades as the premier design automation event. The technical program participants and the many volunteer committees work to provide the core of the program content and direction for future years. Conference Managers MP Associates, Inc. continue to be focused on DAC's success. We are grateful for the support of our sponsors, ACM/SIGDA, IEEE/CASS/CANDE/CEDA, and the EDA Consortium.

Enjoy an educational and exciting week at DAC in San Francisco!

Best regards,
Ellen Sentovich
General Chair, 43rd DAC

PROCEEDINGS OF THE 43RD DESIGN AUTOMATION CONFERENCE®

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Organizers: Pai Chou & Peter Marwedel

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Organizers: James Hoe & Rajeev Murgai

SESSION 33: Low-Power, Thermal-Aware Architectures

Chair: Kevin Skadron *(University of Virginia)*
Organizers: Diana Marculescu & Naehyuck Chang

SESSION 55: Low Power Circuit Design

Chair: Ali Keshavarzi *(Intel Corporation)*
Organizers: Naehyuck Chang & Trevor Mudge

SESSION 56: Beyond-The-Die Circuit and System Integration

Chair: Shauki Elassaad *(Emergent Design Solutions)*
Organizers: John Berrie & Mike Heimlich

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Chair: Luca Daniel *(Massachusetts Institute of Technology)*
Organizers: Koen Lampaert & Rob A. Rutenbar

SESSION 62: Placement

Chair: Bill Halpin *(Synplicity, Inc.)*
Organizers: Jiang Hu & Louis Scheffer

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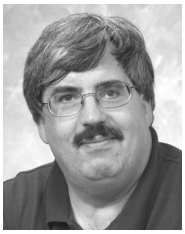

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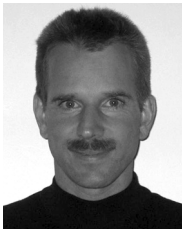

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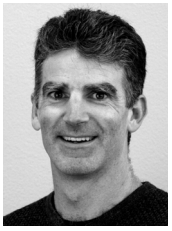

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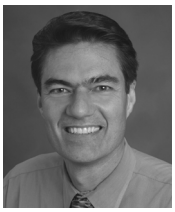

Joe Costello
Chairman of the Board,
Orb Networks, Inc.

iPod or Iridium – Which One Are You Going To Be?

Abstract: An incredible amount of time, resources and investment is being made by EDA, chip, and electronics companies to win in the exploding multi-media, gaming, and entertainment applications markets. With the 2006 DAC conference doing a much-needed "deep dive" into how the semiconductor industry meets technical challenges, Joe Costello, Chairman of Orb Networks, Inc., will turn the spotlight away from technology and onto today's macro consumer trends.

During this session, Joe challenges participants with this fundamental question: are you going in the right direction? As you bend your minds with the complexity of implementing modern day systems and chips, are you racing toward the right finish line? What are consumers really looking for? What will convergence really lead to and are you positioned to take advantage of all it will bring our industry and our world? Join Joe as he reveals lessons learned and offers a simple view of the future of electronics.

Biography: Joe Costello is chairman, co-founder, and an investor in Orb Networks, Inc. He is highly regarded for his business acumen and bold moves in the high-tech industry. In 1997, Chief Executive Magazine named Costello the top performing CEO of all publicly traded companies in North America. He also made Upside Magazine's 1997 "Elite 100" list of the top executives leading the digital revolution. He serves as CEO and chairman of think3, a developer of computer-aided design software used throughout the product development process. He is also chairman of other privately-held companies that include Readio, Abazab and SpeakESL. In addition, Costello is on the board of Mercury Interactive, a publicly-held company. Prior to think3, Costello played a pivotal role as president and CEO at Cadence Design Systems, Inc. for more than a decade. Under his leadership, Cadence became the world's leading supplier of electronic EDA software and services, and one of the ten highest-grossing software vendors in the world. Costello holds a bachelor of science degree in mathematics and physics from Harvey Mudd College, a master of science degree in physics from Yale University, and a master of science degree in physics from the University of California, Berkeley.

GENERAL SESSION KEYNOTE ADDRESS

Hans Stork
Senior Vice President and Chief Technology Officer,
Director of Silicon Technology Department
Texas Instruments Inc.

Structuring Process and Design for Future Mobile Communication Devices

Abstract: The density and speed of sub-50nm CMOS technology enables the design of multi-functional SoCs for highly integrated, mobile, communication devices. At the same time, process variations, power issues and complexity of scope are challenging even the most advanced simulation capabilities. The growing design complexity is addressed by rapidly improving modeling of systematic manufacturing variations and design sensitivities. Physical design is becoming more structured to allow for process optimized design rules and efficient automation. While challenges remain in the scaling and optimization of analog and I/O functions, highly integrated, mobile communication devices are a major driving force for continued economies of scaling.

Biography: Dr. Stork is Senior Vice President, and Chief Technology Officer, of Texas Instruments. As Director of the Silicon Technology Development organization, he is responsible for ensuring that process technology provides a competitive advantage for TI's products.

Prior to joining Texas Instruments in 2001, Dr. Stork was Director of the ULSI Research Lab and later the Internet Systems and Storage Lab at HP Laboratories, Hewlett-Packard. Dr. Stork started his professional career at IBM's T.J. Watson Research Center, working on advanced bipolar technology and circuits, and his group demonstrated the early successes SiGe HBTs.

Dr. Stork serves on the Board of Directors for International Sematech and the Semiconductor Research Corporation (SRC). He also serves on the Governing Councils of the Focus Center Research Programs and Nanotechnology Research Initiative. He is a member of the SIA Technology Strategy Committee.

THURSDAY KEYNOTE ADDRESS

Alessandro Cremonesi
Strategy and System Technology Group Vice President
and Advanced System Technology General Manager,
STMicroelectronics

The Challenges of Convergence

Abstract: In this talk, the trends of the major application fields in the era of convergence are analyzed. The emphasis is on the challenges the semiconductor industry will have to face to address these new trends and opportunities.

Applications are becoming increasingly complex and the need to guarantee the coexistence of a wider range of applications on a single chip makes system-level integration a real challenge. Most of the applications will run on platforms designed for portable products, pushing the industry to emphasize power budgets for new designs, both at silicon and at system level. From the platform architecture perspective, multiprocessing is already a reality and the industry will have to find new paradigms to handle the increased complexity at the system, embedded software, and at the silicon implementation level.

The talk concludes with future perspectives, from the viewpoint of ST's advanced research organization.

Biography: Alessandro Cremonesi received a Doctorate in Electronics Engineering from the University of Pavia, Italy, in 1984. After a period of research activity in the opto-electronics field at the University of Pavia, he joined STMicroelectronics working in different fields from telecommunications to audio/video digital signal processing and multimedia applications. At present, Alessandro Cremonesi is Vice President of Strategy and System Technology group and General Manager of Advanced System Technology (AST) group at STMicroelectronics with the responsibility of the Corporate System R&D and the Corporate Strategic Marketing activities across 14 different STMicroelectronics Labs worldwide.

Marie R. Pistilli Women in EDA Achievement Award

Ellen J. Yoffa – Director of Next Generation Web, IBM T.J. Watson Research Center, Yorktown Heights, NY

For her significant contributions in helping women advance in the field of EDA technology.

The P. O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P. O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship, and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to 5 years, to graduating high school seniors.

The 2006 winners are:

Katlyn DeLuca – attending University of Massachusetts, Lowell, MA

Eletha Flores – attending Massachusetts Institute of Technology, Cambridge, MA

For more information about the P. O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems." Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. **Jennifer L. Dworak**, Division of Engineering – Electrical Sciences and Computer Engineering, Brown University, Providence, RI

Student: **Elif Alpaslan**

A Statistical Coverage Metric and Stimulus Generation Approach for Design Verification Based upon Structural Analysis of the Design and Stimulus

Prof. **Daniel Kroening**, Computer Systems Institute, Swiss Institute of Technology, Zurich, Switzerland

Student: **Vijay D'silva**

Automatic Detection of Multi-Cycle Paths in Large Circuits

Information on next year's DAC scholarship award program will be available on the DAC web site: http://www.dac.com.

DAC/ISSCC 2006 Student Design Contest Winners

Operational Chip Design Category:

1st Place *A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW*

(Best Overall) Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni – University of Pisa
Bert Gyselinckx, Liesbet Van der Perre, Geert Van der Plas – IMEC

2nd Place (tie) *Increasing the Time Dynamic Range of Pulse Measurement Techniques in Digital CMOS*

Mona Safi-Harb, Gordon W. Roberts – McGill University

2nd Place (tie) *A DSP Enabled Microsystem for Cochlear Implants with Hybrid LC Clocking*

Eric D. Marsman, Robert M. Senger – University of Michigan
Richard B. Brown – University of Utah

3rd Place *A 160K Gates/4.5KB SRAM H.264 Video Decoder for HDTV Applications*

Chien-Chang Lin, Jia-Wei Chen, Hsiu-Cheng Chang, Chao-Ching Wang, Yi-Huan Ou-Yang, Ming-Chih Tsai, Yao-Chang Yang, Jiun-In Guo, Jinn-Shyan Wang – National Chung Cheng University

Operational System Design Category:

1st Place *Demonstration of Uncoordinated Multiple Access in Optical Communications*

Herwin Chan, Andres I. Vila Cadaso, Juthika Basak, Miguel Griot, Wen-Yen Weng, Richard Wesel, B. Jalali, Eli Yablonovitch – University of California, Los Angeles
Ingrid Verbauwhede – University of California, Los Angeles & Katholieke University, Leuven

2nd Place *Illumimote: A High Performance Light Sensor Module for Wireless Sensor Networks*

Heemin Park, Jonathan Friedman, Mani B. Srivastava, Pablo Gutierrez, Vidyut Samanta, Jeff Burke – University of California, Los Angeles

3rd Place *An Ultra Low Power Wireless Micro-Sensor Node*

Denis Daly, Daniel Finchelstein, Nathan Ickes, Naveen Verma, Anantha Chandrakasan – Massachusetts Institute of Technology

Honorable Mention *Phase Delay Based Collision Avoidance RADAR for Smart Automobiles*

Babu L. Saincha – Indian Institute of Information Technology

Conceptual Category:

1st Place *ASIC Implementation of LDPC Decoder Accelerating Message-Passing Schedule*

Kazunori Shimizu, Tatsuyuki Ishikawa, Nozomu Togawa, Takeshi Ikenaga, Satoshi Goto – Waseda University

The ACM Transactions on Design Automation of Electronic Systems (TODAES) 2006 Best Paper Award

Zero Cost Indexing for Improved Processor Cache Performance
Volume 11, Issue 1, January 2006, Pages 3–25

Tony Givargis – University of California, Irvine, CA

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) Distinguished Service Award

Robert A. Walker – Kent State University, Kent, OH

For dedicated service as SIGDA Chair (2001–2005), and over a decade of service to SIGDA, DAC, and the EDA profession

2005 Phil Kaufman Award for Distinguished Contributions to EDA

Phil Moorby – Chief Scientist, Synopsys, Inc.

Phil Moorby is the recipient of the prestigious EDA Consortium 2005 Phil Kaufman Award for industry contributions as the inventor of the Verilog hardware design language (HDL) which has become, and today remains, one of the world's most popular electronic design languages.

IEEE Circuits and Systems Society 2006 Education Award

Wayne Wolf – Princeton University, Princeton, NJ

For outstanding education and leadership in VLSI systems and embedded computing

IEEE Circuits and Systems Society 2006 Industrial Pioneer Award

John A Darringer – IBM T. J. Watson Research Center, Yorktown Heights, NY

For the development of practical techniques and algorithms for automated logic synthesis, for their realization as usable tools, and for their successful application to high performance computing products

IEEE Circuits and Systems Society 2006 Donald O. Pederson Award

Janusz Rajski – Mentor Graphics Corp., Wilsonville, OR

Jerzy Tyszer – Poznan University of Technology, Poznan, Poland

Mark Kassab – Mentor Graphics Corp., Wilsonville, OR

Nilanjan Mukherjee – Mentor Graphics Corp., Wilsonville, OR

For the paper entitled, *Embedded Deterministic Test*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 5, pp. 776–792, May 2004