

GENERAL CHAIR'S WELCOME

Welcome to San Francisco and the 43rd Design Automation Conference! San Francisco is an excellent venue for DAC, with its proximity to many high-tech companies, its beautiful location, and a wide variety of activities and sights. DAC's return to San Francisco after eight years of absence promises a lively and especially well-attended event. Thousands of executives, managers, designers, academics, journalists, and others are converging here during DAC, the largest and most prestigious event focused on the design of electronic circuits and systems.

The technical program, which received a record 865 regular paper submissions, includes hot topics such as low power, DFM, and ESL among many others. This year, it sees an increase in design papers and includes two new topics: beyond-the-die, and emerging technologies. Overall, the program contains more than 200 technical presentations in 11 tracks, eight technical program panels, seven special sessions, and seven full-day tutorials – all led by widely respected industry experts. Full-day tutorials are being held Monday and Friday, and cover a wide range of topics including DFM, verification, ESL, embedded systems, chip-package co-design, and test.

DAC is highlighting a special MEGa theme – Multimedia, Entertainment, and Games – found throughout the program in all three keynotes, several pavilion sessions, and in a full day of technical sessions on Wednesday. Topics will range from issues faced in the design of the iPod, to technology requirements for 3D graphics in feature films, to power management for next-generation media applications. This promises to be an exciting part of the program as the topic is timely, exposes cutting-edge problems, and touches everyone's lives.

Three keynote addresses will be held this year. Monday's keynote is Joe Costello, appearing nearly 10 years after leaving his post as Cadence's CEO. His recent endeavor has been serving as Chairman of Orb Networks, Inc., a company working to bring media to mobile devices, and his talk will focus on today's macro consumer trends. Tuesday's keynote is Hans Stork, Senior Vice President and CTO of Texas Instruments Inc., who brings a wealth of experience and knowledge in process technologies. He will address issues in the sub-50nm processes that enable SoCs in mobile communication devices of the future. On Thursday, DAC welcomes Alessandro Cremonesi, VP of Strategy and System Technology and General Manager of Advanced System Technology at STMicroelectronics, who has been leading ST's efforts in SoC design. He will deliver a keynote on the challenges of convergence – handling the increased complexity at the system, embedded software, and silicon implementation level.

DAC has again organized Management Day to be held Tuesday, offering mid- and senior-level design managers a forum for sharing information on technology trends and decision-making processes.

The exhibit floor is crowded and will be lively with more than 240 exhibitors. On the floor, be sure to visit the DAC pavilion which returns with a full schedule of 18 panels, the MEGa theme booth with exciting demos, and the networking opportunities at the Monday exhibit floor happy hour. Hands-on tutorials given by exhibitors are scheduled throughout the week, all covering low-power design.

DAC promises to be a great learning experience. Advancements, research and insights that the global design community brings to this year's event has something to interest everyone.

It is the contributions of many people that make DAC the success that it has been for over four decades as the premier design automation event. The technical program participants and the many volunteer committees work to provide the core of the program content and direction for future years. Conference Managers MP Associates, Inc. continue to be focused on DAC's success. We are grateful for the support of our sponsors, ACM/SIGDA, IEEE/CASS/CANDE/CEDA, and the EDA Consortium.

Enjoy an educational and exciting week at DAC in San Francisco!



Best regards,
Ellen Sentovich
General Chair, 43rd DAC

PROCEEDINGS OF THE 43RD DESIGN AUTOMATION CONFERENCE®

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Table of Contents

General Chair’s Welcome	i
Executive Committee	xxi
Technical Program Committee	xxiii
Panel Sub-Committee	xxv
Tutorial Committee	xxv
Student Design Contest Judges	xxv
Exhibitor Liaison Committee	xxvi
Monday Keynote Address – Joe Costello	xxvii
General Session Keynote Address – Hans Stork	xxviii
Thursday Keynote Address – Alessandro Cremonesi	xxix
Marie R. Pistilli Women in EDA Achievement Award	xxx
P.O. Pistilli Undergraduate Scholarships	xxx
Design Automation Conference Graduate Scholarships	xxx
DAC/ISSCC 2006 Student Design Contest Winners	xxx
ACM Transactions on Design Automation of Electronic Systems	xxxii
ACM/SIGDA Distinguished Service Award	xxxii
2006 Phil Kaufman Award for Distinguished Contributions to EDA	xxxii
IEEE Circuits and Systems Society 2006 Education Award	xxxii
IEEE Circuits and Systems Society 2006 Industrial Pioneer Award	xxxii
IEEE Circuits and Systems Society 2006 Donald O. Pederson Award	xxxii
IEEE Circuits and Systems Society 2006 CSVT Transactions Best Paper Award	xxxiii
IEEE Circuits and Systems Society 2006 VLSI Transactions Best Paper Award	xxxiii
2006 IEEE Fellows	xxxiii
Reviewers	xxxiv
2007 Call for Papers	xxxviii
SESSION 1: PANEL — How Will the Fabless Model Survive?	1
Chair: Don Clark (<i>Wall Street Journal</i>)	
Organizer: Riko Radojic (<i>Qualcomm</i>)	
Panelists: T. Hartung (<i>X-FAB Semiconductor Foundries AG</i>),	
A. Hunter (<i>Samsung Semiconductor Inc.</i>), F. James (<i>Cadence Design Systems</i>),	
M. Bohr (<i>Intel Corp.</i>), B. Paulsen (<i>TSMC NA</i>), N. Yu (<i>Qualcomm</i>)	
SESSION 2: Special Session: Why Doesn’t My System Work?	
Chair: Bart Vermeulen (<i>Philips Research</i>)	
Organizer: Erik Jan Marinissen	
2.1 The Good, the Bad, and the Ugly of Silicon Debug	3
D. Josephson (<i>Intel Corporation</i>)	
2.2 A Reconfigurable Design-for-Debug Infrastructure for SoCs	7
M. Abramovici, P. Bradley, K. Dwarakanath, P. Levin, G. Memmi, D. Miller (<i>DAFCA, Inc.</i>)	
2.3 Visibility Enhancement for Silicon Debug	13
Y.-C. Hsu, F. Tsai, W. Jong, Y.-T. Chang (<i>Novas Software</i>)	

SESSION 3: Hierarchical Synthesis for Mixed-Signal Designs

Chair: Gerd Vandersteen (*IMEC/VUB*)

Organizers: Geert Van Der Plas & Koen Lampaert

- 3.1 A CPPLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time** 19
J. Zou, D. Mueller, H. Graeb, U. Schlichtmann (*Technical University of Meuchen*)
- 3.2 Hierarchical Bottom-up Analog Optimization Methodology Validated by a Delta-Sigma A/D Converter Design for the 802.11a/b/g Standard** 25
T. Eeckelaert, R. Schoofs, G. Gielen, M. Steyaert, W. Sansen (*Katholieke Universiteit Leuven*)
- 3.3 Generation of Yield-Aware Pareto Surfaces for Hierarchical Circuit Design Space Exploration** 31
S. K. Tiwary (*Carnegie Mellon University*), P. K. Tiwary (*BIT Mesra*),
R. A. Rutenbar (*Carnegie Mellon University*)

SESSION 4: Processor and Communication Centric SOC Design

Chair: Johannes Stahl (*CoWare, Inc.*)

Organizers: Brian Bailey & Rainer Leupers

- 4.1 A Real Time Budgeting Method for Module-Level-Pipelined Bus Based System using Bus Scenarios** 37
T. Tanimoto (*Renesas Technology Corporation, Osaka University*),
S. Yamaguchi (*Osaka University, Canon Inc.*), A. Nakata, T. Higashino (*Osaka University*)
- 4.2 Exploiting Forwarding to Improve Data Bandwidth of Instruction-Set Extensions** 43
R. Jayaseelan, H. Liu, T. Mitra (*National University of Singapore*)
- 4.3 Multiprocessor System-on-Chip Data Reuse Analysis for Exploring Customized Memory Hierarchies** 49
I. Issenin (*University of California at Irvine*), E. Brockmeyer, B. Durinck (*IMEC*),
N. Dutt (*University of California at Irvine*)
- 4.4 Prototyping a Fault-Tolerant Multiprocessor SoC with Run-time Fault Recovery** 53
X. Zhu (*Northeastern University*), W. Qin (*Boston University*)

SESSION 5: Practical Applications of DFM

Chair: Nagib Hakim (*Intel Corporation*)

Organizer: Michael Orshansky

- 5.1 Statistical Analysis of SRAM Cell Stability** 57
K. Agarwal, S. Nassif (*IBM Research*)
- 5.2 Criticality Computation in Parameterized Statistical Timing** 63
J. Xiong (*University of California at Los Angeles*), V. Zolotov (*IBM Research*),
N. Venkateswaran (*IBM Systems & Tech. Group*), C. Visweswariah (*IBM Research*)
- 5.3 Mixture Importance Sampling and Its Application to the Analysis of SRAM Designs in the Presence of Rare Failure Events** 69
R. Kanj (*IBM Austin Research Laboratories*), R. Joshi, S. Nassif (*IBM Austin Research Laboratories*)
- 5.4 An Up-stream Design Auto-fix Flow for Manufacturability Enhancement** 73
J. Yang, E. Chohen, C. Tabery, N. Rodriguez, M. Craig (*Advanced Micro Devices*)

SESSION 6: PANEL — DAC Technologist Panel “The IC Nanometer Race — What Will it Take to Win?”

Chair: Walden C. Rhines (*Mentor Graphics*)

Organizer: Laura Parker (*Mentor Graphics*)

Panelists: G. Singer (*Intel Corporation*), P. Magarshack (*STMicroelectronics*),

D. Buss (*Texas Instruments, Inc.*), F.-C. Hsu (*Taiwan Semiconductor Manufacturing Company*),

H.-K. Kang (*Samsung Electronics Co., Ltd.*)

SESSION 7: Special Session: Bridging the System to RTL Verification Gap

Chair: Brian Bailey (*Verification Consultant*)

Organizer: Anmol Mathur

7.1	Use of C/C++ Models for Architecture Exploration and Verification of DSPs	79
	D. Brier, R. S. Mitra (<i>Texas Instruments, Inc.</i>)	
7.2	Maintaining Consistency Between SystemC and RTL System Designs	85
	A. Bruce, A. Nightingale, N. Romdhane (<i>ARM Ltd.</i>), M. M. K. Hashmi, S. Beavis (<i>Spiratech Ltd.</i>), C. Lennard (<i>ARM Ltd.</i>)	
7.3	SystemC Transaction Level Models and RTL Verification	90
	S. Swan (<i>Cadence Design Systems, Inc.</i>)	
7.4	Towards a C++-based Design Methodology Facilitating Sequential Equivalence Checking	93
	P. Georgelin (<i>STMicroelectronics</i>), V. Krishnaswamy (<i>Calypto Design Systems, Inc.</i>)	

SESSION 8: Leakage, Power Analysis and Optimization

Chair: Nam Sung Kim (*Intel Corporation*)

Organizers: Naehyuck Chang & Sanu Mathew

8.1	Charge Recycling in MTCMOS Circuits: Concept and Analysis	97
	E. Pakbaznia (<i>University of Southern California</i>), F. Fallah (<i>Fujitsu Laboratories of America</i>), M. Pedram (<i>University of Southern California</i>)	
8.2	Projection-Based Statistical Analysis of Full-Chip Leakage Power with Non-Log-Normal Distributions	103
	X. Li, J. Le, L. T. Pileggi (<i>Carnegie Mellon University</i>)	
8.3	Physical Design Methodology of Power Gating Circuits for Standard-Cell-Based Design	109
	H.-O. Kim, Y. Shin (<i>KAIST</i>), H. Kim, I. Eo (<i>Electronics and Telecommunications Research Institute</i>)	
8.4	Challenges in Sleep Transistor Design and Implementation in Low-Power Designs	113
	K. Shih (<i>Synopsys Inc.</i>), D. Howard (<i>ARM Ltd.</i>)	
8.5	A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction	117
	L. Cheng, L. Deng, D. Chen, M. D. F. Wong (<i>University of Illinois at Urbana-Champaign</i>)	
8.6	Timing Driven Power Gating	121
	D.-S. Chiou, S.-H. Chen, S.-C. Chang, C. Yeh (<i>National Chung Cheng University</i>)	

SESSION 9: MPSOC Design Methodologies and Applications

Chair: Dan Gajski (*University of California at Irvine*)

Organizers: Peter Marwedel & Tajana Simunic

9.1	A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoring and Analysis: Architectural Design Space Exploration	125
	I. A. Khatib (<i>Royal Institute of Technology</i>), F. Poletti (<i>University of Bologna</i>), D. Bertozzi (<i>University of Ferrara</i>), L. Benini (<i>University of Bologna</i>), M. Bechara, H. Khalifeh (<i>American University of Beirut</i>), A. Jantsch (<i>Royal Institute of Technology</i>), R. Nabiev (<i>Karolinska University</i>)	
9.2	An Automated, Reconfigurable, Low-Power RFID Tag	131
	A. K. Jones, R. R. Hoare, S. R. Dontharaju, S. Tung, R. Sprang, J. Fazekas, J. T. Cain, M. H. Mickle (<i>University of Pittsburgh</i>)	
9.3	Design Space Exploration and Prototyping for On-chip Multimedia Applications	137
	H. G. Lee (<i>Seoul National University</i>), U. Y. Ogras, R. Marculescu (<i>Carnegie Mellon University</i>), N. Chang (<i>Seoul National University</i>)	
9.4	Evaluation and Design Trade-Offs Between Circuit-Switched and Packet-Switched NOCs for Application-Specific SOCs	143
	K.-C. Chang, J.-S. Shen, T.-F. Chen (<i>National Chung Cheng University</i>)	

SESSION 10: Statistical Timing Analysis	
Chair: Chandu Visweswariah (<i>IBM Corporation</i>)	
Organizers: David Blaauw & Hai Zhou	
10.1	Refined Statistical Static Timing Analysis Through Learning Spatial Delay Correlations 149
	B. N. Lee, L.-C. Wang (<i>University of California at Santa Barbara</i>), M. S. Abadir (<i>Freescale Semiconductor, Inc.</i>)
10.2	Statistical Timing Analysis with Correlated Non-Gaussian Parameters using Independent Component Analysis 155
	J. Singh, S. Sapatnekar (<i>University of Minnesota</i>)
10.3	Statistical Timing Based on Incomplete Probabilistic Descriptions of Parameter Uncertainty 161
	W.-S. Wang (<i>University of Texas at Austin</i>), V. Kreinovich (<i>University of Texas at El Paso</i>), M. Orshansky (<i>University of Texas at Austin</i>)
10.4	Probabilistic Interval-Valued Computation: Toward a Practical Surrogate for Statistics Inside CAD Tools 167
	A. Singhee, C. F. Fang, J. D. Ma, R. A. Rutenbar (<i>Carnegie Mellon University</i>)
100	Management Day 100
	Decision-Making for Complex SoCs in Consumer Electronic Products 173
	Chair: Ron Wilson (<i>EDN</i>)
	Organizer: Yervant Zorian (<i>Virage Logic Corporation</i>)
SESSION 11: Panel — Entering the Hot Zone — Can You Handle the Heat and Be Cool? 174	
	Chair: Daya Nadamudi (<i>Gartner Dataquest</i>)
	Organizer: Michelle Clancy (<i>Cayenne Communication</i>)
	Panelists: A. Yang (<i>Apache Design Solutions</i>), R. Chandra (<i>Gradient Design Automation</i>), S. Burke (<i>ATI Technologies</i>), J. A. DeLaCruz (<i>eSilicon Corporation</i>), S. Santhanam (<i>P.A. Semi</i>), U. Ko (<i>Texas Instruments Inc.</i>)
SESSION 12: Special Session: Reliability Challenges for 65nm and Beyond	
Chair: David Yeh (<i>Texas Instruments Inc./SRC</i>)	
Organizers: Joel Phillips & Nagaraj NS	
12.1	Reliability Challenges for 45nm and Beyond 176
	J. W. McPherson (<i>Texas Instruments, Inc.</i>)
12.2	Design Tools for Reliability Analysis 182
	Z. Liu (<i>Cadence Design Systems, Inc.</i>), B. W. McGaughy, J. Z. Ma (<i>Cadence Design Systems, Inc.</i>)
12.3	Design in Reliability for Communication Designs 188
	U. R. Bandi, M. Dasaka, P. K. Kumar (<i>Intel Corporation</i>)
12.4	Practical Aspects of Reliability Analysis for IC Designs 193
	T. Pompl, C. Schlünder, M. Hommel, H. Nielen, J. Schneider (<i>Infineon Technologies</i>)
SESSION 13: Power Grid Analysis and Design	
Chair: Sani R. Nassif (<i>IBM Corporation</i>)	
Organizers: Farid N. Najm & Vikram Jandhyala	
13.1	Power Grid Physics and Implications for CAD 199
	S. Pant (<i>University of Michigan</i>), E. Chiprout (<i>Intel Strategic CAD Labs.</i>)
13.2	Fast Analysis of Structured Power Grid by Triangularization Based Structure Preserving Model Order Reduction 205
	H. Yu, Y. Shi, L. He (<i>University of California at Los Angeles</i>)

13.3	Stochastic Variational Analysis of Large Power Grids Considering Intra-die Correlations	211
	P. Ghanta, S. Vrudhula, S. Bhardwaj (<i>Arizona State University</i>), R. Panda (<i>Freescale Semiconductor, Inc.</i>)	
13.4	A Fast On-Chip Decoupling Capacitance Budgeting Algorithm Using Macromodeling and Linear Programming	217
	M. Zhao, R. Panda, S. Sundareswaran, S. Yan, Y. Fu (<i>Freescale Semiconductor, Inc.</i>)	
SESSION 14: Advances in Formal Solvers		
	Chair: Jeremy Levitt (<i>Mentor Graphics Corporation</i>)	
	Organizers: Alan Hu & Anmol Mathur	
14.1	Distributed Dynamic BDD Reordering	223
	Z. Nevo (<i>IBM Haifa Research Labs</i>), M. Farkash (<i>IBM Systems Group</i>)	
14.2	SAT Sweeping with Local Observability Don't-Cares	229
	Q. Zhu, N. Kitchen (<i>University of California at Berkeley</i>), A. Kuehlmann (<i>University of California at Berkeley, Cadence Berkeley Labs.</i>), A. Sangiovanni-Vincentelli (<i>University of California at Berkeley</i>)	
14.3	Predicate Learning and Selective Theory Deduction for a Difference Logic Solver	235
	C. Wang, A. Gupta, M. Ganai (<i>NEC Laboratories America</i>)	
14.4	Fast Illegal State Identification for Improving SAT-Based Induction	241
	V. C. Vimjam, M. S. Hsiao (<i>Virginia Tech.</i>)	
SESSION 15: Gate Modeling and Model Order Reduction		
	Chair: Peter Feldmann (<i>IBM Corporation</i>)	
	Organizers: Charlie Chung-Ping Chen & Joel Phillips	
15.1	A Multi-port Current Source Model for Multiple-Input Switching Effects in CMOS Library Cells	247
	C. Amin, C. Kashyap, N. Menezes, K. Killpack, E. Chiprout (<i>Intel Corporation</i>)	
15.2	Statistical Logic Cell Delay Analysis Using a Current-based Model	253
	H. Fatemi, S. Nazarian, M. Pedram (<i>University of Southern California</i>)	
15.3	Multi-Shift Quadratic Alternating Direction Implicit Iteration for High-Speed Positive-Real Balanced Truncation	257
	N. Wong (<i>The University of Hong Kong</i>), V. Balakrishnan (<i>Purdue University</i>)	
15.4	A Fast Passivity Test for Descriptor Systems Via Structure-Preserving Transformations of Skew-Hamiltonian/Hamiltonian Matrix Pencils	261
	N. Wong, C. K. Chu (<i>The University of Hong Kong</i>)	
15.5	Model Order Reduction of Linear Networks with Massive Ports via Frequency-Dependent Port Packing	267
	P. Li, W. Shi (<i>Texas A&M University</i>)	
150	Management Day SESSION 150	
	Tradeoffs and Choices for Emerging SoCs in High-End Applications	273
	Chair: Nic Mokhoff (<i>EE Times</i>)	
	Organizer: Yervant Zorian (<i>Virage Logic Corporation</i>)	
SESSION 16: Special Session: MPSOC Design Tools		
	Chair: Pierre Paulin (<i>STMicroelectronics</i>)	
	Organizer: Sumit Gupta	
16.1	Overview of the MPSoC Design Challenge	274
	G. Martin (<i>Tensilica, Inc.</i>)	
16.2	Programming Models and HW-SW Interfaces Abstraction for Multi-Processor SoC	280
	A. A. Jerraya, A. Bouchhima, F. Pétrot (<i>TIMA Laboratory</i>)	
16.3	System-Level Exploration Tools for MPSoC Designs	286
	P. Flake, S. Davidmann, F. Schirrmeyer (<i>Imperas, Inc.</i>)	

SESSION 17: Special Session — Highlights of ISSCC: Multimedia

Chair: Wanda Gass (*Texas Instruments Inc.*)

Organizers: Andrew B. Kahng & Ingrid Verbauwhede

- 17.1 Design of a 125 μ W, Fully-Scalable MPEG-2 and H.264/AVC Video Decoder for Mobile Applications**288
T.-M. Liu, C.-C. Chung, C.-Y. Lee (*National Chiao-Tung University*),
T.-A. Lin, S.-Z. Wang (*MediaTek Inc.*)
- 17.3 A CMOS SoC for 56/18/16 CD/DVD-dual/RAM Applications**290
J.-S. Pan, H.-C. Chen, B.-Y. Hsieh, H.-C. Chen, R. Lee, C.-H. Chu, Y.-C. Liu, C. Liu, L. Huang,
C.-L. Wu, M.-H. Lin, C.-Y. Lin, S.-N. Tsai, J.-N. Yang, C.-P. Ma, Y. Cheng, S.-H. Chou,
H.-C. Peng, P.-C. Huang, B. Chiu, A. Ho (*MediaTek Inc.*)
- 17.4 Hierarchical Power Distribution and Power Management Scheme for a Single Chip Mobile Processor**292
T. Hittori, T. Irita, M. Ito, E. Yamamoto, H. Kato, G. Sado, T. Yamada, K. Nishiyama,
H. Yagi, T. Koike, Y. Tsuchihashi, M. Higashida, H. Asano, I. Hayashibara, K. Tatezawa,
Y. Shimazaki, N. Morino, Y. Yasu, T. Hoshi, Y. Miyairi, K. Yanagisawa, K. Hirose,
S. Tamaki, S. Yoshioka (*Renesas Technology Corporation*), T. Ishii (*Hitachi ULSI Systems*),
Y. Kanno, H. Mizuno, T. Yamada, N. Irie (*Hitachi, Ltd.*),
R. Tsuchihashi, N. Arai, T. Akiyama, K. Ohno (*NTT DoCoMo, Inc.*)

SESSION 18: Buffer Insertion

Chair: Charles J. Alpert (*IBM Corporation*)

Organizers: Dirk Stroobandt & Louis Scheffer

- 18.1 Buffer Insertion in Large Circuits with Constructive Solution Search Techniques** ...296
M. Waghmode, Z. Li, W. Shi (*Texas A&M University*)
- 18.2 Low-Power Repeater Insertion With Both Delay and Slew Rate Constraints**302
Y. Peng, X. Liu (*North Carolina State University*)
- 18.3 Fast Algorithms For Slew Constrained Minimum Cost Buffering**308
S. Hu (*Texas A&M University*), C. J. Alpert (*IBM Austin Research Laboratories*),
J. Hu (*Texas A&M University*), S. Karandikar (*IBM Austin Research Laboratories*),
Z. Li, W. Shi (*Texas A&M University*), C. N. Sze (*IBM Austin Research Laboratories*)

SESSION 19: Testing and Validation for Timing Defects

Chair: Cecilia Metra (*University of Bologna*)

Organizers: Erik Jan Marinissen & Gordon Roberts

- 19.1 A Flexible and Scalable Methodology for GHz-Speed Structural Test**.....314
V. Iyengar, G. Grise, M. Taylor, B. Bassett, R. Farmer (*IBM Microelectronics*)
- 19.2 Timing-Based Delay Test for Screening Small Delay Defects**320
N. Ahmed, M. Tehranipoor (*University of Maryland*), V. Jayaram (*Texas Instruments, Inc.*)
- 19.3 Hold Time Validation on Silicon and the Relevance of Hazards in Timing Analysis**326
A. Majumdar, W.-Y. Chen (*Stratosphere Solutions, Inc.*), J. Guo (*Sun Microsystems, Inc.*)

SESSION 20: Advanced Topics in Processor and System Verification

Chair: Jon Michelson (*Cisco Systems, Inc.*)

Organizers: Avi Ziv & Harry Foster

- 20.1 Practical Methods in Coverage-Oriented Verification of the Merom Microprocessor**.....332
A. Gluska (*Intel MG*)
- 20.2 Verification of the Cell Broadband Engine™ Processor**.....338
K. Shimizu, S. Gupta (*IBM Corporation*), T. Koyama (*Sony Computer Entertainment Inc.*),
T. Omizo (*Toshiba Corporation*), J. Abdulhafiz, L. McConville, T. Swanson (*IBM Corporation*)
- 20.3 Shielding Against Design Flaws with Field Repairable Control Logic**.....344
I. Wagner, V. Bertacco, T. Austin (*The University of Michigan*)
- 20.4 Scheduling-based Test-case Generation for Verification of Multimedia SoCs**348
A. Nahir, A. Ziv (*IBM Research*), R. Emek (*Yahoo! Inc.*), T. Keidar, N. Ronen (*Zoran Microelectronics Ltd.*)

SESSION 21: Software for Real-Time Applications

Chair: Mahmut Kandemir (*Pennsylvania State University*)

Organizers: Lothar Thiele & Vincent Mooney

- 21.1 Rapid and Low-Cost Context-Switch through Embedded Processor Customization for Real-Time and Control Applications** 352
X. Zhou, P. Petrov (*University of Maryland*)
- 21.2 Efficient Detection and Exploitation of Infeasible Paths for Software Timing Analysis** 358
V. Suhendra, T. Mitra, A. Roychoudhury, T. Chen (*National University of Singapore*)
- 21.3 Leakage-Aware Intraprogram Voltage Scaling for Embedded Processors** 364
P.-K. Huang, S. Ghiasi (*University of California at Davis*)

SESSION 22: Panel — Building a Standard ESL Design and Verification Methodology: Is It Just a Dream? 370

Chair: Gary Smith (*Gartner-DataQuest*)

Organizer: Francine Bacchini (*Francine Bacchini, Inc.*)

Panelists: A. Hosseini (*Cisco Systems*), A. Parikh (*Pixelworks, Inc.*), H. T. Chin (*HD Lab, Inc.*),

P. Urard (*STMicroelectronics*), E. Girczyc (*Summit Design, Inc.*),

S. Bloch (*Mentor Graphics Corporation*)

SESSION 23: Invited Session

CAD Challenges for Leading-Edge Multimedia Designs 372

Chair: Andrew B. Kahng (*University of California at San Diego*)

Organizer: Andrew B. Kahng

SESSION 24: Routing

Chair: Dinesh Gaitonde (*Xilinx, Inc.*)

Organizers: Patrick Groeneveld & Phiroze Parakh

- 24.1 BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP** ... 373
M. Cho, D. Z. Pan (*University of Texas at Austin*)
- 24.2 Steiner Network Construction for Timing Critical Nets** 379
S. Hu, Q. Li, J. Hu, P. Li (*Texas A&M University*)
- 24.3 Circuit Simulation Based Obstacle-Aware Steiner Routing** 385
Y. Shi, P. Mesa, H. Yu, L. He (*University of California at Los Angeles*)
- 24.4 Timing-Driven Steiner Trees are (Practically) Free** 389
C. J. Alpert (*IBM Austin Research Laboratories*), A. B. Kahng (*University of California at San Diego*),
C. N. Sze (*IBM Austin Research Laboratories*), Q. Wang (*University of California at San Diego*)

SESSION 25: The Test Bin

Chair: Roni Khazaka (*McGill University*)

Organizers: Cecilia Metra & Erik Jan Marinissen

- 25.1 Systematic Software-Based Self-Test for Pipelined Processors** 393
M. Psarakis, D. Z. Gizopoulos, M. Hatzimihail (*University of Piraeus*),
A. Paschalis (*University of Athens*), A. Raghunathan, S. Ravi (*NEC Laboratories America*)
- 25.2 A Test Pattern Ordering Algorithm for Diagnosis with Truncated Fail Data** 399
G. Chen (*Mentor Graphics Corporation*), S. M. Reddy (*University of Iowa*),
I. Pomeranz (*Purdue University*), J. Rajski (*Mentor Graphics Corporation*)
- 25.3 DFT for Controlled-Impedance I/O Buffers** 405
A. A. Al-Yamani (*King Fahd University of Petroleum and Minerals*)

SESSION 26: Panel: Variation-Aware Analysis: Savior of the Nanometer Era? 411

Chair: William H. Joyner, Jr. (*IBM Corp./SRC*)

Organizer: Shishpal Rawat (*Intel Corporation*)

Panelists: S. R. Nassif (*IBM*), V. Pitchumani (*Intel Corporation*), N. Rodriguez (*AMD*),

D. Sylvester (*University of Michigan*), C. Bittlestone (*Texas Instruments Inc.*),

R. Radojic (*Qualcomm CDMA Technologies*)

SESSION 27: Low Power and Ultra-low Voltage Design

Chair: Chris Kim (*University of Minnesota*)

Organizers: Diana Marculescu & Trevor Mudge

- 27.1 A Fully Physical Model for Leakage Distribution under Process Variations in Nanoscale Double-Gate CMOS** 413
H. Ananthan, K. Roy (*Purdue University*)
- 27.2 A PLA Based Asynchronous Micropipelining Approach for Subthreshold Circuit Design** 419
N. Jayakumar, R. Garg (*Texas A&M University*), B. Gamache (*Conexant Systems, Inc.*),
S. P. Khatri (*Texas A&M University*)
- 27.3 Subthreshold Logical Effort: A Systematic Framework for Optimal Subthreshold Device Sizing** 425
J. Keane, H. Eom, T.-H. Kim, S. Sapatnekar, C. Kim (*University of Minnesota*)
- 27.4 Timing-Constrained and Voltage-Island-Aware Voltage Assignment** 429
H. Wu (*Cadence Design Systems, Inc.*), M. D. F. Wong (*University of Illinois at Urbana-Champaign*),
I.-M. Liu (*Atoptech, Inc.*)

SESSION 28: High-Level Exploration and Optimization

Chair: Rishiyur S. Nikhil (*Bluespec, Inc.*)

Organizers: Reinaldo Bergamaschi & Rishiyur S. Nikhil

- 28.1 An Efficient and Versatile Scheduling Algorithm Based On SDC Formulation**..... 433
J. Cong, Z. Zhang (*University of California at Los Angeles*)
- 28.2 Register Binding for Clock Period Minimization** 439
S.-H. Huang, C.-H. Cheng, Y.-T. Nieh, W.-C. Yu (*Chung Yuan Christian University*)
- 28.3 Towards the Automatic Exploration of Arithmetic-Circuit Architectures** 445
A. K. Verma, P. lenne (*Ecole Polytechnique Fédérale de Lausanne*)
- 28.4 Design Space Exploration using Time and Resource Duality with the Ant Colony Optimization** 451
G. Wang, W. Gong, B. DeRenzi, R. Kastner (*University of California at Santa Barbara*)
- 28.5 Rapid Estimation of Control Delay from High-Level Specifications** 455
G. R. Gupta (*University of Wisconsin*),
M. Gupta (*Purdue University*), P. R. Panda (*Indian Institute of Technology*)

SESSION 29: Panel — Design Challenges for Next-Generation Multimedia, Game and Entertainment Platforms

..... 459

Chair: Bryan Lewis (*Gartner DataQuest*)

Organizer: Andrew B. Kahng (*University of California at San Diego*)

Panelists: J. Cohn (*IBM Corporation*), J.-T. Kong (*Samsung Electronics Co., Ltd.*),

C. Malachowsky (*NVIDIA Corporation*), R. Tobias (*Pixelworks, Inc.*), B. Traw (*Intel Corporation*)

SESSION 30: CAD for FPGAS

Chair: William N. N. Hung (*Synplicity, Inc.*)

Organizers: Bill Halpin & Steven Teig

- 30.1 Architecture-Aware FPGA Placement using Metric Embedding**..... 460
P. Gopalakrishnan, X. Li, L. Pileggi (*Carnegie Mellon University*)
- 30.2 Efficient SAT-based Boolean Matching for FPGA Technology Mapping** 466
S. Safarpour, A. Veneris (*University of Toronto*), G. Baeckler, R. Yuan (*Altera Corporation*)
- 30.3 Optimal Simultaneous Mapping and Clustering for FPGA Delay Optimization** 472
J. Y. Lin (*Magma Design Automation*), D. Chen (*University of Illinois at Urbana-Champaign*),
J. Cong (*University of California at Los Angeles*)
- 30.4 Simultaneous Time Slack Budgeting and Retiming for Dual-Vdd FPGA Power Reduction** 478
Y. Hu, Y. Lin (*University of California at Los Angeles*), T. Tuan (*Xilinx Research Laboratories*)

SESSION 31: Secure Systems

Chair: Catherine Gebotys (*University of Waterloo*)

Organizers: Pai Chou & Peter Marwedel

- 31.1 VIRTUS: A New Processor Virtualization Architecture for Security-Oriented Next-Generation Mobile Terminals** 484
H. Inoue (*NEC Corporation*), A. Ikeno, M. Kondo (*NEC Informatec Systems, Ltd.*),
J. Sakai, M. Edahiro (*NEC Corporation*)
- 31.2 A Network Security Processor Design Based on an Integrated SOC Design and Test Platform** 490
C.-H. Wang, C.-Y. Lo, M.-S. Lee, J.-C. Yeh, C.-T. Huang,
C.-W. Wu, S.-Y. Huang (*National Tsing-Hua University*)
- 31.3 Software Architecture Exploration for High-Performance Security Processing on a Multiprocessor Mobile SoC** 496
D. Arora (*Princeton University*), A. Raghunathan, S. Ravi, M. Sankaradass (*NEC Laboratories America*),
N. K. Jha (*Princeton University*), S. T. Chakradhar (*NEC Laboratories America*)
- 31.4 IMPRES: Integrated Monitoring for Processor RELiability and Security** 502
R. G. Ragel, S. Parameswaran (*The University of New South Wales & National Information*)
- 31.5 A Parallelized Way to Provide Data Encryption and Integrity Checking on a Processor-Memory Bus** 506
R. Elbaz (*University of Montpellier & STMicroelectronics*),
L. Torres, G. Sassatelli (*University of Montpellier*),
P. Guillemain, M. Bardouillet, A. Martinez (*STMicroelectronics*)

SESSION 32: Logic Synthesis I

Chair: Davide Pandini (*STMicroelectronics*)

Organizers: James Hoe & Rajeev Murgai

- 32.1 Symmetry Detection for Large Boolean Functions using Circuit Representation, Simulation, and Satisfiability** 510
J. S. Zhang (*Portland State University*), A. Mishchenko, R. Brayton (*University of California at Berkeley*),
M. Chrzanowska-Jeske (*Portland State University*)
- 32.2 Exploiting K-Distance Signature for Boolean Matching and G-Symmetry Detection** 516
K.-H. Wang (*Fu Jen Catholic University*)
- 32.3 Gain-Based Technology Mapping for Minimum Runtime Leakage under Input Vector Uncertainty** 522
A. K. Singh, M. Mani (*University of Texas at Austin*), R. Puri (*IBM T.J. Watson Research Center*),
M. Orshansky (*University of Texas at Austin*)
- 32.4 Gate Sizing: FinFETs vs 32nm Bulk MOSFETs** 528
B. Swahn, S. Hassoun (*Tufts University*)
- 32.5 DAG-Aware AIG Rewriting-A-Fresh Look at Combinational Logic Synthesis** 532
A. Mishchenko, S. Chatterjee, R. Brayton (*University of California at Berkeley*)

SESSION 33: Low-Power, Thermal-Aware Architectures

Chair: Kevin Skadron (*University of Virginia*)

Organizers: Diana Marculescu & Naehyuck Chang

- 33.1 Energy-Scalable OFDM Transmitter Design and Control** 536
B. Debaille (*IMEC*), B. Bougard (*IMEC & KU Leuven*), G. Lenoir (*IMEC*),
G. Vandersteen (*IMEC & VUB*), F. Catthoor (*IMEC & KU Leuven*)
- 33.2 Systematic Temperature Sensor Allocation and Placement for Microprocessors** 542
R. Mukherjee, S. O. Memik (*Northwestern University*)
- 33.3 HybDTM: A Coordinated Hardware-Software Approach for Dynamic Thermal Management** 548
A. Kumar (*Princeton University*), L. Shang (*Queen's University*),
L.-S. Peh, N. K. Jha (*Princeton University*)

33.4	A Systematic Method For Functional Unit Power Estimation in Microprocessors	554
	W. Wu, L. Jin, J. Yang, P. Liu, S. X.-D. Tan (<i>University of California at Riverside</i>)	
33.5	Low-Power Architectural Trade-Offs in a VLSI Implementation of an Adaptive Hearing Aid Algorithm	558
	F. Buergin, F. Carbognani, M. Hediger, H. Meier, R. Meyer-Piening, R. Santschi, H. Kaeslin, N. Felber, W. Fichtner (<i>ETH Zurich</i>)	
SESSION 34: Low Power System Level Design		
	Chair: Massoud Pedram (<i>University of Southern California</i>)	
	Organizers: Diana Marculescu & Sanu Mathew	
34.1	Extending the Lifetime of Fuel Cell Based Hybrid Systems	562
	J. Zhuo, C. Chakrabarti (<i>Arizona State University</i>), N. Chang (<i>Seoul National University</i>), S. Vrudhula (<i>Arizona State University</i>)	
34.2	High-Level Power Management of Embedded Systems with Application-Specific Energy Cost Functions	568
	Y. Cho, N. Chang (<i>Seoul National University</i>), C. Chakrabarti, S. Vrudhula (<i>Arizona State University</i>)	
34.3	Communication Latency Aware Low Power NoC Synthesis	574
	Y. Hu, Y. Zhu (<i>University of California at San Diego</i>), H. Chen (<i>Synopsys Inc.</i>), R. Graham, C.-K. Cheng (<i>University of California at San Diego</i>)	
34.4	Optimality Study of Resource Binding with Multi-Vdds	580
	D. Chen (<i>University of Illinois at Urbana-Champaign</i>), J. Cong, Y. Fan (<i>University of California at Los Angeles</i>), J. Xu (<i>Peking University</i>)	
SESSION 35: Power-Constrained Design for Multimedia		
	Chair: Richard Tobias (<i>PixelWorks, Inc.</i>)	
	Organizers: Andrew B. Kahng & John Cohn	
35.1	SMERT: Energy-Efficient Design of a Multimedia Messaging System for Mobile Devices	586
	L. Zhong (<i>Rice University</i>), B. Wei (<i>AT&T Labs-Research</i>), M. J. Sinclair (<i>Microsoft Research</i>)	
35.2	Signature-Based Workload Estimation for Mobile 3D Graphics	592
	B. C. Mochocki (<i>University of Notre Dame & NEC Laboratories America</i>), K. Lahiri, S. Cadambi (<i>NEC Laboratories America</i>), X. S. Hu (<i>University of Notre Dame</i>)	
35.3	Games Are Up for DVFS	598
	Y. Gu, S. Chakraborty, W. T. Ooi (<i>National University of Singapore</i>)	
35.4	Backlight Dimming in Power-Aware Mobile Displays	604
	A. Iranli, W. Lee, M. Pedram (<i>University of Southern California</i>)	
35.5	Minimization for LED-backlit TFT-LCDs	608
	W.-C. Cheng, C.-F. Chao (<i>National Chiao-Tung University</i>)	
SESSION 36: Electrical and Thermal Issues in FPGAS		
	Chair: Rajeev Jayaraman (<i>Xilinx, Inc.</i>)	
	Organizers: Patrick Lysaght & Ryan Kastner	
36.1	Leakage Power Reduction of Embedded Memories on FPGAs Through Location Assignment	612
	Y. Meng, T. Sherwood, R. Kastner (<i>University of California at Santa Barbara</i>)	
36.2	A Fast HW/SW FPGA-Based Thermal Emulation Framework for Multi-Processor System-on-Chip	618
	D. Aienza (<i>Complutense University of Madrid, Ecole Polytechnique Federale de Lausanne</i>), P. G. Del Valle, G. Paci (<i>Complutense University of Madrid</i>), F. Poletti, L. Benini (<i>University of Bologna</i>), G. De Micheli (<i>LSI, Ecole Polytechnique Federale de Lausanne</i>), J. M. Mendias (<i>DACYA, Complutense University of Madrid</i>)	

36.3	An Adaptive FPGA Architecture with Process Variation Compensation and Reduced Leakage	624
	G. Nabaa (<i>Actel</i>), N. Azizi, F. N. Najm (<i>University of Toronto</i>)	
36.4	FLAW: FPGA Lifetime Awareness	630
	S. Srinivasan, P. Mangalagiri, Y. Xie, N. Vijaykrishnan, K. Sarpatwari (<i>Pennsylvania State University</i>)	
SESSION 37: Special Session: Beyond Low-Power Design:		
Environmental Energy Harvesting		
Chair: Kaushik Roy (<i>Purdue University</i>)		
Organizers: Pai Chou & Vijay Raghunathan		
37.1	Solution-Processed Infrared Photovoltaic Devices	636
	D. D. MacNeil, E. H. Sargent (<i>University of Toronto</i>)	
37.2	Circuits for Energy Harvesting Sensor Signal Processing	639
	R. Amirtharajah, J. Wenck (<i>University of California at Davis</i>), J. Collier (<i>Boston Scientific</i>), J. Siebert, B. Zhou (<i>Intel Corporation</i>)	
37.3	Systems for Human-Powered Mobile Computing	645
	J. A. Paradiso (<i>Massachusetts Institute of Technology</i>)	
37.4	Harvesting Aware Power Management for Sensor Networks	651
	A. Kansal, J. Hsu, M. Srivastava (<i>University of California at Los Angeles</i>), V. Raghunathan (<i>NEC Labs America</i>)	
SESSION 38: Communication-Driven Synthesis		
Chair: Luca Carloni (<i>Columbia University</i>)		
Organizer: Stephen Edwards		
38.1	Synthesis of Synchronous Elastic Architectures	657
	J. Cortadella (<i>Universitat Politècnica de Catalunya</i>), M. Kishinevsky, B. Grundmann (<i>Intel Corporation</i>)	
38.2	Statistical On-Chip Communication Bus Synthesis and Voltage Scaling Under Timing Yield Constraint	663
	S. Pandey, M. Glesner (<i>Darmstadt University</i>)	
38.3	Optimization of Area under a Delay Constraint in Digital Filter Synthesis Using SAT-Based Integer Linear Programming	669
	L. Aksoy (<i>Istanbul Technical University</i>), E. Costa (<i>Universidade Catolica de Pelotas</i>), P. Flores, J. Monteiro (<i>INESC-ID/IST</i>)	
38.4	Behavior and Communication Co-Optimization for Systems with Sequential Communication Media	675
	J. Cong, Y. Fan, G. Han, W. Jiang, Z. Zhang (<i>University of California at Los Angeles</i>)	
38.5	Synthesis of High-Performance Packet Processing Pipelines	679
	C. Soviani (<i>Columbia University</i>), I. Hadžić (<i>Bell Laboratories</i>), S. A. Edwards (<i>Columbia University</i>)	
SESSION 39: Parallelism and Memory Optimizations		
Chair: Steven Tjiang (<i>Google</i>)		
Organizers: Steven Tjiang & Vincent Mooney		
39.1	Optimizing Code Parallelization through a Constraint Network Based Approach	683
	O. Ozturk, G. Chen, M. Kandemir (<i>Pennsylvania State University</i>)	
39.2	Buffer Memory Optimization for Video Codec Application Modeled in Simulink	689
	S.-I. Han (<i>Seoul National University, TIMA Laboratory</i>), X. Guerin (<i>TIMA Laboratory</i>), S.-I. Chae (<i>Seoul National University</i>), A. A. Jerraya (<i>TIMA Laboratory</i>)	
39.3	Configurable Cache Subsetting for Fast Cache Tuning	695
	P. Viana (<i>Federal University of Pernambuco</i>), A. Gordon-Ross, E. Keogh (<i>University of California at Riverside</i>), E. Barros (<i>Federal University of Pernambuco</i>), F. Vahid (<i>University of California at Riverside</i>)	

39.4	High-Performance Operating System Controlled Memory Compression	701
	L. Yang (<i>Northwestern University</i>), H. Lekatsas (<i>NEC Laboratories America</i>), R. P. Dick (<i>Northwestern University</i>)	
39.5	A Cost-Effective Implementation of an ECC-protected Instruction Queue for Out-of-Order Microprocessors	705
	V. Stojanovic, R. I. Bahar, J. Dworak (<i>Brown University</i>), R. Weiss (<i>Evergreen State College</i>)	
SESSION 40: Panel — Tomorrow’s Analog: Just Dead or Just Different?		709
	Chair: Georges Gielen (<i>Katholieke University</i>) Organizer: Rob A. Rutenbar (<i>Carnegie Mellon University</i>) Panelists: S. Borkar (<i>Intel Corporation</i>), R. Brodersen (<i>University of California at Berkeley</i>), J.-H. Chern (<i>Mentor Graphics Corporation</i>), E. Naviasky (<i>Cadence Design Services</i>), D. Saias (<i>STMicroelectronics</i>), C. Sodini (<i>Massachusetts Institute of Technology</i>)	
SESSION 41: Nanotubes and Nanowires		
	Chair: Sankar Basu (<i>National Science Foundation</i>) Organizers: Igor Markov & Krishnendu Chakrabarty	
41.1	NATURE: A Hybrid Nanotube/CMOS Dynamically Reconfigurable Architecture	711
	W. Zhang, N. K. Jha (<i>Princeton University</i>), L. Shang (<i>Queen’s University</i>)	
41.2	Modeling and Analysis of Circuit Performance of Ballistic CNFET	717
	B. C. Paul (<i>Stanford University & Toshiba America Research Inc.</i>), S. Fujita, M. Okajima (<i>Toshiba America Research Inc.</i>), T. Lee (<i>Stanford University</i>)	
41.3	Topology Aware Mapping of Logic Functions onto Nanowire-based Crossbar Architectures	723
	W. T. Rao, A. Orailoglu (<i>University of California at San Diego</i>), R. Karri (<i>Polytechnic University</i>)	
41.4	A New Hybrid FPGA with Nanoscale Clusters and CMOS Routing	727
	R. M. P. Rad, M. Tehranipoor (<i>University of Maryland</i>)	
SESSION 42: Simulation Assisted Formal Verification		
	Chair: Andrew Piziali (<i>Cadence Design Systems, Inc.</i>) Organizers: Harry Foster & Richard Ho	
42.1	Directed-Simulation Assisted Formal Verification of Serial Protocol and Bridge	731
	S. Gorai (<i>Mentor Graphics</i>), S. Biswas, L. Bhatia, P. Tiwari, R. S. Mitra (<i>Texas Instruments, Inc.</i>)	
42.2	Guiding Simulation with Increasingly Refined Abstract Traces	737
	K. Nanshi, F. Somenzi (<i>University of Colorado at Boulder</i>)	
42.3	Mining Global Constraints for Improving Bounded Sequential Equivalence Checking	743
	W. Wu, M. S. Hsiao (<i>Virginia Tech</i>)	
SESSION 43: Yield Analysis and Improvement		
	Chair: Evanthia Papadopoulou (<i>IBM Corporation</i>) Organizers: Fook-Luen Heng & Patrick Groeneveld	
43.1	An IC Manufacturing Yield Model Considering Intra-Die Variations	749
	J. Luo, S. Sinha, Q. Su, J. Kawa, C. Chiang (<i>Synopsys Inc.</i>)	
43.2	Novel Full-Chip Gridless Routing Considering Double-Via Insertion	755
	H.-Y. Chen, M.-F. Chiang, Y.-W. Chang (<i>National Taiwan University</i>), L. Chen, B. Han (<i>United Microelectronics Corporation</i>)	
43.3	Optimal Jumper Insertion for Antenna Avoidance under Ratio Upper-Bound	761
	J. Wang, H. Zhou (<i>Northwestern University</i>)	

SESSION 44: Approaches to Soft Error Mitigation

Chair: Subashish Mitra (*Stanford University*)

Organizers: Dennis Sylvester & Haihua Su

- 44.1 MARS-C: Modeling and Reduction of Soft Errors in Combinational Circuits** 767
N. Miskov-Zivanov, D. Marculescu (*Carnegie Mellon University*)
- 44.2 A Design Approach for Radiation-hard Digital Electronics** 773
R. Garg, N. Jayakumar, S. P. Khatri, G. Choi (*Texas A&M University*)
- 44.3 A Family of Cells to Reduce the Soft-Error-Rate in Ternary-CAM** 779
N. Azizi, F. N. Najm (*University of Toronto*)

SESSION 45: Design/Technology Interaction

Chair: Jerry D. Hayes (*IBM Corporation*)

Organizer: Sani Nassif

- 45.1 Process Variation Aware OPC with Variational Lithography Modeling** 785
P. Yu, S. X. Shi, D. Z. Pan (*University of Texas at Austin*)
- 45.2 Modeling of Intra-die Process Variations for Accurate Analysis and Optimization of Nano-scale Circuits** 791
S. Bhardwaj, S. Vrudhula, P. Ghanta, Y. Cao (*Arizona State University*)
- 45.3 Computation of Accurate Interconnect Process Parameter Values for Performance Corners under Process Variations** 797
F. Huebbers (*Northwestern University*), A. Dasdan (*Yahoo!*), Y. Ismail (*Northwestern University*)
- 45.4 Standard Cell Characterization Considering Lithography Induced Variations** 801
K. Cao, S. Dobre (*Qualcomm, Inc.*), J. Hu (*Texas A&M University*)

SESSION 46: Panel —Building a Verification Test Plan:

Trading Brute Force for Finesse 805

Chair: Sharad Malik (*Princeton University*)

Organizer: Francine Bacchini (*Francine Bacchini, Inc.*)

Panelists: J. Bergeron (*Synopsys Inc.*), H. Foster (*Mentor Graphics*),
A. Piziali (*Cadence Design Systems*), R. S. Mitra (*Texas Instruments, Inc.*),
C. Ahlschlager (*Sun Microsystems*), D. Stein (*Cisco Systems, Inc.*)

SESSION 47: Special Session: More Moore's Law and More Than Moore's Law

Chair: Igor L. Markov (*University of Michigan*)

Organizers: Krishnendu Chakrabarty & Niraj Jha

- 47.1 Electronics Beyond Nano-scale CMOS** 807
S. Borkar (*Intel Corporation*)
- 47.2 Are Carbon Nanotubes the Future of VLSI Interconnections?** 809
K. Banerjee, N. Srivastava (*University of California at Santa Barbara*)
- 47.3 The Zen of Nonvolatile Memories** 815
E. J. Prinz (*Freescale Semiconductor, Inc.*)

SESSION 48: Formal Specification and Verification Testbench Generation

Chair: Michael Theobald (*D.E. Shaw Research*)

Organizers: Alan Hu & Erich Marschner

- 48.1 Formal Analysis of Hardware Requirements** 821
I. Pill (*Graz University of Technology*), S. Semprini, R. Cavada, M. Roveri (*ITC-irst*),
R. Bloem (*Graz University of Technology*), A. Cimatti (*ITC-irst*)
- 48.3 Test Generation Games from Formal Specifications** 827
A. Banerjee, B. Pal, S. Das, A. Kumar, P. Dasgupta (*Indian Institute of Technology*)

SESSION 49: Analysis and Optimization Issues in NoC Design

Chair: Petru Eles (*Linköping University*)

Organizers: Joerg Henkel & Radu Marculescu

- 49.1 Optimal Link Scheduling on Improving Best-Effort and Guaranteed Services Performance in Network-on-Chip Systems** 833
L.-F. Leung (*Hong Kong University of Science and Technology*), C.-Y. Tsui (*Hong Kong University*)
- 49.2 Prediction-based Flow Control for Network-on-Chip Traffic** 839
U. Y. Ogras, R. Marculescu (*Carnegie Mellon University*)
- 49.3 A Multi-Path Routing Strategy with Guaranteed In-Order Packet Delivery and Fault-Tolerance for Networks on Chip** 845
S. Murali (*Stanford University*), D. Atienza (*Complutense University of Madrid*),
L. Benini (*University of Bologna*), G. De Micheli (*LSI, Ecole Polytechnique Federale de Lausanne*)
- 49.4 DyXY - A Proximity Congestion-Aware Deadlock-Free Dynamic Routing Method for Network on Chip** 849
M. Li, Q.-A. Zeng, W.-B. Jone (*University of Cincinnati*)

SESSION 50: Special Session: Key Technologies for Beyond the Die

Chair: Mike Heimlich (*Applied Wave Research*)

Organizer: Lei He

- 50.1 The Importance of Adopting a Package-Aware Chip Design Flow** 853
K. Sheth, E. Sarto, J. McGrath (*Rio Design Automation*)
- 50.2 Silicon Carrier for Computer Systems** 857
C. S. Patel (*IBM T.J. Watson Research Center*)
- 50.3 4.25 Gb/s Laser Driver: Design Challenges and EDA Tool Limitations** 863
B. Sheahan (*Stanford University*), J. W. Fattaruso, J. Wong, K. Muth (*Texas Instruments*),
B. Murmann (*Stanford University*)
- 50.4 Power-Centric Design of High-Speed I/Os** 867
H. Hatamkhani (*University of California at Los Angeles*), F. Lambrecht (*Rambus Inc.*),
V. Stojanovic (*Massachusetts Institute of Technology*),
C.-K. K. Yang (*University of California at Los Angeles*)

SESSION 51: Analog Design and Design Assistance

Chair: Peng Li (*Texas A&M University*)

Organizers: Helmut Graeb & Rob A. Rutenbar

- 51.1 A 10.6mw/0.8pJ Power-Scalable 1GS/s 4b ADC in 0.18 μ m CMOS with 5.8GHz ERBW** 873
P. Nuzzo (*University of Pisa, IMEC*), G. Van der Plas (*IMEC, DESICS/Wireless*),
F. De Bernardinis, L. Van der Perre (*University of Pisa*),
B. Gyselinckx (*IMEC, WATS*), P. Terreni (*University of Pisa*)
- 51.2 SOC-NLNA: Synthesis and Optimization for Fully Integrated Narrow-Band CMOS Low Noise Amplifiers** 879
A. Nieuwoudt, T. Ragheb, Y. Massoud (*Rice University*)
- 51.3 Chameleon ART: A Non-Optimization Based Analog Design Migration Framework** 885
S. Hammouda (*Mentor Graphics Egypt, University of Calgary*), H. Said (*Ain Shams University*),
M. Dessouky, M. Tawfik (*Mentor Graphics Egypt*), Q. Nguyen (*ON Semiconductor France SAS*),
W. Badawy (*University of Calgary*), H. Abbas (*Mentor Graphics Egypt*),
H. Shahein (*Ain Shams University*)
- 51.4 Ensuring Consistency during Front-end Design using an Object-oriented Interfacing Tool Called NETLISP** 889
M. Goffioul (*IMEC vzw. - Wireless Research*),
G. Vandersteen (*IMEC VZW-Wireless Research & Vrije Universiteit Brussel*),
J. Van Driessche, B. Debaillie, B. Come (*IMEC vzw. - Wireless Research*)

SESSION 52: High-Performance Simulation of Transaction Level and Dataflow Models	
Chair: Felice Balarin (<i>Cadence Berkeley Labs.</i>)	
Organizers: Adam Donlin, Andres R. Takach, Luciano Lavagno, & Sandeep Shukla	
52.1	Efficient Simulation of Critical Synchronous Dataflow Graphs 893
	C.-J. Hsu (<i>University of Maryland</i>), S. Ramasubbu (<i>Agilent Technologies Inc.</i>), M.-Y. Ko (<i>University of Maryland</i>), J. L. Pino (<i>Agilent Technologies Inc.</i>), S. S. Bhattacharyya (<i>University of Maryland</i>)
52.2	Exploring Trade-Offs in Buffer Requirements and Throughput Constraints for Synchronous Dataflow Graphs 899
	S. Stuijk, M. Geilen, T. Basten (<i>Eindhoven University</i>)
52.3	GreenBus - A Generic Interconnect Fabric for Transaction Level Modelling 905
	W. Klingauf, R. Günzel (<i>TU Braunschweig</i>), O. Bringmann, P. Parfuntseu (<i>FZI, Microelectronic System Design</i>), M. Burton (<i>GreenSocs Ltd.</i>)
52.4	A Framework for Embedded System Specification under Different Models of Computation in SystemC 911
	F. Herrera, E. Villar (<i>University of Cantabria</i>)
52.5	A Model-driven Design Environment for Embedded Systems 915
	E. Riccobene (<i>University of Milano</i>), P. Scandurra (<i>University of Catania</i>), A. Rosti, S. Bocchio (<i>STMicroelectronics</i>)
SESSION 53: Nano- and Bio-Chip Design	
Chair: Ion Mandoiu (<i>University of Connecticut</i>)	
Organizers: Igor Markov & Niraj Jha	
53.1	Design Automation for DNA Self-Assembled Nanostructures 919
	C. Pistol, A. R. Lebeck, C. Dwyer (<i>Duke University</i>)
53.2	Automated Design of Pin-Constrained Digital Microfluidic Arrays for Lab-on-a-Chip Applications 925
	W. L. Hwang, F. Su, K. Chakrabarty (<i>Duke University</i>)
53.3	Placement of Digital Microfluidic Biochips Using the T-tree Formulation 931
	P.-H. Yuh, C.-L. Yang, Y.-W. Chang (<i>National Taiwan University</i>)
53.4	A High Density, Carbon Nanotube Capacitor for Decoupling Applications 935
	M. Budnik, A. Raychowdhury, A. Bansa, K. Roy (<i>Purdue University</i>)
SESSION 54: Logic and Sequential Synthesis	
Chair: Maciej Ciesielski (<i>University of Massachusetts</i>)	
Organizers: Adam Donlin, Jean Christophe Madre, & Malgorzata Marek-Sadowska	
54.1	State Encoding of Large Asynchronous Controllers 939
	J. Carmona, J. Cortadella (<i>Universitat Politècnica de Catalunya</i>)
54.2	An Efficient Retiming Algorithm Under Setup and Hold Constraints 945
	C. Lin, H. Zhou (<i>Northwestern University</i>)
54.3	ExtensiveSlackBalance: an Approach to Make Front-end Tools Aware of Clock Skew Scheduling 951
	K. Wang, L. Duan, X. Cheng (<i>Peking University</i>)
54.4	Budgeting-Free Hierarchical Design Method for Large Scale and High-Performance LSIs 955
	Y. Nakamura (<i>Waseda University</i>), M. Tagata (<i>Houriku Corporation</i>), T. Okamoto, S. Tawada, K. Yoshikawa (<i>NEC Corporation</i>)
54.5	Variability Driven Gate Sizing for Binning Yield Optimization 959
	A. Davoodi, A. Srivastava (<i>University of Maryland</i>)

SESSION 55: Low Power Circuit Design

Chair: Ali Keshavarzi (*Intel Corporation*)

Organizers: Naehyuck Chang & Trevor Mudge

- 55.1 Elmore Model for Energy Estimation in RC Trees** 965
Q. Zhou, K. Mohanram (*Rice University*)
- 55.2 Self-Calibration Technique for Reduction of Hold Failures in Low-Power Nano-scaled SRAM** 971
S. Ghosh, S. Mukhopadhyay, K. Kim, K. Roy (*Purdue University*)
- 55.3 A Novel Variation-Aware Low-Power Keeper Architecture for Wide Fan-in Dynamic Gates** 977
H. F. Dadgour (*University of California at Santa Barbara*),
R. V. Joshi (*IBM T.J. Watson Research Center*),
K. Banerjee (*University of California at Santa Barbara*)
- 55.4 Standard Cell Library Optimization for Leakage Reduction** 983
S. Shah (*University of Michigan*), P. Gupta, A. Kahng (*Blaze DFM, Inc.*)
- 55.5 Low-Power Bus Encoding Using an Adaptive Hybrid Algorithm** 987
A. R. Brahmabhatt, J. Zhang, Q. Wu, Q. Qiu (*Binghamton University*)

SESSION 56: Beyond-The-Die Circuit and System Integration

Chair: Shauki Elassaad (*Emergent Design Solutions*)

Organizers: John Berrie & Mike Heimlich

- 56.1 A Thermally-Aware Performance Analysis of Vertically Integrated (3-D) Processor-Memory Hierarchy** 991
G. L. Loi, B. Agrawal, N. Srivastava, S.-C. Lin, T. Sherwood,
K. Banerjee (*University of California at Santa Barbara*)
- 56.2 Exploring Compromises among Timing, Power and Temperature in Three-Dimensional Integrated Circuits** 997
H. Hua, C. Mineo, K. Schoenfliess, A. Sule, S. Melamed,
R. Jenkal, W. R. Davis (*North Carolina State University*)
- 56.3 Efficient Escape Routing for Hexagonal Array of High Density I/Os** 1003
R. Shi, C.-K. Cheng (*University of California at San Diego*)
- 56.4 System Level Signal and Power Integrity Analysis Methodology for System-In-Package Applications** 1009
R. Mandrekar, K. Bharath, K. Srinivasan, E. Engin, M. Swaminathan (*Georgia Institute of Technology*)
- 56.5 PELE: Pre-emphasis & Equalization Link Estimator to Address the Effects of Signal Integrity Limitations** 1013
W. Bereza, Y. Tao, S. Wang, T. Kwasniewski, R. H. Patel (*Altera Corporation*)

SESSION 57: New Ideas in Analog/RF Modeling and Simulation

Chair: Luca Daniel (*Massachusetts Institute of Technology*)

Organizers: Koen Lampaert & Rob A. Rutenbar

- 57.1 A Multilevel Technique for Robust and Efficient Extraction of Phase Macromodels of Digitally Controlled Oscillators** 1017
X. Lai, J. Roychowdhury (*University of Minnesota*)
- 57.2 Systematic Development of Nonlinear Analogy Circuit Macromodels through Successive Operator Composition and Nonlinear Model Decoupling** 1023
Y. Wei, A. Doholi (*Stony Brook University*)
- 57.3 A Robust Envelope Following Method Applicable to Both Non-autonomous and Oscillatory Circuits** 1029
T. Mei, J. Roychowdhury (*University of Minnesota*)
- 57.4 Lookup Table Based Simulation and Statistical Modeling of Sigma-Delta ADCs** 1035
G. Yu, P. Li (*Texas A&M University*)

SESSION 58: Advanced Methods for Interconnect Extraction, Clocks and Reliability	
Chair: Arvind NV (<i>Texas Instruments Inc.</i>)	
Organizers: Farid N. Najm & Nagaraj NS	
58.1	Clock Buffer and Wire Sizing Using Sequential Programming 1041
	M. R. Guthaus, D. Sylvester (<i>University of Michigan</i>), R. B. Brown (<i>University of Utah</i>)
58.2	Modeling and Mimimization of PMOS NBTI Effect for Robust Nanometer Design 1047
	R. Vattikonda, W. Wang, Y. Cao (<i>Arizona State University</i>)
58.3	A Parallel Low-Rank Multilevel Matrix Compression Algorithm for Parasitic Extraction of Electrically Large Structures 1053
	C. Yang (<i>University of Wisconsin</i>), S. Chakraborty, D. Gope, V. Jandhyala (<i>University of Washington</i>)
58.4	Reliability Modeling and Management in Dynamic Microprocessor-Based Systems 1057
	E. Karl, D. Blaauw, D. Sylvester, T. Mudge (<i>University of Michigan</i>)
SESSION 59: Panel — DFM: Where’s the Proof of Value? 1061	
Chair: Joe Brandenburg (<i>Consultant</i>)	
Organizers: Linda Marchant (<i>Cayenne Communication</i>) & Shishpal Rawat (<i>Intel Corporation</i>)	
Panelists: R. Camposano (<i>Synopsys Inc.</i>), A. Kahng (<i>Blaze DFM, Inc.</i>), J. Sawicki (<i>Mentor Graphics</i>), M. Gianfagna (<i>Aprio Technologies</i>), N. Zafar (<i>Pyxis Technology</i>), A. Sharan (<i>Clear Shape Technologies</i>)	
SESSION 60: Bounded Model Checking and Equivalence Verification	
Chair: Gagan Hasteer (<i>Calypto Design Systems, Inc.</i>)	
Organizers: Anmol Mathur & Avi Ziv	
60.1	Early Cutpoint Insertion for High-Level Software vs. RTL Formal Combinational Equivalence Verification 1063
	X. Feng, A. J. Hu (<i>University of British Columbia</i>)
60.2	Transistor Abstraction for the Functional Verification of FPGAs 1069
	G. Dupenloup, T. Lemeunier, R. Mayr (<i>Altera Corporation</i>)
60.3	Automatic Invariant Strengthening to Prove Properties in Bounded Model Checking 1073
	M. Awedh, F. Somenzi (<i>University of Colorado at Boulder</i>)
60.4	Fast Falsification Based on Symbolic Bounded Property Checking 1077
	P. M. Peranandam, P. K. Nalla, J. Ruf, R. J. Weiss, T. Kropf, W. Rosenstiel (<i>University of Tübingen</i>)
SESSION 61: Test Response Compaction and ATPG	
Chair: Anuja Sehgal (<i>Advanced Micro Devices, Inc.</i>)	
Organizers: Kazumi Hatayama & Patrick Girard	
61.1	Unknown-Tolerance Analysis and Test-Quality Control for Test Response Compaction using Space Compactors 1083
	M. C.-T. Chao, K.-T. Cheng (<i>University of California at Santa Barbara</i>), S. Wang, S. Chakradhar, W.-L. Wei (<i>NEC Labs. America</i>)
61.2	Test Response Compactor with Programmable Selector 1089
	G. Mrugalski, J. Rajski (<i>Mentor Graphics Corp.</i>), J. Tyszer (<i>Poznań University of Technology</i>)
61.3	Fault Detection and Diagnosis with Parity Trees for Space Compaction of Test Responses 1095
	H. Vranken, S. K. Goel (<i>Philips Research</i>), A. Glowatz, J. Schloeffel, F. Hapke (<i>Philips Semiconductors</i>)
61.4	Multiple-Detect ATPG Based on Physical Neighborhoods 1099
	J. E. Nelson, J. G. Brown, R. Desineni, R. D. Blanton (<i>Carnegie Mellon University</i>)

SESSION 62: Placement

Chair: Bill Halpin (*Synplicity, Inc.*)

Organizers: Jiang Hu & Louis Scheffer

62.1	Constraint-Driven Floorplan Repair	1103
	M. D. Moffitt, A. N. Ng, I. L. Markov, M. E. Pollack (<i>University of Michigan</i>)	
62.2	Optimal Cell Flipping in Placement and Floorplanning	1109
	C.-w. Sham, E. F. Y. Young (<i>Chinese University of Hong Kong</i>), C. Chu (<i>Iowa State University</i>)	
62.3	A New LP Based Incremental Timing Driven Placement for High Performance Designs	1115
	T. Luo (<i>University of Texas at Austin</i>), D. Newmark (<i>Advanced Micro Devices</i>), D. Z. Pan (<i>University of Texas at Austin</i>)	
	Author Index	1121

EXECUTIVE COMMITTEE



GENERAL CHAIR

Ellen M. Sentovich
Cadence Berkeley Labs
1995 University Ave. Ste. 460
Berkeley, CA 94704
510-647-2807
ellens@cadence.com



VICE/FINANCE CHAIR

Steven P. Levitan
University of Pittsburgh, ECE Dept.,
348 Benedum Eng. Hall
Pittsburgh, PA 15261
412-648-9663
steve@ee.pitt.edu



TECHNICAL PROGRAM CO-CHAIR (METHODS)

Grant E. Martin
Tensilica, Inc.
3255-6 Scott Blvd.
Santa Clara, CA 95054
408-327-7323
gmartin@tensilica.com



TECHNICAL PROGRAM CO-CHAIR (TOOLS)

Sachin Sapatnekar
University of Minnesota
200 Union St., 4-174 EE/CSI
Minneapolis, MN 55455
612-625-0025
sachin@ece.umn.edu



EDA INDUSTRY CHAIR

Limor Fix
Intel Research Pittsburgh
4720 Forbes Ave., Ste. 410
Mailstop CM2
Pittsburgh, PA 15213
412-297-4021
limor.fix@intel.com



PAST CHAIR

William H. Joyner, Jr.
IBM Corp./SRC
PO Box 12053
Research Triangle Park,
NC 27709
919-941-9472
william.joyner@src.org



TUTORIAL CHAIR

Leon Stok
IBM Corp.
2070 Route 52
Hopewell Junction, NY 12533
845-892-5262
leonstok@us.ibm.com



PANEL CHAIR

Dennis Brophy
Mentor Graphics Corp.
8005 SW Boeckman Rd., Bldg. E4
Wilsonville, OR 97070
503-685-0893
dennisb@model.com



DESIGN COMMUNITY CHAIR

Ingrid Verbauwhede
Katholieke University
Kasteelpark Arenberg 10
Leuven, Belgium
+32-16-32-86-25
ivebauw@esat.kuleuven.be



NEW INITIATIVES CHAIR

Andrew B. Kahng
Univ. of California at San Diego
CSE & ECE Depts. 0114
9500 Gilman Dr.
La Jolla, CA 92093
858-822-4884
abk@cs.ucsd.edu

EXECUTIVE COMMITTEE (Continued)



PUBLICITY CHAIR
Nanette V. Collins
Public Relations Consultant
37 Symphony Rd., Unit A
Boston, MA 02115
617-437-1822
nanette@nvc.com



EUROPE/MIDDLE EAST REPRESENTATIVE
Ahmed A. Jerraya
TIMA Lab
46, Avenue Felix Viallet
Grenoble Cedex, France F-38031
+33 476-574759
ahmed.jerraya@imag.fr



ASIA/SOUTH PACIFIC REPRESENTATIVE
Yusuke Matsunaga
Kyushu University
6-1 Kasuga Koen
Kasuga, Fukuoka
816-8580, Japan
+81 92-583-7621
matsunaga@c.csce.kyushu-u.ac.jp



ACM/SIGDA REPRESENTATIVE
Diana Marculescu
Carnegie Mellon University
EEC Department - HH #2124
Pittsburgh, PA 15213
412-268-1167
dianam@ece.cmu.edu



IEEE/CASS/CANDE REPRESENTATIVE
Alan Mantooth
University of Arkansas
Dept. of EE
3217 Bell Engineering Center
Fayetteville, AR 72701
479-575-4838
mantooth@uark.edu



EDA CONSORTIUM REPRESENTATIVE
Anne Cirkel
Mentor Graphics Corp.
8005 SW Boeckman Rd.
Wilsonville, OR 97070
503-685-7934
anne_cirkel@mentorg.com



CONFERENCE MANAGER
Kevin Lepine
MP Associates, Inc.
5405 Spine Rd., Ste. 102
Boulder, CO 80301
303-530-4562
kevin@mpassociates.com



EXHIBITS MANAGER
Lee Wood
MP Associates, Inc.
5405 Spine Rd., Ste. 102
Boulder, CO 80301
303-530-4562
lee@mpassociates.com

TECHNICAL PROGRAM COMMITTEE

Grant E. Martin
Technical Program Co-Chair
Tensilica, Inc.
gmartin@tensilica.com

Sachin Sapatnekar
Technical Program Co-Chair
University of Minnesota
sachin@ece.umn.edu

Brian Bailey
Consultant
Oregon City, OR

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Denton, TX

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MONDAY KEYNOTE ADDRESS



Joe Costello
Chairman of the Board,
Orb Networks, Inc.

iPod or Iridium – Which One Are You Going To Be?

Abstract: An incredible amount of time, resources and investment is being made by EDA, chip, and electronics companies to win in the exploding multi-media, gaming, and entertainment applications markets. With the 2006 DAC conference doing a much-needed “deep dive” into how the semiconductor industry meets technical challenges, Joe Costello, Chairman of Orb Networks, Inc., will turn the spotlight away from technology and onto today’s macro consumer trends.

During this session, Joe challenges participants with this fundamental question: are you going in the right direction? As you bend your minds with the complexity of implementing modern day systems and chips, are you racing toward the right finish line? What are consumers really looking for? What will convergence really lead to and are you positioned to take advantage of all it will bring our industry and our world? Join Joe as he reveals lessons learned and offers a simple view of the future of electronics.

Biography: Joe Costello is chairman, co-founder, and an investor in Orb Networks, Inc. He is highly regarded for his business acumen and bold moves in the high-tech industry. In 1997, Chief Executive Magazine named Costello the top performing CEO of all publicly traded companies in North America. He also made Upside Magazine’s 1997 “Elite 100” list of the top executives leading the digital revolution. He serves as CEO and chairman of think3, a developer of computer-aided design software used throughout the product development process. He is also chairman of other privately-held companies that include Radio, Abazab and SpeakESL. In addition, Costello is on the board of Mercury Interactive, a publicly-held company. Prior to think3, Costello played a pivotal role as president and CEO at Cadence Design Systems, Inc. for more than a decade. Under his leadership, Cadence became the world’s leading supplier of electronic EDA software and services, and one of the ten highest-grossing software vendors in the world. Costello holds a bachelor of science degree in mathematics and physics from Harvey Mudd College, a master of science degree in physics from Yale University, and a master of science degree in physics from the University of California, Berkeley.

GENERAL SESSION KEYNOTE ADDRESS



Hans Stork

Senior Vice President and Chief Technology Officer,
Director of Silicon Technology Department
Texas Instruments Inc.

Structuring Process and Design for Future Mobile Communication Devices

Abstract: The density and speed of sub-50nm CMOS technology enables the design of multi-functional SoCs for highly integrated, mobile, communication devices. At the same time, process variations, power issues and complexity of scope are challenging even the most advanced simulation capabilities. The growing design complexity is addressed by rapidly improving modeling of systematic manufacturing variations and design sensitivities. Physical design is becoming more structured to allow for process optimized design rules and efficient automation. While challenges remain in the scaling and optimization of analog and I/O functions, highly integrated, mobile communication devices are a major driving force for continued economies of scaling.

Biography: Dr. Stork is Senior Vice President, and Chief Technology Officer, of Texas Instruments. As Director of the Silicon Technology Development organization, he is responsible for ensuring that process technology provides a competitive advantage for TI's products.

Prior to joining Texas Instruments in 2001, Dr. Stork was Director of the ULSI Research Lab and later the Internet Systems and Storage Lab at HP Laboratories, Hewlett-Packard. Dr. Stork started his professional career at IBM's T.J. Watson Research Center, working on advanced bipolar technology and circuits, and his group demonstrated the early successes SiGe HBTs.

Dr. Stork serves on the Board of Directors for International Sematech and the Semiconductor Research Corporation (SRC). He also serves on the Governing Councils of the Focus Center Research Programs and Nanotechnology Research Initiative. He is a member of the SIA Technology Strategy Committee.

THURSDAY KEYNOTE ADDRESS



Alessandro Cremonesi

Strategy and System Technology Group Vice President
and Advanced System Technology General Manager,
STMicroelectronics

The Challenges of Convergence

Abstract: In this talk, the trends of the major application fields in the era of convergence are analyzed. The emphasis is on the challenges the semiconductor industry will have to face to address these new trends and opportunities.

Applications are becoming increasingly complex and the need to guarantee the coexistence of a wider range of applications on a single chip makes system-level integration a real challenge. Most of the applications will run on platforms designed for portable products, pushing the industry to emphasize power budgets for new designs, both at silicon and at system level. From the platform architecture perspective, multiprocessing is already a reality and the industry will have to find new paradigms to handle the increased complexity at the system, embedded software, and at the silicon implementation level.

The talk concludes with future perspectives, from the viewpoint of ST's advanced research organization.

Biography: Alessandro Cremonesi received a Doctorate in Electronics Engineering from the University of Pavia, Italy, in 1984. After a period of research activity in the opto-electronics field at the University of Pavia, he joined STMicroelectronics working in different fields from telecommunications to audio/video digital signal processing and multimedia applications. At present, Alessandro Cremonesi is Vice President of Strategy and System Technology group and General Manager of Advanced System Technology (AST) group at STMicroelectronics with the responsibility of the Corporate System R&D and the Corporate Strategic Marketing activities across 14 different STMicroelectronics Labs worldwide.

Marie R. Pistilli Women in EDA Achievement Award

Ellen J. Yoffa – Director of Next Generation Web, IBM T.J. Watson Research Center, Yorktown Heights, NY

For her significant contributions in helping women advance in the field of EDA technology.

The P. O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P. O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship, and SIGDA continues to administer the program for DAC. DAC normally funds two or more \$4000 scholarships, renewable up to 5 years, to graduating high school seniors.

The 2006 winners are:

Katlyn DeLuca – attending University of Massachusetts, Lowell, MA

Eletha Flores – attending Massachusetts Institute of Technology, Cambridge, MA

For more information about the P. O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several \$24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in “design and test automation of electronic and computer systems.” Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. **Jennifer L. Dworak**, Division of Engineering – Electrical Sciences and Computer Engineering, Brown University, Providence, RI

Student: **Elif Alpaslan**

*A Statistical Coverage Metric and Stimulus Generation Approach for Design Verification
Based upon Structural Analysis of the Design and Stimulus*

Prof. **Daniel Kroening**, Computer Systems Institute, Swiss Institute of Technology, Zurich, Switzerland

Student: **Vijay D’silva**

Automatic Detection of Multi-Cycle Paths in Large Circuits

Information on next year’s DAC scholarship award program will be available on the DAC web site: <http://www.dac.com>.

DAC/ISSCC 2006 Student Design Contest Winners

Operational Chip Design Category:

- 1st Place** *A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW*
- (Best Overall)** Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni – University of Pisa
Bert Gyselinckx, Liesbet Van der Perre, Geert Van der Plas – IMEC
- 2nd Place (tie)** *Increasing the Time Dynamic Range of Pulse Measurement Techniques in Digital CMOS*
Mona Safi-Harb, Gordon W. Roberts – McGill University
- 2nd Place (tie)** *A DSP Enabled Microsystem for Cochlear Implants with Hybrid LC Clocking*
Eric D. Marsman, Robert M. Senger – University of Michigan
Richard B. Brown – University of Utah
- 3rd Place** *A 160K Gates/4.5KB SRAM H.264 Video Decoder for HDTV Applications*
Chien-Chang Lin, Jia-Wei Chen, Hsiu-Cheng Chang, Chao-Ching Wang, Yi-Huan Ou-Yang, Ming-Chih Tsai, Yao-Chang Yang, Jiun-In Guo, Jinn-Shyan Wang – National Chung Cheng University

Operational System Design Category:

- 1st Place** *Demonstration of Uncoordinated Multiple Access in Optical Communications*
Herwin Chan, Andres I. Vila Cadaso, Juthika Basak, Miguel Griot, Wen-Yen Weng, Richard Wesel, B. Jalali, Eli Yablonovitch – University of California, Los Angeles
Ingrid Verbauwhede – University of California, Los Angeles & Katholieke University, Leuven
- 2nd Place** *Illumimote: A High Performance Light Sensor Module for Wireless Sensor Networks*
Heemin Park, Jonathan Friedman, Mani B. Srivastava, Pablo Gutierrez, Vidyut Samanta, Jeff Burke – University of California, Los Angeles
- 3rd Place** *An Ultra Low Power Wireless Micro-Sensor Node*
Denis Daly, Daniel Finchelstein, Nathan Ickes, Naveen Verma, Anantha Chandrakasan – Massachusetts Institute of Technology
- Honorable Mention** *Phase Delay Based Collision Avoidance RADAR for Smart Automobiles*
Babu L. Saincha – Indian Institute of Information Technology

Conceptual Category:

- 1st Place** *ASIC Implementation of LDPC Decoder Accelerating Message-Passing Schedule*
Kazunori Shimizu, Tatsuyuki Ishikawa, Nozomu Togawa, Takeshi Ikenaga, Satoshi Goto – Waseda University

The ACM Transactions on Design Automation of Electronic Systems (TODAES) 2006 Best Paper Award

Zero Cost Indexing for Improved Processor Cache Performance
Volume 11, Issue 1, January 2006, Pages 3–25

Tony Givargis – University of California, Irvine, CA

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) Distinguished Service Award

Robert A. Walker – Kent State University, Kent, OH

For dedicated service as SIGDA Chair (2001–2005), and over a decade of service to SIGDA, DAC, and the EDA profession

2005 Phil Kaufman Award for Distinguished Contributions to EDA

Phil Moorby – Chief Scientist, Synopsys, Inc.

Phil Moorby is the recipient of the prestigious EDA Consortium 2005 Phil Kaufman Award for industry contributions as the inventor of the Verilog hardware design language (HDL) which has become, and today remains, one of the world's most popular electronic design languages.

IEEE Circuits and Systems Society 2006 Education Award

Wayne Wolf – Princeton University, Princeton, NJ

For outstanding education and leadership in VLSI systems and embedded computing

IEEE Circuits and Systems Society 2006 Industrial Pioneer Award

John A Darringer – IBM T. J. Watson Research Center, Yorktown Heights, NY

For the development of practical techniques and algorithms for automated logic synthesis, for their realization as usable tools, and for their successful application to high performance computing products

IEEE Circuits and Systems Society 2006 Donald O. Pederson Award

Janusz Rajski – Mentor Graphics Corp., Wilsonville, OR

Jerzy Tyszer – Poznan University of Technology, Poznan, Poland

Mark Kassab – Mentor Graphics Corp., Wilsonville, OR

Nilanjan Mukherjee – Mentor Graphics Corp., Wilsonville, OR

For the paper entitled, *Embedded Deterministic Test*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 5, pp. 776–792, May 2004