Journal of Instrumentation

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To cite this article: L. Gaioni *et al* 2024 *JINST* **19** C04001

Published by IOP Publishing for Sissa Medialab

Received: *November 3, 2023*
Accepted: *February 12, 2024*
Published: *April 2, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

28 nm front-end channels for the readout of pixel sensors in future high-rate applications

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Abstract: This work is concerned with the design and the characterization of front-end channels, developed in a 28 nm CMOS technology, conceived for the readout of pixel sensors in future, high-rate applications at the next generation facilities. Two front-end architectures are discussed. In the first one, an in-pixel flash ADC is exploited for the digitization of the signal, whereas the second one features a Time-over-Threshold (ToT) approach. A prototype including the ADC-based front-end has been submitted and the characterization of the chip is discussed in the paper. Simulation results relevant to the ToT-based architecture are reported.

Keywords: Front-end electronics for detector readout; Analogue electronic circuits; Electronic detector readout concepts (solid-state)

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https://doi.org/10.1088/1748-0221/19/04/C04001

Contents

1 Introduction

State-of-the-art readout channels for pixel detectors in high energy physics (HEP) experiments are being developed, in a 65 nm CMOS technology, by the RD53 collaboration [1], established at CERN in 2013. The RD53 design team submitted three families of readout chips optimized for the high luminosity (HL) upgrades of the ATLAS and CMS experiments at the LHC. The RD53 chips have been extensively characterized, and proved to be able to withstand total ionizing doses (TIDs) up to 1 Grad(SiO_2), while preserving the main performance parameters [2].

The HEP designers' community is now generally migrating to the 28 nm process for the development of new circuits [3, 4]. The 28 nm node is the major commercial successor of the 65 nm one, and brings along some interesting features. A number of test campaigns with TIDs in the Grad regime did show that properly sized 28 nm transistors can be operated with limited performance losses [5, 6]. Moreover, the scaling-down process intrinsically improves speed and density of digital circuits, allowing the designers to develop very compact pixel cells and fast readout logic and I/O circuits. This makes the 28 nm technology an ideal candidate for the design of next generation, high data rate readout chips to be operated in extremely harsh radiation environments.

This work discusses the design of two front-end circuits being developed in the framework of the INFN Falaphel project, aiming at the integration of silicon photonics modulators with high speed, rad-hard electronics in a 28 nm CMOS technology. The Falaphel project was conceived having in mind the challenging requirements set by the tracker of the hadronic Future Circular Collider [7]. Nonetheless, the outcome of the project can be of interest for a potential replacement of the innermost pixel layers of the HL-LHC experiments after 2030. The two architectures described in this work implement different digitization techniques. The first one relies on an in-pixel flash ADC, and is intended for synchronous environments, where events take place with a known repetition rate and with a non negligible probability of hits occurring in adjacent time segments. The second architecture leverages the Time-over-Threshold method, and shares the same specifications of the RD53 front-end channels [8], but targets lower threshold operation. A prototype including a matrix of 8×4 flash ADC-based channels has been submitted and the preliminary characterization of the chip is discussed in the paper. Simulation results relevant to the ToT-based architecture, whose submission is foreseen for the beginning of 2024, are reported.

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2 Flash ADC-based front-end

The schematic diagram of the flash ADC-based front-end is shown in figure 1. The readout channel includes a charge sensitive amplifier (CSA) with detector leakage compensation. The CSA features two independent feedback loops: a fast one, featuring transistor M_F operated as a constant current source, provides a linear discharge of the CSA feedback capacitance. A slower loop, including the M_L transistor and an RC network which guarantees low-frequency operation of the feedback, has instead been devised to compensate for the sensor leakage current. The preamplifier core is a regulated cascode gain stage with a common drain output stage, needed to face kick-back noise from the comparator. In the flash ADC-based channel, a set of three clocked comparators are connected to the preamplifier, providing a 2-bit resolution analog-to-digital conversion (the schematic of one comparator is shown in figure 1). In this specific implementation, the threshold is a negative voltage step, synchronous with the clock falling edge, injected at the comparator input together with the signal from the CSA (which can be approximated by means of a positive voltage step). As a result, a positive going signal is present at the gate of M_1 for a signal exceeding the threshold: such a signal is amplified by the cascade of two common source structures (featuring M_1 and M_2) and then converted into a digital pulse by means of a chain of two inverters. The two switches, S_1 and S_2, are controlled by the clock signal, being closed when the clock is high. In this phase, with clock high, the offset at the CSA output is stored onto C1, which is then subtracted from the signal in the comparison phase, when the clock is low and the signal from CSA and the threshold one are injected to the comparator. This architecture is expected to be rather insensitive to device threshold mismatch, since the threshold and the preamplifier signals are fed to the gate of one single transistor. Typical implementations, instead, rely on differential pair structures, where the mismatch of the input transistors is a critical source of front-end threshold dispersion. A detailed description of the comparator is given in [9]. The total current consumption of the front-end is 5.4 µA, with the main contribution, around 3 µA, being the one from the CSA, and a current of 800 nA per comparator. With a power supply voltage of 0.9 V, this translates to a total power consumption of 4.9 µW/channel.

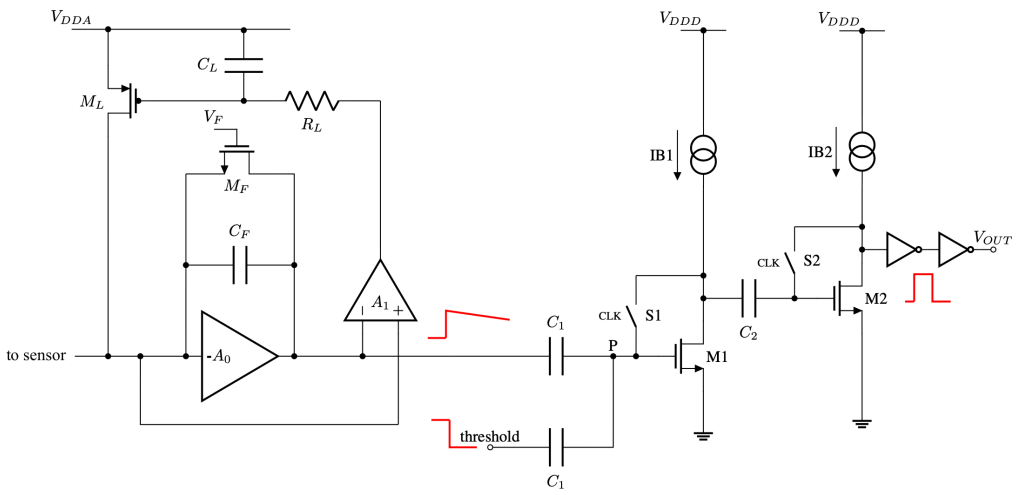

Figure 1. Schematic diagram of the flash ADC-based front-end. The preamplifier is AC coupled to a clocked comparator featuring auto-zero. A set of three identical comparators is needed to implement a 2-bit flash ADC, each featuring a dedicated threshold input. Coupling capacitors C1 and C2 are equal to 15 fF and 35 fF, respectively.

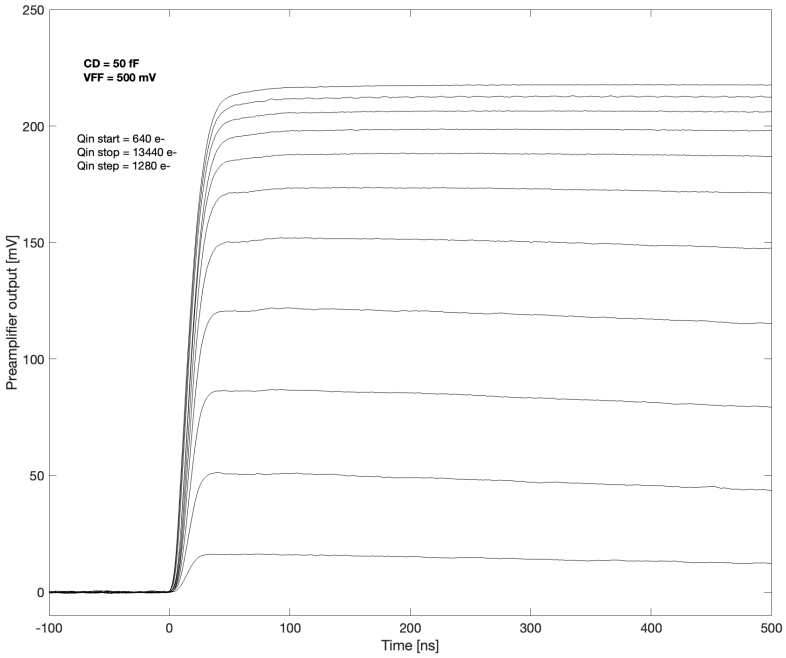

Figure 2. Measured preamplifier response to an input signal ranging from 640 up to 13440 electrons. A 50 fF detector emulating capacitor was enabled during data taking.

As mentioned in the introduction, the submitted prototype chip includes a small matrix of readout channels, with the CSA output of a peripheral pixel being sent to a dedicated pad (through a source follower stage). Each pixel in the matrix is equipped with two capacitors (25 fF and 50 fF) which can be selectively connected to the preamplifier input, emulating the presence of a detector. An injection circuit (not shown in the schematic of figure 1) makes it possible to provide test signals to the front-end channel. Figure 2 shows the measured CSA output of the peripheral pixel in response to an input signal ranging from around 600 up to 13000 electrons, for a detector emulating capacitance of 50 fF. The output signal features a very slow return-to-baseline (close to 5 µs for an input signal of 6000 electrons), which is requested for proper operation of the subsequent comparator stage. The CSA peak amplitude is found to be linear with the injected charge for signals up to around 7000 electrons, while a saturation effect is clearly visible for larger signals. The measured Equivalent Noise Charge (ENC) is shown in figure 3 as a function of the detector emulating capacitance. An ENC close to 80 electrons r.m.s. was achieved for a detector capacitance of 50 fF, which is deemed to be a reasonable value for the pixel sensors to be used in the innermost layers of the CMS and ATLAS experiments at the HL-LHC.

3 ToT-based front-end

The schematic diagram of the ToT-based front-end is shown in figure 4. The gain stage of the CSA is implemented by means of a self-cascode amplifier [10], whose bandwidth has been purposely limited to enhance the noise performance of the front-end processor. The feedback architecture is identical to the one described in the previous section, while the overall current consumption of the preamplifier is smaller, around 2 µA. At the CSA output, the single-ended signal is converted into a differential one through the pre-comparator stage, featuring a differential pair with diode-connected MOS load, with a

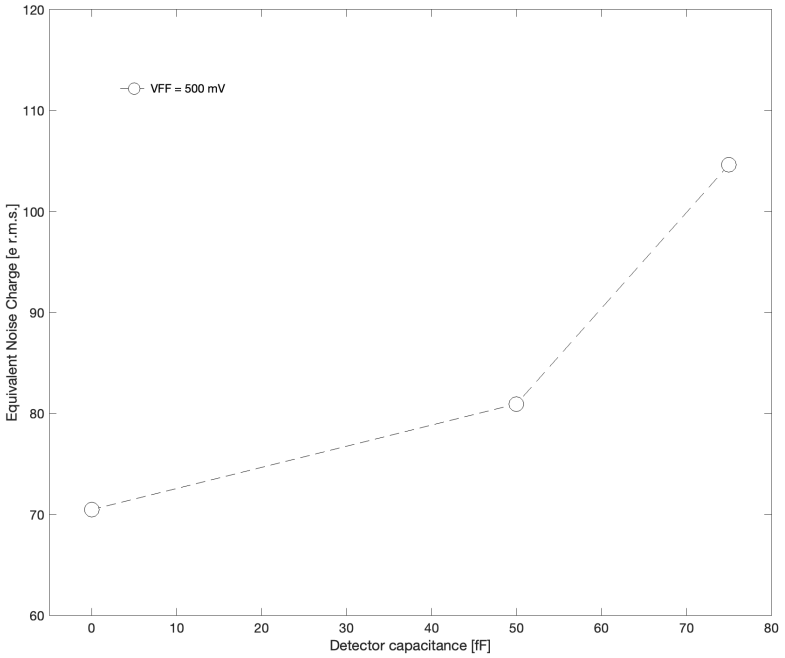

Figure 3. Measured Equivalent Noise Charge as a function of the detector capacitance.

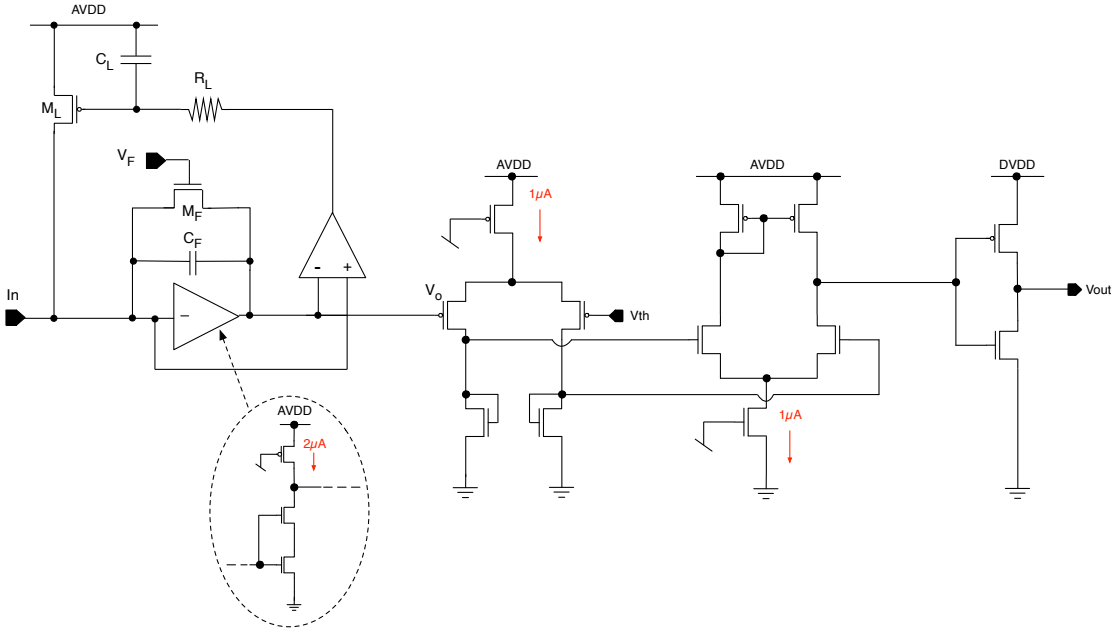

Figure 4. Schematic diagram of the ToT-based front-end. The preamplifier is DC coupled to a pre-comparator stage, providing single-ended to differential signal conversion, followed by a discriminator stage.

current consumption close to 1 µA. A differential structure with active load is instead exploited for the subsequent discriminator stage, whose quiescent current is, again, around 1 µA, and which feeds a CMOS inverter consolidating the digital levels at the output of the readout chain. The global threshold, V_{th}, is applied at the input of the pre-comparator stage, while a local threshold tuning DAC (not shown in the schematic of figure 4) is needed to bring the threshold dispersion down to manageable levels.

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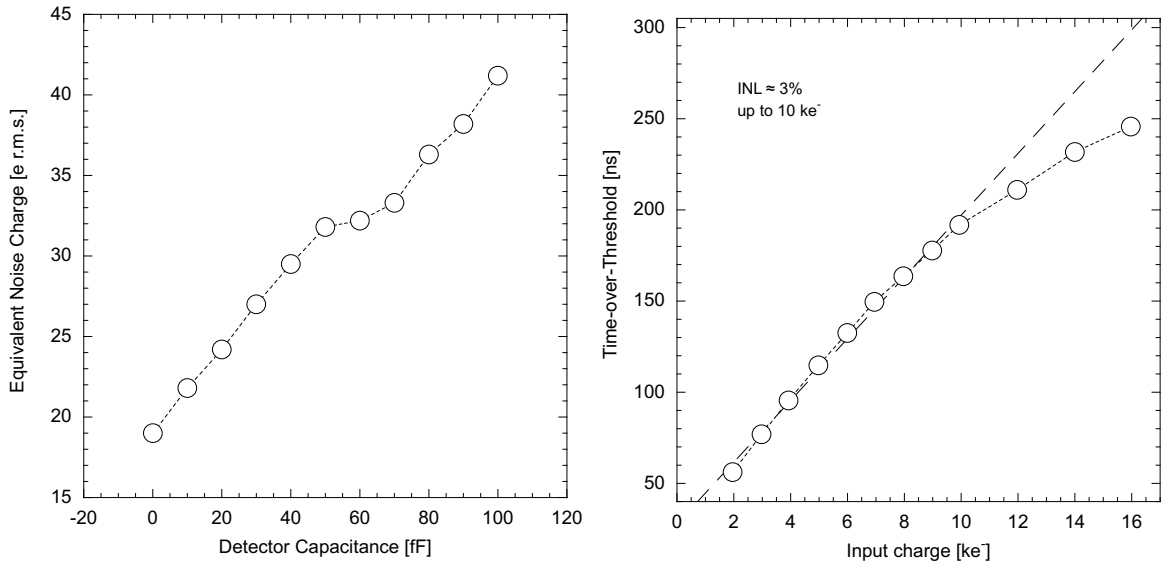

Figure 5. Equivalent Noise Charge as a function of the detector capacitance (left) and Time-over-Threshold as a function of the input charge (right).

Figure 5 (left) shows the simulated equivalent noise charge as a function of the detector capacitance for the ToT-based front-end. An ENC close to 32 e r.m.s. has been obtained for a sensor capacitance of 50 fF. The results shown here are relevant to the readout channel simulated at schematic level in the TT corner, for a temperature of −20°C (which is expected for the pixel readout chips for the Phase-II upgrades of the CMS and ATLAS experiments). Figure 5 (right) shows the Time-over-Threshold as a function of the input charge, for a global threshold set around 1000 electrons. A linear behavior (with an integral non linearity close to 3%) was achieved for input signals up to 10000 electrons.

4 Conclusion

Two pixel readout circuit architectures have been briefly discussed in this work. Such architectures, developed in a 28 nm CMOS technology in the framework of the INFN Falaphel project, are devised for the readout of pixels sensors in future, high-rate applications at the next generation facilities. The first architecture discussed in the paper features an in-pixel flash ADC, whereas the second one is based on Time-over-Threshold conversion. A prototype chip including the flash ADC-based front-end has been submitted and the test results show that the analog processor can be operated with an ENC not exceeding 100 electrons r.m.s. for a detector capacitance close to 50 fF, compatible to the value expected for the sensors to be used in the innermost layers of the tracker in the phase-2 upgrades of the CMS and ATLAS experiments. The design of a very low-noise, ToT-based front-end is in progress, with a submission of a small readout matrix planned for the beginning of 2024.

Acknowledgments

The authors wish to thank Mirco Mazzoleni, who carried out the characterization of the flash ADC-based analog processor. The authors are also in debt with Massimo Manghisoni, Elisa Riceputi, Paolo Lazzaroni and Luca Ghislotti for their useful suggestions. The design activity has been carried out in the framework of the Falaphel project funded by INFN.

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