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A Time-over-Threshold asynchronous front-end in 28 nm CMOS for the readout of pixel detectors in extreme radiation environments

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Abstract: This work describes the design, in a 28 nm CMOS technology, of a front-end channel for the readout of pixel sensors in future particle accelerators. The channel being developed leverages the Time-Over-Threshold technique for the numerical conversion of the detector signal amplitude, and includes a low-noise charge sensitive amplifier featuring a compact gain stage architecture. The front-end circuit features an equivalent noise charge not exceeding 70 electrons r.m.s. for a detector capacitance of 50 fF, with a threshold dispersion of the order of 20 electrons r.m.s. A prototype chip including a matrix of 8x32 readout channels has been submitted for fabrication. The design of the front-end channel, together with the main simulation results, is discussed in the paper.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout

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Contents

2024 JINST 19 C12011

1 Introduction

In the realm of electronic circuits for high energy physics experiments, the 28 nm CMOS technology is emerging as a key enabler for the development of instrumentation in the next generation particle colliders. Such a process has been demonstrated to withstand, with rather marginal performance losses, total ionizing doses of the order of 1 Grad(SiO_2), even without introducing any specific hardening technique [1–3]. With respect to the 65 nm process, which represents the technology choice for the ASICs designed by the RD53 collaboration for the phase-II upgrades of the ATLAS and CMS experiments [4], the 28 nm node makes it possible to develop more compact digital readout logic that can be ultimately packed into smaller pixel cells. On the other hand, the design of analog circuits in the 28 nm node can be challenging: one of the main reasons for this is related to the supply voltage of the technology, which is limited to 0.9 V. Such a constraint significantly limits the number of architectures that can be implemented in the design of high-gain stages, which are the core of basic analog building blocks such as charge sensitive amplifiers and threshold discriminators. Moreover, the 28 nm CMOS technology leverages resolution enhancement techniques such as Phase-Shifting Masks, which imply a number of layout restrictions — including the usage of two dummy gates per transistor side, required for lithography and planarization, as well as maintaining a uniform component orientation throughout the silicon wafer.

This work discusses the development of a front-end circuit being designed in the framework of the INFN Falaphel project and the PiHEX project, funded by the Italian Ministry of University and Research. These projects share the developments of rad-hard, front-end electronics to be operated in harsh radiation environments, such as the one at the hadronic Future Circular Collider, and may also be relevant for possible upgrades at the CMS and ATLAS experiments in the post phase-II era at the LHC. The front-end channel described in this work exploits the Time-over-Threshold technique for the digitization of the signal delivered by the sensor. It includes a compact charge sensitive amplifier (CSA, or preamplifier), DC coupled to a differential comparator driving a Time-over-Threshold and a Time-of-Arrival counter. A 5-bit digital-to-analog converter is integrated in the elementary cell for the local tuning of the threshold.

2 Front-end design

The analog front-end schematic is shown in figure 1. The analog processor consists of a charge sensitive amplifier featuring two independent feedback loops. The one integrating the transistor M_F and the capacitor C_F is exploited for the processing of the signal (i.e. the integration of the charge

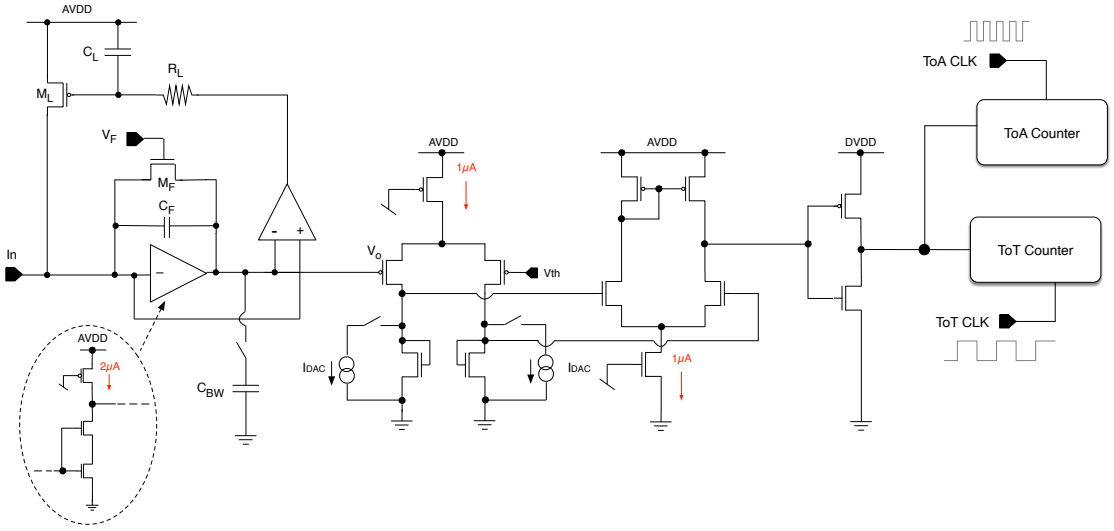

Figure 1. Schematic diagram of the front-end channel. The CSA is DC coupled to a pre-comparator stage, exploited for single-ended to differential signal conversion, followed by the comparator.

delivered by the sensor into C_F, and its subsequent discharge), while the second one, including a low-power (around 0.2 µW) amplifier and the PMOS transistor M_L, provides the front-end channel with a compensation mechanism for the detector leakage current. The feedback operational amplifier locks indeed the DC voltage at the output of the CSA to the gate-to-source voltage of the preamplifier input transistor, even in the presence of leakage, by adjusting the potential at the gate of M_L transistor. The C_L capacitor and the R_L resistor, implemented by means of a NMOS transistor with gate and source terminals tied together, introduce a very low frequency pole (at around 1 Hz) in the feedback loop, so that the compensation circuit reacts to DC leakage currents only. The CSA gain stage is based on the so-called self (or composite) cascode topology [5], providing additional gain with respect to a straightforward common source stage. From circuit simulations, the DC open-loop gain of such a stage was found to be close to 50 dB. By programming a CMOS switch, the capacitor C_{BW} (a 20 fF Metal-oxide-Metal capacitance) can load the preamplifier output to purposely limit its bandwidth (from 3 MHz, when C_{BW} is not connected to the output of the preamplifier, down to 1 MHz), with the aim of enhancing the noise performance of the front-end channel. The current discharging the CSA feedback capacitance is provided by the transistor M_F, whose gate potential is set to V_F. Instead of setting a direct voltage to the gate of the transistor, a solution, shown in figure 2, has been proposed which makes the architecture robust against process and temperature variations. In view of integrating the front-end channel in a pixel matrix structure, a replica of the CSA core amplifier is implemented in the matrix periphery, in such a way to track the gate-to-source voltage of the preamplifier input transistor. A 1:1 current mirror, featuring the transistors M_{FP} and M_F, ultimately provides the current I_F for the discharge of C_F capacitor. Such a discharge is mostly linear for large input signals, which push the M_F transistor in the saturation region. This architecture may actually be exploited for compensating for IR drops across the matrix as well. Assuming that the analog power is distributed along the matrix columns, the described structure can possibly be distributed along columns (1 every n pixels, not to impair the overall power consumption of the front-end) and be connected, except for $AVDD_F$, to the local $AVDD$ and $AGND$ power supplies, in order to track voltage changes along the column. A

2024 JINST 19 C12011

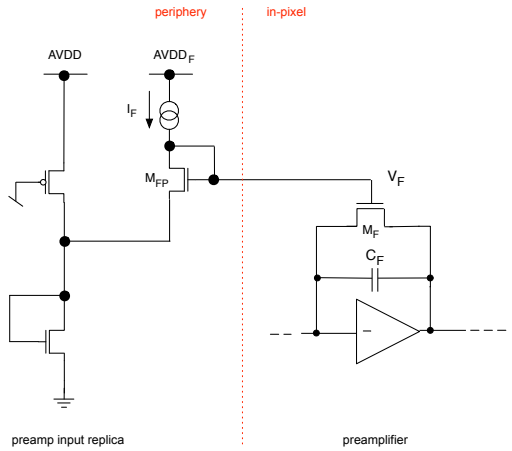

Figure 2. Schematic diagram of the circuit generating the bias for the discharge of the CSA feedback capacitance.

dedicated bias line, $AVDD_F$, provides the supply for the current mirror. Since the current I_F is of the order of tens of nanoamps, a negligible voltage drop is expected on the $AVDD_F$ line, hence a uniform discharge current can be mirrored into the pixels irrespective of their position along the matrix column.

A two stages, threshold discriminator is DC coupled to the preamplifier, comparing the signal from the CSA output with a global threshold, V_{th}. The first stage consists of a single-ended to differential signal converter, featuring a differential pair with PMOS input and diode connected NMOS load. The differential signal at the output of this stage is provided to the second stage, implemented by means of a straightforward differential pair with NMOS input and active load. An additional gain stage, featuring an inverter, provides a consolidated digital signal at the discriminator output. A dedicated line supplies power to this inverter to reduce cross-talk between the analog and digital sections of the front-end channel.

Local adjustment of the threshold is performed by means of an in-pixel digital-to-analog (DAC) converter, implemented with a binary weighted current architecture, draining the current I_{DAC} on the left or right branch of the pre-comparator stage. Such an implementation makes it possible to both increase or decrease the local threshold of the pixel, by properly configuring a suitable set of CMOS switches connected to the tuning DAC output. At the output of the comparator, a Time-over-Threshold (ToT) counter is exploited for digitization of the signal, while a Time-of-Arrival (ToA) counter is integrated for testing purposes, in particular for time-walk measurements for the front-end channel.

A current budget of 2 µA was allocated to the preamplifier stage (with an additional contribution of 200 nA for the low-power amplifier in the CSA feedback loop), while a nominal current consumption of 1 µA was set for each stage of the comparator, resulting in a total power consumption, with a supply voltage of 0.9 V, around 3.8 µW.

3 Simulation results

This section gathers the main simulation results for the front-end, with a focus on noise and threshold dispersion performance, time-walk and Time-over-Threshold charactersitics. The analog performance parameters have been evaluated for the CSA operated with the bandwidth (BW) limitation introduced by the capacitor C_{BW} connected to the preamplifier output, as discussed in the previous section (such

2024 JINST 19 C12011

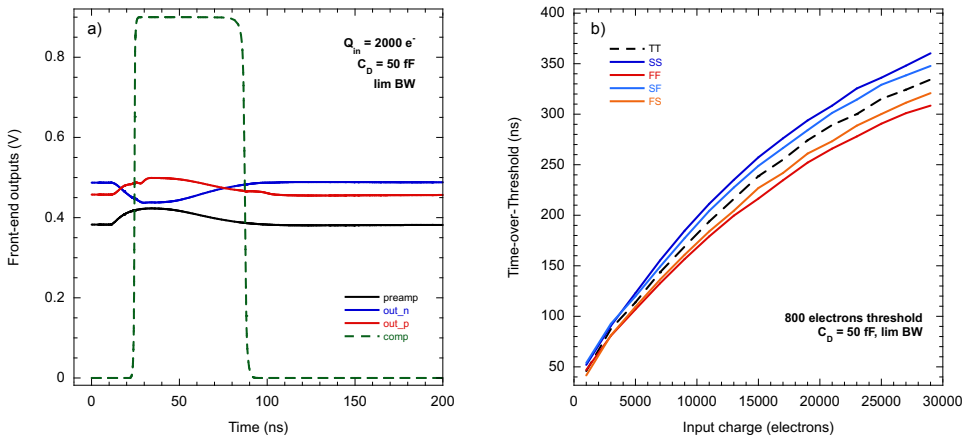

Figure 3. Front-end output signals (a) and ToT as a function of the input charge (b).

a configuration of the CSA is hereafter referred to as the *limited BW* version), and in the case of un-loaded CSA output (*regular BW* flavour).

The main outputs of the front-end are visible in figure 3a), which shows the CSA response (black waveform), together with the differential pre-comparator (red and blue curves) and comparator (dotted green line) outputs, in response to an input signal of 2000 electrons, for the limited BW configuration of the front-end operated with a threshold of 800 electrons. The Time-over-Threshold as a function of the input charge is shown in figure 3b), as a result of a four corners simulation. The ToT characteristic features an integral non-linearity close to 2% (for both the CSA configurations) for an input charge range extending to 15000 electrons.

Figure 4a) shows the simulated Equivalent Noise Charge (ENC) as a function of the detector capacitance for the two configurations of the charge sensitive amplifier. Spectre simulations were performed on the extracted view (post-layout) of the front-end channel, in the typical corner, for a temperature of -20°C, which is the expected operating temperature for the pixel readout chips at the high-luminosity upgrades of the ATLAS and CMS experiments [6]. An ENC close to 67 electrons r.m.s. was obtained for the regular BW configuration of the CSA, for a detector capacitance of 50 fF, with a noise reduction around 14% with bandwidth limitation. The equivalent noise charge was found to be well below 100 electrons r.m.s., for both the configurations, for the maximum simulated value of the detector capacitance, namely 100 fF. While, on one hand, the bandwidth limitation is beneficial from the noise standpoint, on the other hand it slows down the preamplifier response, resulting in an increased time-walk of the front-end channel. This is shown in figure 4b), where the simulated time-walk is plotted as a function of the input charge for the two configurations of the CSA. Simulations have been performed with a nominal threshold of 800 electrons, with a detector capacitance of 50 fF. It is worth mentioning that, even in the limited BW configuration, the time-walk turns out to be smaller than 25 ns (i.e. the bunch crossing period at the LHC).

Threshold dispersion properties of the front-end channel have been investigated by running a set of Montecarlo simulations, integrated into an Ocean script specifically developed for the fine-tuning of the pixel threshold. Figure 5a) shows the threshold dispersion, as obtained after the tuning, as a function of the maximum current delivered by the in-pixel tuning DAC. It is possible to notice that the dispersion, here evaluated at the comparator input (in mV r.m.s.), features a minimum for a maximum

2024 JINST 19 C12011

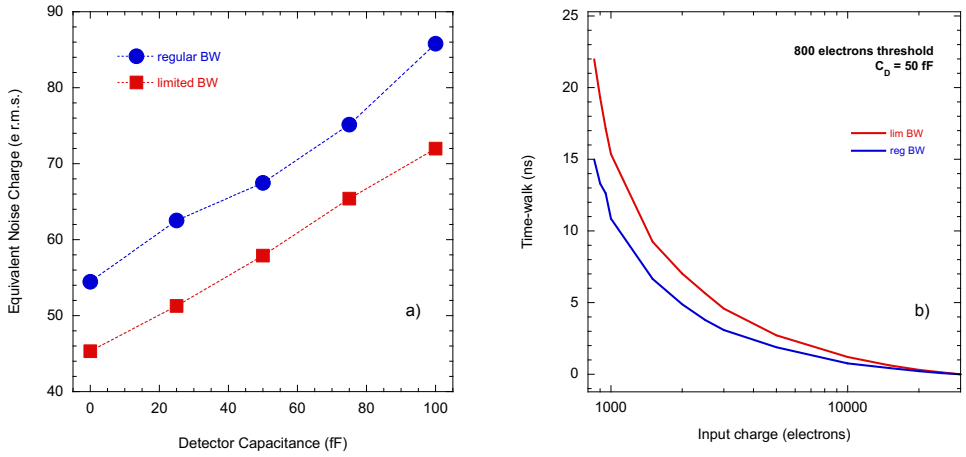

Figure 4. Equivalent Noise Charge as a function of the detector capacitance (a) and time-walk for different input charge (b). Data is relevant to both the limited and regular BW configurations of the CSA.

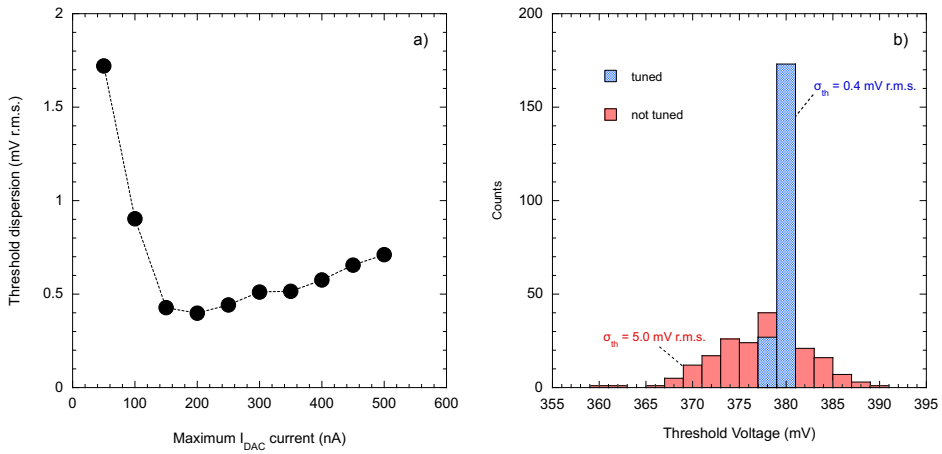

Figure 5. Threshold dispersion as a function of the maximum I_{DAC} current delivered by the threshold tuning DAC (a), and threshold distributions before and after fine-tuning of the threshold (b).

I_{DAC} close to 200 nA. Smaller DAC currents lead to an insufficient tuning DAC dynamic range, resulting in a larger threshold dispersion. The same holds for larger I_{DAC} values, which leads to a too large dynamic range (compared to the un-tuned threshold dispersion) and, hence, to an oversized LSB. The optimum threshold dispersion, around 0.4 mV r.m.s., can be easily referred to the front-end input by dividing such a value by the charge sensitivity of the channel (25 mV/ke$^-$ from circuit simulations), resulting in a dispersion close to 16 electrons r.m.s. Figure 5b) shows the threshold distributions as obtained before (red histogram) and after (blue) threshold tuning, performed with the optimum value of I_{DAC}. The ratio between the un-tuned and tuned threshold dispersion was found to be close to 12.

4 Conclusion

This work discussed the design of a 28 nm CMOS front-end channel for the readout of pixel sensors in future high energy physics experiments. The architecture described in the paper leverages the Time-over-Threshold technique for analog-to-digital conversion of the signal delivered by the sensor. The

2024 JINST 19 C12011

front-end channel includes a charge sensitive amplifier, equipped with a detector leakage compensation circuit, and a differential threshold discriminator, with an overall current consumption around 4 µA. Spectre simulations show that the front-end circuit features an equivalent noise charge smaller than 70 electrons r.m.s. (for a detector capacitance of 50 fF), with a threshold dispersion close to 16 electrons r.m.s. These results, along with simulated time-walk performance, are fully compatible with operation in the high-luminosity upgrades of the ATLAS and CMS experiments at the LHC [7]. A prototype chip, including a 8×32 matrix of readout channels featuring a size of 100×25 μm^2, has been submitted in July 2024, and the test setup for its characterization is under development.

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2024 JINST 19 C12011