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Analog Front-End for the Readout of LGAD-Based Particle Detectors

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ABSTRACT

This paper presents an analog front-end channel for the readout of Low Gain Avalanche Diodes (LGADs) based particle detectors for the next generation of space-borne experiments. The circuit has been designed in a 65 nm CMOS technology. The charge generated by the detector is integrated by a Charge Sensitive Amplifier (CSA) with dynamic signal compression feature to achieve improved noise performance, along with enhanced time resolution capabilities over the wide range of input charge to be detected (from 45 fC to 16 pC). An RC-CR shaper with selectable shaping time, a fast discriminator and a Time-to-Amplitude Converter (TAC) complete the readout circuit. An SNR around 300, together with a time resolution of slightly below 60 ps, is achieved in post-layout simulations.

1. Introduction

In space experiments, charge identification of individual cosmic-ray elements with energies greater than hundreds of GeV suffers from the presence of backscattered radiation (BS) originating from the calorimeter [1]. Indeed, the backscattered radiation degrades the detector charge resolution whenever it falls onto the same detector element traversed by the incident cosmic-ray. However, spurious signals from backscattering can be prevented by exploiting the difference in the arrival time between the incident particle and the backscattered radiation hitting the detector, being the two events separate in time. Thus, with a flight time of around 700 ps between the detector and the calorimeter, in order to efficiently reject BS to better than five sigma, front-end (FE) circuits for particle detectors should provide a time resolution better than 100–150 ps. To this end, the ADA-5D project (funded by the National Institute for Nuclear Physics, INFN, Italy) aims at the development of an innovative particle detector, consisting of arrays of Low Gain Avalanche Diodes (LGADs), featuring internal gain amplification, for the simultaneous measurement of the incident particle position (x, y and z coordinates, for tracking purposes), charge (for nucleus identification) and timing (for false signal rejection).

2. Analog front-end

Fig. 1 provides a schematic representation of the proposed FE channel for LGAD based particle detectors. When cosmic rays hit the LGAD sensor (not included in the FE), the charge generated by impact ionization is amplified by the internal gain and fed to the Charge Sensitive Amplifier (CSA), which performs a charge-to-voltage conversion. The CSA implements a dynamic signal compression feature (by taking advantage of the non-linear features of MOS capacitors [2]) to achieve improved noise performance, along with enhanced time resolution capabilities over the wide range of input charge to be detected, from 45 fC to 16 pC [3]. The CSA output signal is then fed to the shaping stage (with selectable shaping time, i.e., 10 ns, 15 ns, 25 ns and 45 ns), which implements a semi-Gaussian shaping filter of the first order (i.e., an RC-CR shaper). After the shaper, a fast discriminator and a Time-to-Amplitude Converter (TAC) have been included into the FE channel. The discriminator has been designed as the cascade of low-gain cells featuring high Gain-Bandwidth Product (GBP) to obtain a fast response, for jitter minimization. The TAC, designed in a pseudo-

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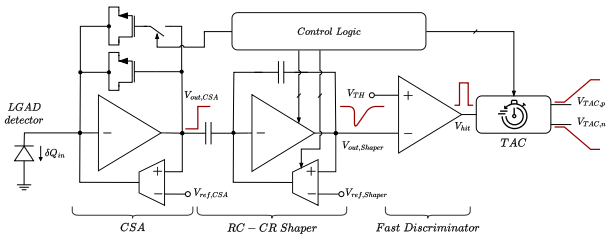

Fig. 1. Schematic diagram of the designed FE circuit.

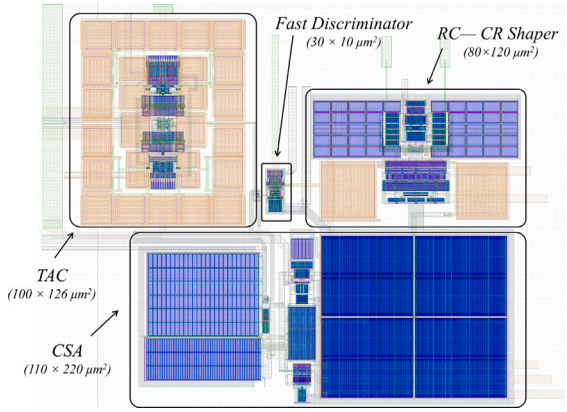

Fig. 2. Layout of the complete FE channel. It features an overall area of 240 × 270 μm² (TAC and RC-CR Shaper MIM capacitances included).

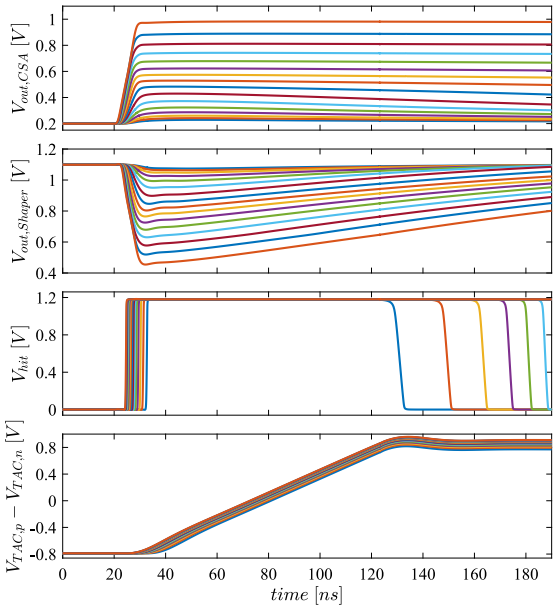

Fig. 3. Post-layout transient response of the analog FE channel to an input charge varying from 45 fC to 16 pC, with 6 steps per decade (the ratio between two consecutive steps is $\sqrt[6]{10}$). The horizontal scale is the same for all graphs.

differential fashion, consists of a pair of integrators where the feedback capacitor is charged by a constant current. Thus, when a hit is detected, a ramp-like output signal is generated at the output of the TAC. At this step, timing information on the detected event can be derived, being the output voltage proportional to the time interval between the hit detection and the trigger signal. The designed TAC can operate over two selectable Full-Scale Ranges (FSRs), namely 100 ns and 1 μs [4]. The layout of the proposed FE is shown in Fig. 2.

3. Post-layout simulation results

Fig. 3 shows a time diagram of the output of all the blocks included in the FE. In the graphs, a shaping time of 10 ns is set for the shaping stage, whereas post-layout results refer to an injected charge varying within the input dynamic range of interest. The CSA provides a trilinear response with high-gain, medium-gain and low-gain regions featuring a charge sensitivity $S_{q,h} \simeq 833$ mV/pC, $S_{q,m} \simeq 52$ mV/pC and $S_{q,l} \simeq 19$ mV/pC respectively (extracted from post-layout simulations). This behavior is obtained through an equivalent feedback capacitance varying from 1.2 pF to around 53 pF. The CSA step-like output signal features a recovery time of around 10 μs. As a consequence of the dynamic signal compression, the overall output signal amplitude increases less than linearly (as can be seen in Fig. 3, first plot from the top). Simulations show also that the rising time is within 10 ns for all the output signals, under nominal conditions as well as in all the process corners, as required by project specifications. From post-layout simulations, the discriminator features a positive slew-rate of nearly 4.2 V/ns. An Equivalent Noise Charge ENC ≤ 945 e⁻ is obtained in post-layout simulations, which leads to an SNR ≥ 300. The jitter of the overall channel up to the discriminator is around 100 ps (less than 60 ps after the TAC at 100 ns FSR and less than 180 ps at 1 μs FSR [4]), in agreement with the project specifications.

4. Conclusion

The paper discusses the design of a FE circuit capable of working over a range of input charge larger than three decades (from 45 fC to 16 pC). The CSA implementing a dynamic signal compression feature allows to achieve improved noise performance along with enhanced time resolution capabilities over the wide range of input charge to be detected. The test chip has been delivered on Q2 2024 and is now under testing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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