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Experimental results of the pFREYA16 ASIC for x-ray ptychography in continuous wave light sources

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Abstract: The pFREYA16, prototype Fast Readout for ptYchography Applications with 16 channels, ASIC is a pixellated 8-by-2 readout matrix developed for ptychography experiments based on fourth generation storage ring light sources, also known as diffraction-limited storage rings (DLSR), pushing towards continuous wave operation. The target of the experiment is to obtain a 128-by-128 matrix of pixels, working at a frame rate of 1 MHz with single-photon resolution, as well as low-noise and low-power figures, in a modest-size pixel area of 150 µm × 150 µm. The readout chain is composed of a switch-reset CSA and a semi-Gaussian unipolar RC-CR shaper, and includes signal discrimination, zero-suppression capabilities, and pixel-level analog to digital conversion. The ASIC is also configurable for 5, 9, 18, or 25 keV input photon energy, with a full well capacity of 256 equivalent photons in each mode, and four different peaking times are available for noise optimisation. The paper will focus on the characterisation of the CSA and the shaper stage.

Keywords: Front-end electronics for detector readout; Hybrid detectors; X-ray detectors

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1 Introduction

New generations of radiation light sources provide thrilling possibilities from the standpoint of the application, but pose stringent requirements on the setup employed in the experimental chamber, particularly the detector. In fourth generation storage ring light sources, also known as diffraction-limited storage rings (DLSR), in order to achieve high brilliance the trend is to use a continuous wave of tightly-spaced pulses with a low photon count each [1], in place of the free-electron laser (FEL) approach leveraging insertion devices to produce high-brilliance bunches with long separation time between one and the other [2]. This implies that detectors must comply with very fast signals at their inputs and attain zero dead-time performance.

The application of interest in the following is x-ray ptychography, that is a computational imaging technique exploiting a fast acquisition rate at the expense of a limited amount of pixels in the detector [3]. Specifically, the key idea of modern x-ray ptychography is to avoid the large overhead due to motor repositioning before scanning the impinging photon beam on the specimen under test, by continuously acquiring diffraction patterns in the detector while the specimen is scanned across the beam [4].

In this way, the typical low-throughput of x-ray ptychography is overcome. With that, the experiment can last for a shorter time, implying a smaller dose delivered to the sample under test and shorter beam time overall. More importantly, a higher throughput satisfies the requirements of typical reconstruction techniques, such as iterative phase retrieval (IPR), which needs a huge amount of diffraction patterns to properly estimate the phases from the amplitude measured, and in turn reconstruct the 2D or 3D model representation of the specimen under test [5]. The combination of high-troughput and IPR algorithms is renown to push the resolution beyond the mechanical limits of the system, typically imposed by the precision of the lenses used to focalise the impinging beam, and with that achieve a super-resolution to the nanometre scale [4].

The need to comply with new synchrotron sources, the high frame rate required by the application, together with the need of low-power, low-noise pixellated detectors to be employed in this scenario, asks for research in readout electronics, which would be the bottleneck of the chain once every other piece is in place. For this reason Argonne National Laboratory, University of Bergamo, and University of Pavia have instituted a collaboration to develop a hybrid detector for x-ray ptychography in new generation continuous wave light sources. The target of the collaboration is to develop a 128-by-128 pixellated hybrid detector that will work at 1 MHz conversion rate, with single photon resolution at 5 keV, 9 keV, 18 keV, and 25 keV photon energies, and a pixel pitch of 150 µm.

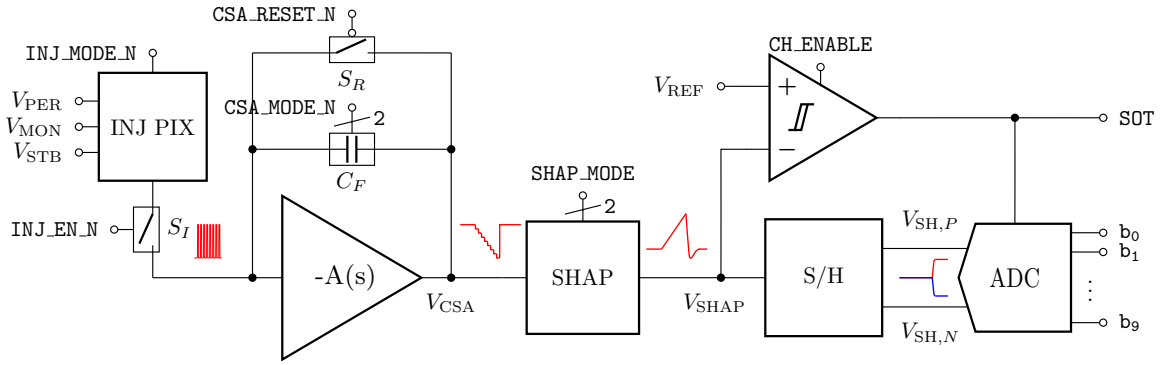

Figure 1. Block diagram of the readout channel integrated in a pixel of the pFREYA ASIC. A depiction of the signal expected at each node in the chain is provided.

A first iteration of a prototype architecture proposed by the collaboration has been designed and fabricated. The chip pFREYA, prototype Fast REadout for ptYchography Applications, developed in a commercial 65 nm CMOS technology, reports a per-pixel power consumption of 220 µW and an equivalent noise charge (ENC) of 250 e^- rms in simulation. The produced chips include two 8-by-2 matrices: one is dedicated to test structures to characterise the single blocks in the readout chain, and the other with fully-populated pixels to validate the proposal at a system level.

The paper will report the characterisation of the main analog blocks composing the pFREYA readout chain, namely the charge sensitive amplifier (CSA) and the shaper.

2 pFREYA readout channel

The readout channel integrated in a pixel of the pFREYA matrix is reported in figure 1. Starting from the left-hand side of the schematic, the in-pixel section of the distributed injection circuit (INJ PIX) is represented. This circuit mirrors an externally generated current from the periphery to each and every pixel in the matrix, if the corresponding `INJ_EN_N` bit in the configuration word is low, and steers it between the input of the channel and a peripheral monitor circuit. Leveraging the injection circuit, a continuous train of pulses with a frequency of 100 MHz is generated at the input of the channel, in order to emulate the signal coming from the DLSR. Details on the peripheral circuitry integrated in the matrix can be found in [6].

The processing chain comprises, at first, a CSA with a forward gain stage, and a feedback realised through the parallel of an array of capacitors C_F and a pair of PMOS transistors used as a reset switch S_R to discharge the integrated charge. In particular, one of the PMOS is used as a dummy to compensate for charge injection, while the other acts like the actual reset switch. The mode of the CSA is selectable through 2 configuration bits to account for 5 keV, 9 keV, 18 keV, and 25 keV photon energies. The signal expected at the output of the CSA is a downward going staircase-like signal, where each step is an integrated pulse, that returns to baseline after a controllable exposure time t_{exp}, as sketched in figure 1.

A first-order, semi-Gaussian, unipolar shaper (SHAP) follows the integrating stage. The circuit is AC-coupled and it is realised with a forward stage with a controllable dominant pole, and a feedback composed by a capacitor in parallel with a transconductance amplifier to keep the input of the gain stage stable. By tuning the capacitors in the stage by means of a 2-bit configuration, four peaking times are realisable, that are 230 ns, 330 ns, 430 ns, and 530 ns, to optimise the channel ENC, that is

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the noise of the channel reported at the input with the dimension of a charge, easier to compare with actual signals to be detected. The signal at the output of the shaper is a ramp, reaching a positive peak at t_{pp}, then followed by a lobe typical of semi-Gaussian unipolar shapers, peaking again at t_{np}.

The shaped signal is fed to both a comparator chain and an analog-to-digital (A/D) chain. The most important blocks in the first chain are a threshold generator, in which the signal is converted from single-ended to differential and a differential, tunable threshold is applied to it, and a comparator with hysteresis, to avoid bouncing at the output for very low thresholds. The chain generates a signal-over-threshold (SOT) bit which is key to reject noise-induced signals and enable zero-compression at the output, a feature that is required as the matrix will generate a data stream with a huge bandwidth, for which digital techniques are being studied [7, 8]. The second chain is comprised of a sample and hold (S/H) and an analog-to-digital converter (ADC). The S/H is a flip-capacitor-based stage with a fully-differential, rail-to-rail output, operational amplifier. It samples the two peaks reached by the shaper signal on two capacitor arrays and holds their difference at the differential outputs of the operational amplifier. The difference is also amplified by the flipping of capacitors in the arrays. The conversion to digital is performed by a 10-bit successive approximation register (SAR) ADC that receives the differential outputs of the S/H. The architecture of the SAR ADC includes mainly a differential capacitive DAC with split capacitors and a common mode logic (CML) comparator. It is designed for a 20 MHz input clock. For a detailed discussion on the comparator chain and the A/D chain one can refer to [9].

Not shown in figure 1, each pixel integrates a simple digital interface (DIG). This is needed to provide each pixel in the matrix with the slow control configuration bits, which are 7 per pixel, and to read out the digital word generated by each pixel, comprising 11 bits between the ADC ones and the SOT one. The layout of the pixels is modular, meaning that the digital interface, the digital control buses, the analog references, and power lines are contiguous when juxtaposing pixels together to build up an arbitrary-sized matrix. Digital sections were integrated in a deep N-well (DNW) and kept at a distance from the analog area so as to avoid coupling with fast digital signals. Moreover, to reduce the area usage of each block, metal-insulator-metal (MIM) capacitors have been used and integrated over the electronics when possible.

3 Experimental results

The test structure chip (pFREYATS), among others, exposes the outputs of one channel with INJ PIX and CSA alone, and one including also the SHAP. An in-chip buffer has been designed to give the option to drive the passive probes of an oscilloscope to enable direct probing of the analog chains. The following reports the main results obtained from the characterisation of the two aforementioned channels.

The transient response of the CSA in 9 keV photon mode for different equivalent photons is shown in figure 2(a), without baseline. The signal is as expected from simulation, with a downward going staircase reset after t_{exp} = 300 ns from the start of the integration. The difference between the voltage value of the baseline and the one just before the reset time is the amplitude of the CSA, which is proportional to the photons integrated during the exposure time, hereon referred to as equivalent input photons $\#\gamma_{eq}$. The reset is completed in tens of nanoseconds, but presents an overshoot that was not expected from simulation. This artifact is generated by a non proper tuning of the gain stage integrated in the test board that interfaces with the oscilloscope. The injection signal was driven by a strobe of 50 MHz instead of 100 MHz due to limitations coming from the test setup, justifying the

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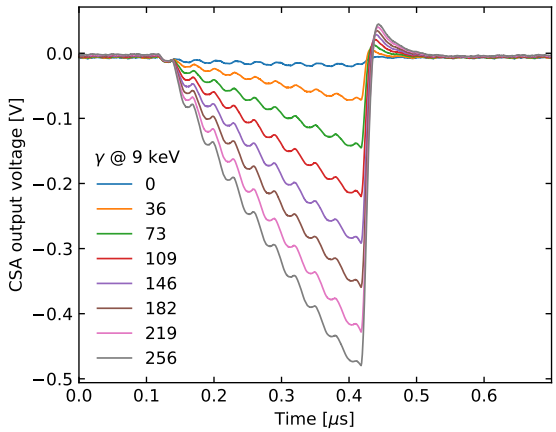
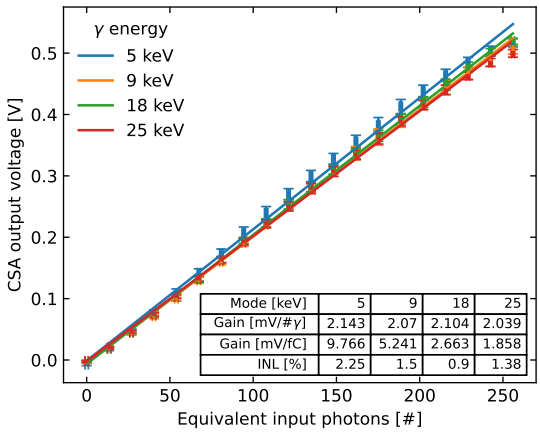


(a) Transient response of the CSA in 9 keV photon mode, stimulated by a 50 MHz train of pulses at different equivalent photons in t_{exp} = 300 ns. The baseline is removed.



(b) CSA transcharacteristics, reported for all modes, over the input dynamic range. A summary of the related figures of merit is provided in the table.

Figure 2. Results of the measurements on the CSA.

steps arrival in the staircase-like signal. The strobe is still present in the measurements when the equivalent input photon figure is zero, that is why the signal is fluctuating also for 0 $\#\gamma_{eq}$.

In figure 2(b) the transcharacteristics of the CSA is reported. The plot represent the amplitude of the CSA signal versus the equivalent photons at the input in each mode of the CSA, interpolated by means of a linear fit. The sensitivity of the CSA is consistent over the four modes and it is around 2 mV/$\#\gamma_{eq}$. The linearity is calculated as integral non-linearity (INL), adapted from the definition used for ADCs, and it is shown to be below 2.3% in each mode. The non-linearity is mainly due to the last few points in the dynamic range, which contribute a lot due to saturation effects. The linearity was an important figure to keep track of during the design, due to requirements, and the results confirm what was obtained in simulation.

The time response of the shaper, with the CSA in 9 keV photon mode and reported for every peaking time available, is shown in figure 3(a), after baseline removal. The signal is almost a ramp for the first t_{exp} = 300 ns, and then follows with a negative lobe. The behaviour of the shaper is as expected by simulation and from a typical semi-Gaussian unipolar shaper, given the CSA signal at the input as shown before. The only deviation from simulations is that the peaking times do not scale precisely as in simulations, but by correcting a voltage reference the same peaking times can be obtained. The effect of the overshoot seen in the CSA waveform is not present in the shaper one, once again justifying that the problem is related to the test board. The amplitude of the shaper is defined as the difference between the positive and the negative peak in the waveform, attained at times t_{pp} and t_{np}, which in turn define the peaking time as $t_p = t_{np} - t_{pp}$. The wiggling of the waveform is once again due to the effect of the injection strobe, as explained for the CSA.

The transcharacteristics of the CSA and shaper chain, called the analog chain, is showcased in figure 3(b). The plot represent the amplitude of the shaper output signal in a similar way as done for the CSA. The sensitivity of the chain is around 2.4 mV/$\#\gamma_{eq}$, as the shaper does not add much gain to the chain to improve linearity. The sensitivity is consistent even across peaking times. The

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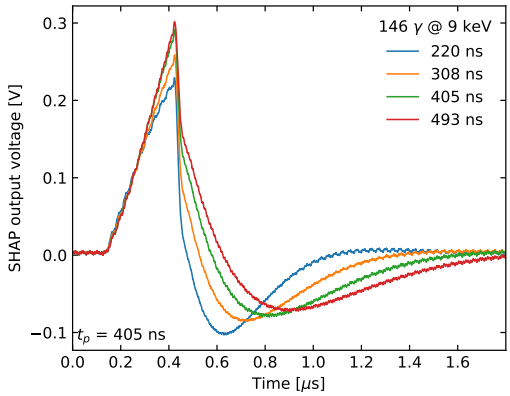
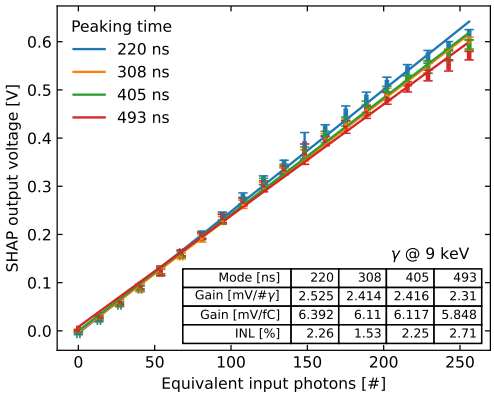


(a) Transient response of the shaper, with CSA in 9 keV photon mode and t_{exp} = 300 ns, for all the peaking times available. The baseline is removed.



Mode [ns]	220	308	405	493
Gain [mV/#γ]	2.525	2.414	2.416	2.31
Gain [mV/fC]	6.392	6.11	6.117	5.848
INL [%]	2.26	1.53	2.25	2.71

(b) Analog chain transcharacteristics, with CSA in 9 keV photon mode and for all peaking times, over the input dynamic range. A summary of the related figures of merit is provided in the table.

Figure 3. Results of the measurements on the CSA.

INL reported for this transcharacteristics is under 2.8% for each peaking time, worse than that at the CSA stage due to the non-idealities of the shaper. Overall the transcharacteristics at this point of the chain is in accordance with what expected from simulation.

4 Conclusions

A prototype of a readout chain designed for x-ray ptychography and leveraging new generation storage ring light sources has been design and produced in a commercial 65 nm CMOS technology.

The first results from measurements on the analog chain integrated in the pixel of the pFREYA ASIC have been reported. The waveforms obtained through direct probing of the output of the CSA and the shaper are in line with what expected from simulation. Furthermore, the transcharacteristics of both the CSA and the analog chain has been studied and the selected figures of merit show good agreement with simulation and are in line with the requirements.

A new test setup based on an FPGA board that generates all the digital control signals, is currently available and measurements on the rest of the test structures and the fully-populated pixels are upcoming.

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