Modeling Temperature Effects on MOS Capacitors in Charge Amplifier Feedback

Massimo Manghisoni, *Senior Member, IEEE*, Luca Ghislotti, *Member, IEEE*, Paolo Lazzaroni, *Member, IEEE*, Lodovico Ratti, *Senior Member, IEEE*, Valerio Re, and Elisa Riceputi

***Abstract*— This article discusses the effects of temperature on an inversion-mode MOS (I-MOS) capacitor. The study extends to the transfer characteristic of a charge-sensitive amplifier (CSA) featuring dynamic signal compression by implementing this device in its feedback. This technique has been adopted to read out semiconductor detectors in experiments where both high-energy resolution and a wide input dynamic energy range are crucial, such as in free electron lasers (FELs) or astroparticle physics experiments. This study presents a theoretical analysis of the relationship between MOS capacitance and temperature with a focus on how this affects the amplifier gain. Furthermore, it discusses the methodology used to design a circuit able to mitigate some of these effects. The study has been carried out in a 180-nm commercial CMOS technology, and experimental results are reported to support the theoretical analysis.**

***Index Terms*— Charge amplifier, CMOS, dynamic signal compression, temperature dependency.**

I. Introduction

CHARGE amplifiers are widely used as interfaces for various types of sensors to convert the generated charge into a proportional voltage output. The field of application includes a number of piezoelectric transducers, such as accelerometers, microphones, and pressure sensors [1]. In addition to mechanical sensors, charge amplifiers are used to interface with photosensors where photocurrent is integrated over time to produce a voltage representation of the accumulated charge [2]. In radiation detection systems, these amplifiers play a crucial role in X-ray imaging and particle tracking applications to read out the charge collected by capacitive semiconductor detectors. Over the past decades, the demand in physics experiments for high-energy resolution while maintaining a wide dynamic energy range has significantly increased. For example, in free electron laser (FEL) applications there is the need to cover a wide input dynamic range, measuring from 1 to 10^4 photons in the 1–10 keV range, while at the same time ensuring single-photon resolution at small signal levels [3]. Astroparticle physics experiments may also have the requirement to detect energies up to 100 MeV (heavy particles) while maintaining an energy resolution of a few kiloelectronvolts, for example to detect X-rays [4]. Compliance with these requirements can be achieved by adopting a nonlinear transfer characteristic of the sensor readout chain, which comes with a reduction of the channel sensitivity with the increase of the input signal amplitude.

Several strategies are reported in the literature [5], [6], [7], [8]. A solution was first proposed in [9] in which the dynamic compression is implemented at amplifier level by exploiting the nonlinear features of an inversion-mode MOS (I-MOS) used as the feedback capacitor. Here the feedback MOS acts as a varactor whose capacitance is controlled by the amplitude of the voltage step at the amplifier output and increases as the input charge increases. As a result, the amplifier gain, which is proportional to the inverse of the capacitance, decreases accordingly. The transition between the high- and low-gain region is set by the MOS threshold voltage. This solution has been successfully adopted in various projects and in designs with different CMOS technology nodes [10], [11], [12]. In the frame of the general antiparticle spectrometer (GAPS) experiment, this solution has been adopted in the design of an analog channel developed for the readout of the lithium-drifted silicon detectors used in the tracker [13]. The channel, which has been designed in a commercial 180-nm CMOS technology, is the focus of this work. One of the main concerns in the use of this compression strategy is associated with the voltage at which the compression occurs, which is determined by the MOS threshold voltage. Since this parameter is temperature dependent, the resulting transfer characteristic also varies with temperature. The purpose of this article is to discuss in detail the effects of temperature on the dynamic compression implemented with a MOS capacitor. In addition, a solution to mitigate these effects is proposed, and the experimental results are discussed.

This article is organized as follows. Section II provides a discussion on the effects of temperature on the nonlinear capacitance implemented with an I-MOS transistor. In Section III, a general discussion on the dynamic signal compression architecture under study is reported, with particular focus on temperature variation effects. In Section IV, a solution for mitigating these temperature effects is proposed and discussed. Such a solution has been implemented in an ASIC

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Massimo Manghisoni, Luca Ghislotti, Paolo Lazzaroni, Valerio Re, and Elisa Riceputi are with the Dipartimento di Ingegneria e Scienze Applicate, Università degli Studi di Bergamo, 24044 Bergamo, Italy, and also with INFN, Sezione di Pavia, 27100 Pavia, Italy (e-mail: massimo.manghisoni@unibg.it).

Lodovico Ratti is with the Dipartimento di Ingegneria Industriale e dell'Informazione, Università di Pavia, 27100 Pavia, Italy, and also with INFN, Sezione di Pavia, 27100 Pavia, Italy.

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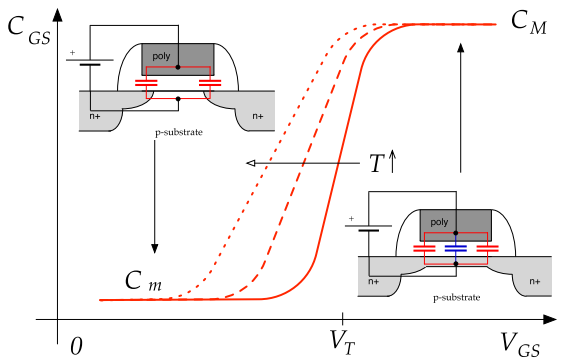


Fig. 1. Gate-to-source capacitance C_{GS} as a function of the gate-to-source voltage V_{GS} for an inversion-mode NMOS capacitor.

fabricated in a 180-nm CMOS technology, which is presented in Section V. Experimental data are included to corroborate the proposed model.

II. Modeling Temperature Effects in I-MOS Capacitor

A. I-MOS Capacitor

In a MOS capacitor, the drain and source are shorted together and form one terminal, while the gate forms the other. By tying the bulk to ground for an nMOS (the n-well to the power-supply V_{DD} for a pMOS), the device is constrained to operate exclusively in inversion mode [14]. This yields the nonlinear and monotonic C–V characteristic of the C_{GS} capacitance as a function of V_{GS}, as shown in Fig. 1. For simplicity, hereafter we will refer to an nMOS device.

For values of the gate-to-source voltage V_{GS} smaller than the threshold voltage V_T, the device operates in the subthreshold region. In this condition, the value of C_{GS} is set to its minimum C_m, which is mainly determined by the gate-to-source and gate-to-drain overlap capacitances

$$C_m \approx C_{GSOV} + C_{GDOV} = 2W\Delta L\, C_{ox} \tag{1}$$

where W is the width of the device channel, ΔL is the extension of the overlap region, and C_{ox} is the gate oxide capacitance per unit area. On the other hand, for values of V_{GS} larger than V_T, a conductive channel is formed under the gate oxide and C_{GS} shows a maximum value C_M which is mainly given by the gate-to-channel capacitance

$$C_M \approx C_m + WLC_{ox} \tag{2}$$

where L is the length of the device channel. Since the transition between low and high capacitance depends on the value of V_{GS} with respect to V_T, in the following the study is conducted considering the overdrive voltage of the MOS transistor: $V_{OV} = V_{GS} - V_T$.

B. Temperature Effects in the C–V Curve

Since the transistor threshold depends on temperature, the capacitance characteristic is also temperature dependent. V_T shows a linear dependence with the temperature and can be modeled with the following equation [15, p. 301]:

$$V_T(T) = V_{T0} - K_T \cdot T \tag{3}$$

TABLE I
MOS Surface-Charge Condition for p-Type Silicon in Inversion

ϕ_s	Surface charge condition	Surface carrier density
$\lvert\phi_s\rvert<\lvert\phi_p\rvert$	Weak inversion	$n_i < n_s < N_a$
$\phi_s=-\phi_p$	Onset of strong inversion	$n_s = N_a$
$\lvert\phi_s\rvert>\lvert\phi_p\rvert$	Strong inversion	$n_s > N_a$

where V_{T0} is the threshold voltage at 0 K and K_T is the coefficient accounting for the threshold voltage variation with temperature. Since the threshold voltage decreases as the temperature increases, the C_{GS} characteristic shifts accordingly, as shown in Fig. 1.

One of the main purposes of this work is to demonstrate that temperature also affects the slope of the transition. The slope decreases as the temperature increases, as shown in Fig. 1. To achieve this goal, we must consider that in a MOS transistor the overdrive voltage V_{OV} is related to the level of channel inversion: when $V_{OV} < 0$, the MOS is biased in the *weak inversion* region, whereas for $V_{OV} > 0$ the device operates in *strong inversion*. The transition between the two is defined as the *moderate inversion* region. In the following, we analyze the effects of temperature on the MOS inversion level and on gate-to-channel capacitance from a physical point of view. The study is carried out on a two-terminal MOS structure and then on a three-terminal MOSFET, considering a p-type silicon substrate.

1) Ideal Two-Terminal MOS Structure: The level of channel inversion can be expressed in terms of the surface free-carrier density n_s, which in turn depends on the value of the surface potential ϕ_s, with respect to the potential in the p-type region ϕ_p, as summarized in Table I [16, p. 390] where N_a is the acceptor atomic density for the p-type semiconductor and n_i is the intrinsic free-carrier density. Since the MOS device under consideration is always in inversion, the levels shown in the table are restricted to this operating condition.

In a two-terminal MOS device, the capacitance per unit area C_T is given by the series of the gate-dielectric capacitance per unit area C_{ox}, and the space-charge region capacitance per unit area C_{sc} [17, p. 8]

$$C_T(\phi_s) = \frac{C_{ox}C_{sc}(\phi_s)}{C_{ox} + C_{sc}(\phi_s)}. \tag{4}$$

C_{ox} is a constant defined as $C_{ox} = \varepsilon_{ox}/t_{ox}$, with ε_{ox} and t_{ox} being the oxide permittivity and the oxide thickness, respectively. These parameters depend only on the CMOS process. On the contrary, C_{sc} depends on the surface potential and can be determined as the derivative of the charge at the silicon surface $Q_s(\phi_s)$ with respect to the surface potential ϕ_s

$$C_{sc} = \frac{dQ_s(\phi_s)}{d\phi_s}. \tag{5}$$

The space charge per unit area at the silicon-oxide interface can be defined as follows:

$$Q_s(\phi_s) = \varepsilon_s \cdot E(\phi_s) = \sqrt{2}\frac{k_BT}{q}\frac{\varepsilon_s}{L_D} f(\phi_s) \tag{6}$$

where ε_s is the silicon permittivity, $E(\phi_s)$ is the surface electric field, k_B is the Boltzmann's constant, and q is the elementary

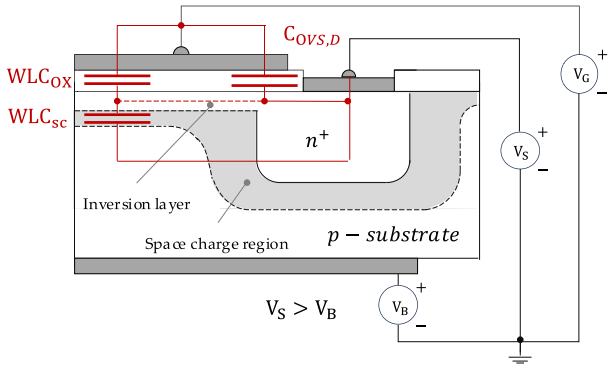


Fig. 2. Three-terminal MOS cross section, with external biases.

charge. L_D and $f(\phi_s)$ are the extrinsic Debye length and the Kingston function, respectively, and they are defined as follows:

$$L_D = \sqrt{\frac{\varepsilon_s k_B T}{q^2 N_a}} \tag{7}$$

$$f(u) = \sqrt{(e^{-u} + u - 1) + \left(\frac{n_i}{N_a}\right)^2 (e^u - u - 1)} \tag{8}$$

where $u = q\phi_s/(k_B T)$. The Kingston function provides a complete description of the variation of the surface charge in the channel in all inversion regions.

2) Three-Terminals MOS Structure: We move now to the three-terminal MOS device, as shown in Fig. 2, obtained by including the source and drain n^+ diffusions biased at a fixed voltage V_S, whereas the substrate is held at $V_B = 0$. This configuration prevents the MOS from operating in the accumulation regime. Therefore, the model can be simplified by considering, in (8), only the term $-u$ that represents the contributions to the charge of the ionized donors and $e^u - 1$ that corresponds to the contributions coming from free electrons [17, p. 6]. In moderate and strong inversion operating regions, $u = q(\phi_s - V_S)/(k_B T) \gg 1$, and (8) reduces to

$$f(\phi_s) \simeq \frac{n_i}{N_a} \sqrt{e^{\frac{q}{k_B T}(\phi_s - V_S)}} \tag{9}$$

and the surface charge can then be expressed as follows:

$$Q_s(\phi_s) = \sqrt{2} \frac{k_B T}{q} \frac{\varepsilon_s}{L_D} \frac{n_i}{N_a} \sqrt{e^{\frac{q}{k_B T}(\phi_s - V_S)}}. \tag{10}$$

By differentiating (10) with respect to ϕ_s, we obtain the expression for $C_{sc}(\phi_s)$

$$C_{sc}(\phi_s) = \frac{1}{\sqrt{2}} \frac{\varepsilon_s}{L_D} \frac{n_i}{N_a} \sqrt{e^{\frac{q}{k_B T}(\phi_s - V_S)}}. \tag{11}$$

By substituting (11) in (4) and accounting for the gate dimensions and for the overlap gate-to-source and gate-to-drain capacitances, the following expression for the total I-MOS capacitance is obtained:

$$C_{GS} = C_m + WLC_T(\phi_s). \tag{12}$$

From the previous equations, it can be noted that C_{GS} is a monotonically increasing function with respect to ϕ_s. It goes from $C_{GS} = C_m$ to the maximum value of $C_{GS} = C_M \simeq C_m + WLC_{ox}$, for $\phi_s \gg V_S$. We define ϕ_s^* as the value of ϕ_s for which $C_{sc}(\phi_s^*) = C_{ox}$. For this value of C_{sc}, the total capacitance C_T is halfway between its minimum and maximum values. The slope of the transition in ϕ_s^* is given by the following equation:

$$\left.\frac{dC_{GS}(\phi_s)}{d\phi_s}\right|_{\phi_s = \phi_s^*} = \frac{1}{4} \frac{q}{k_B T} WLC_{ox}. \tag{13}$$

Therefore, we find that the slope of the transition between the minimum and maximum value of the capacitance decreases as the temperature increases. Although the surface potential ϕ_s is not under the direct control of the gate terminal, the following relationship exists between the voltage V_G applied to the gate of the MOS device and the surface potential ϕ_s [16, p. 395]: $V_G = V_{FB} + \phi_s$, where V_{FB} is the flat-band voltage [17]. We can conclude that the slope of the capacitance transition with respect to the gate voltage decreases as the temperature increases, as shown by (13). It is interesting to note that the C_{GS} model provided by (12) can be traced back to the model proposed in [18]

$$C_{GS} = \frac{C_M + C_m}{2} + \frac{C_M - C_m}{2} \cdot \tanh[a(V_{GS} - b)] \tag{14}$$

provided that the following assumptions are adopted:

$$a = \frac{1}{4} \frac{q}{k_B T} \quad \text{and} \quad b = V_{FB} + 2 \frac{k_B T}{q} \ln\left(\frac{C_{ox}}{\frac{1}{\sqrt{2}} \frac{\varepsilon_S}{L_D} \frac{n_i}{N_a}}\right). \tag{15}$$

In the rest of the discussion, we refer to this model since the a and b coefficients provide direct information on the slope of the transition and the voltage at which the transition occurs, respectively.

III. Temperature Effects in CSAs With I-MOS Capacitor

A. CSA With I-MOS Capacitor

In charge-sensitive amplifiers (CSAs), dynamic range compression can be achieved by exploiting the nonlinear behavior of an I-MOS transistor, M_F, employed as a capacitor C_F in the amplifier feedback, as shown in Fig. 3(a). Since the gain of the amplifier, G, is inversely proportional to the feedback capacitance ($G = 1/C_F$), the nonlinear behavior of the MOS gate-to-source capacitance C_{GS} as a function of the gate-to-source voltage V_{GS} results in a nonlinear behavior of the CSA transfer characteristic [9].

For low collected charge Q_{IN}, the amplitude V_{OUT} of the voltage step at the CSA output that corresponds to the gate of the feedback I-MOS ($V_{OUT} = V_{GS}$), is sufficiently small for the device to be in the subthreshold region ($0 < V_{GS} \ll V_T$). In this condition, the value of C_{GS} is set at its minimum C_m. On the other hand, for large input charge ($V_{GS} \gg V_T$) C_{GS} shows a maximum value C_M. As a result, the CSA exhibits a value of the gain that decreases with the increase of the input charge, resulting in a transfer characteristic that is almost bilinear, as shown in Fig. 3(b). The transition between high- and low-gain regions is called *kink*, and it is defined as the intercept of the tangents to the characteristic in the two regions.

B. Temperature Effect Analysis

To investigate the effect of temperature variations on the dynamic signal compression, we consider the circuit shown in Fig. 3(c). The figure shows the simplified schematic of the amplifier described in [13], implemented in a 180-nm CMOS technology. The amplifier forward gain stage is modeled

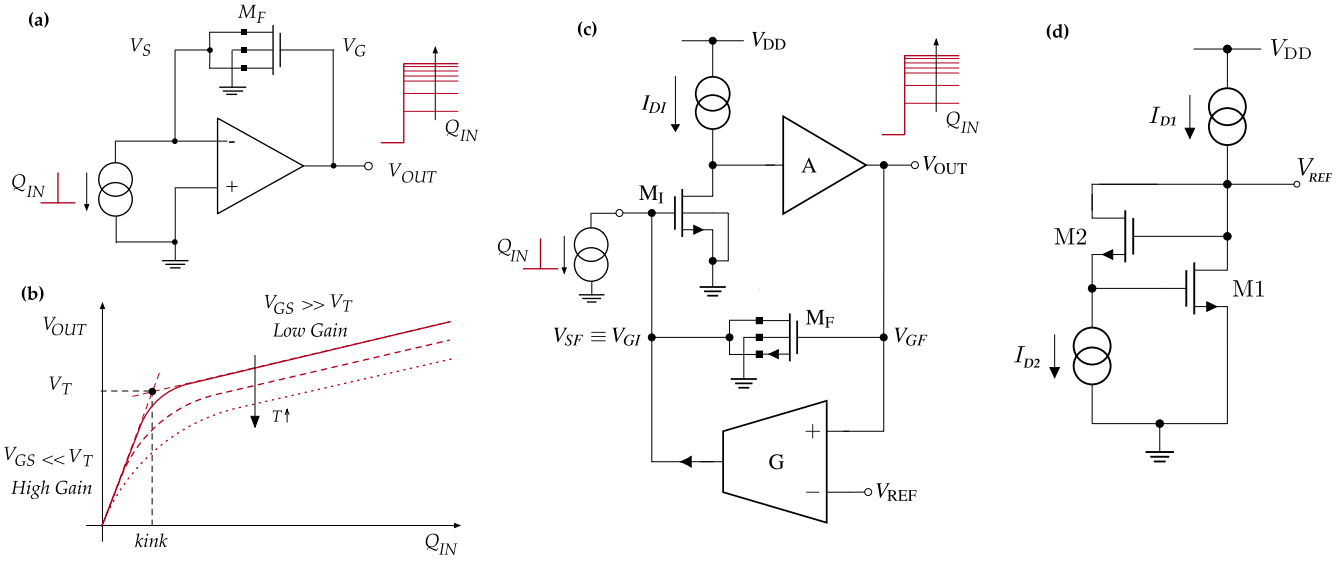


Fig. 3. (a) Simplified schematic of a CSA with a nonlinear I-MOS feedback capacitor M_F and (b) simplified transfer characteristic. (c) Simplified schematic of the CSA with dynamic signal compression architecture under study and (d) simplified schematic of the reference voltage generator.

using a common source nMOS transistor M_I, with W_I/L_I = 2400/0.5 μm, biased with a drain current I_{DI} = 1.62 mA provided by an ideal current source, and an additional stage that represents the gain introduced by the folded cascode. The feedback network is comprised of an I-nMOS capacitor, M_F, with W_F/L_F = 80/20 μm, and of an ideal transconductor for charge restoration. The transconductor is biased with an external reference voltage V_{REF} on one input. V_{DD} = 1.8 V for the 180-nm technology.

The transition between the high- and low-gain regions of the CSA depends on the overdrive voltage of the I-MOS feedback device, and the transition voltage is determined by the circuit operating point. The M_F overdrive voltage can be expressed by the following equation:

$$V_{OVF} = V_{GF} - V_{SF} - V_{TF} \tag{16}$$

where V_{GF} and V_{SF} are the gate and source voltages of the feedback MOS, respectively, and V_{TF} is its threshold voltage. Referring to the schematic in Fig. 3(c), the gate of M_F is at the same voltage level of V_{REF} for the virtual short property of the amplifier negative feedback, and its source is shorted to the gate of the input device M_I at V_{GI}. It is therefore possible to rewrite (16) as follows:

$$V_{OVF} = V_{REF} - V_{GI}(T) - V_{TF}(T). \tag{17}$$

In (17), the dependence of V_{GI} and V_{TF} on the absolute temperature T has been highlighted. Due to body-effect, V_{TF} also depends on the source-to-bulk voltage of the feedback device $V_{SBF} = V_{GI}$ [16, p. 396]. Nonetheless, it is negligible with respect to other effects, and this dependence can be neglected in the following discussion. Since the input device of the amplifier is biased in the subthreshold region, as it is typically the case in low-power front-end electronics for radiation detectors, its gate voltage can be written as [16, p. 443]

$$V_{GI}(T) = V_{TI}(T) + \frac{nk_BT}{q} \ln\left(\frac{I_{DI}}{I_{DI0}}\right) \tag{18}$$

where V_{TI} is the threshold voltage of M_I and n is the subthreshold slope factor of I_{DI}. I_{DI0} is a parameter that depends on the transistor aspect ratio W_I/L_I and on the thermal voltage $\phi_T = k_BT/q$. However, since I_{DI0} is inside a logarithmic function, the dependence of this term on temperature can reasonably be considered negligible for the rest of the discussion. The threshold voltage shows a linear temperature dependence. Therefore, V_{TF} and V_{TI} can be modeled with the following equations:

$$V_{TF}(T) = V_{TF0} - K_FT \tag{19}$$

$$V_{TI}(T) = V_{TI0} - K_IT \tag{20}$$

where V_{TF0} and V_{TI0} are the threshold voltages at 0 K, and K_F and K_I are the coefficients accounting for the threshold voltage variation with temperature. To be consistent with this notation, (18) can be rewritten in the following form:

$$V_{GI}(T) = V_{GI0} - K_GT \tag{21}$$

where $V_{GI0} = V_{TI0}$ and $K_G = K_I + nk_B/q \ln(I_{DI}/I_{DI0})$.

To validate these models, simulations of the circuit shown in Fig. 3(c) have been carried out with temperature varying from −40 °C, the operating temperature for which the CSA was optimized, to 30 °C, which is slightly higher than the ambient temperature at which the circuits are typically characterized. Results obtained with typical (TT) models are shown in Fig. 4. The linear trend of all three voltages with respect to temperature is evident, thus validating (19)–(21). The parameters extracted from the linear fit performed in the three nMOS corner models are reported in Table II. Based on these considerations, we can conclude that the overdrive voltage of the feedback device at zero input signal varies linearly with temperature, and (17) can be rewritten as follows:

$$V_{OVF}(T) = V_{REF} - V_{GI0} - V_{TF0} + (K_G + K_F)T. \tag{22}$$

Simulation results of the overdrive voltage are reported in Fig. 4. As a result, the transition point (kink) between the high and the low gain regions of the CSA transfer characteristic displaces linearly with temperature.

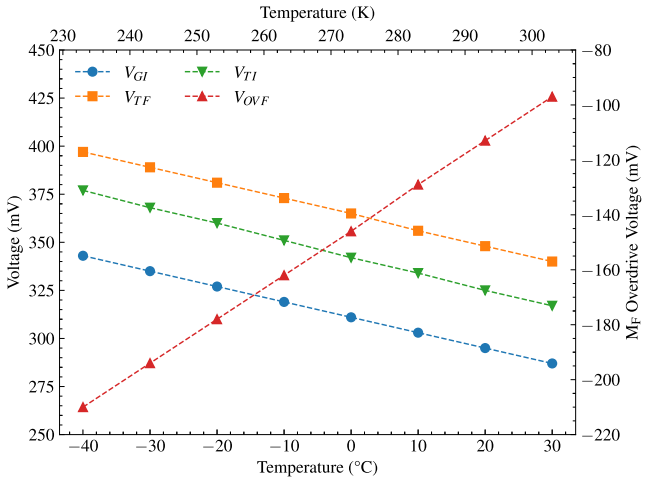


Fig. 4. Voltages V_{GI}, V_{TF}, V_{TI}, and V_{OVF} as function of temperature in the range from −40 °C to 30 °C (from −233 to 303 K).

TABLE II
VOLTAGE COEFFICIENTS

NMOS Corner Model	Fast	Typical	Slow
V_{TF0} [mV]	545	588	631
V_{TI0} [mV]	530	577	618
V_{GI0} [mV]	484	530	571
K_F [µV/K]	814	818	822
K_I [µV/K]	853	859	853
K_G [µV/K]	777	800	812
α [mV]	820	905	992
α^* [mV]	450	530	612
β [mV/K]	1.59	1.61	1.63

In addition, we have the effect of temperature on the slope of the feedback MOS capacitance in the transition region between minimum and maximum values. The slope decreases with increasing temperature, which results in a less sharp transition of the CSA characteristic between the high- and low-gain regions, as shown in Fig. 3(b).

IV. TEMPERATURE EFFECTS MITIGATION

The study conducted so far highlights that an increasing temperature has two effects on the C–V curve: a shift to the left along the X-axis, due to the reduction of the MOS threshold voltage, and a reduction in the slope, due to the dependence on temperature of the space charge at the silicon-oxide interface (both effects are technology dependent and this dependence is linked to process parameters that can be precisely controlled, such as the as dopants concentration and silicon-oxide thickness). Therefore, the temperature has two effects on the CSA transfer characteristic: a shift in the kink position and a change in the sharpness of the transition between high and low gain. Since the second effect is more difficult to compensate for, the study focuses on a circuit that generates a temperature-dependent reference voltage to mitigate the kink shift.

A. Basic Idea

To compensate for the effect of temperature on the overdrive voltage of the feedback device, the idea proposed in this work is to generate a voltage reference V_{REF} that is not fixed but which varies with temperature, so as to obtain a temperature-independent overdrive voltage. Starting from (22) one finds that the voltage reference $V_{REF}(T)$ must be composed of an independent term and a term which is linearly dependent on temperature

$$V_{REF}(T) = V_{OVF0} + V_{GI0} + V_{TF0} - (K_G + K_F) \cdot T \quad (23)$$

where V_{OVF0} is the value of the overdrive voltage at the reference temperature of −40 °C (V_{OVF0} = −210 mV in the circuit we are considering here). The equation can be written in a more compact form as follows:

$$V_{REF}(T) = \alpha - \beta \cdot T \quad (24)$$

where α and β are two temperature-independent coefficients

$$\alpha = V_{OVF0} + V_{TI0} + V_{TF0}$$
$$\beta = K_F + K_G. \quad (25)$$

Values of α and β are also reported in Table II.

In conclusion, a voltage reference $V_{REF}(T)$ that follows (24) makes V_{OVF} independent of temperature and, consequently, ensures that the CSA transfer characteristic does not vary its transition point with temperature. For the sake of simplicity, (24) has been rewritten to express V_{REF} as a function of temperature T_C in°C taking the operating temperature T_R = −40 °C as a reference

$$V_{REF}(T_C) = \alpha^* - \beta(T_C - T_R) \quad (26)$$

with α^* = 530 mV and β = 1.61 mV/°C.

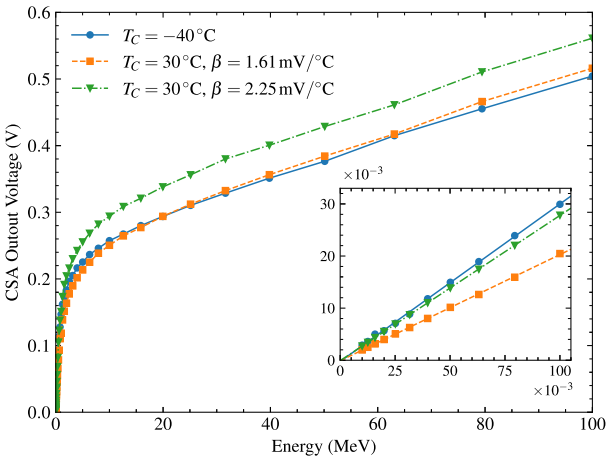


Fig. 5. Transfer characteristic of the CSA simulated at −40 °C (blue) and at 30 °C with $V_{REF}(T_C)$ generated according to (26) with α^* = 530 mV, β = 1.61 mV/°C (orange), and β = 2.25 mV/°C (green). The inset shows the range from 10 to 100 keV.

B. Simulations Results

To validate the solution proposed in Section IV-A, the transfer characteristic of the charge amplifier discussed in [13] was simulated using an ideal voltage source to generate V_{REF} according to (26). Simulations were performed at two temperatures representing the opposite limits of the range considered here. Fig. 5 shows the transfer characteristic of the CSA simulated at −40 °C (blue line) and at 30 °C with $V_{REF}(T_C)$ generated according to (26), with α^* = 530 mV and β = 1.61 mV/°C (orange line.) It can be seen that the

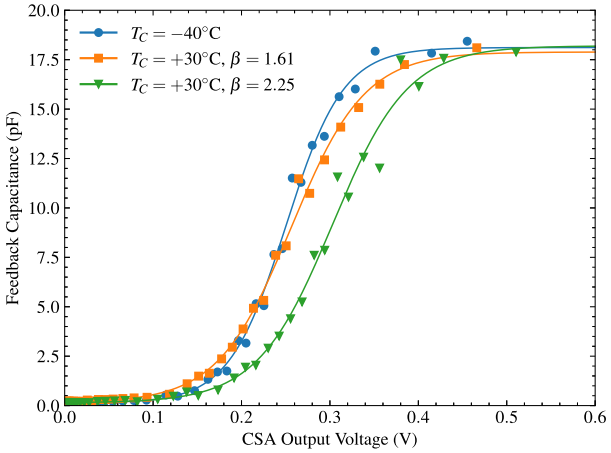


Fig. 6. Feedback capacitance extracted by differentiating the transfer characteristic of the CSA with respect to the output voltage (dots) and fit with the model proposed in [18] (lines), simulated at −40 °C (blue) and at 30 °C with $V_{REF}(T_C)$ generated according to (26) with α^* = 530 mV, β = 1.61 mV/°C (orange), and β = 2.25 mV/°C (green).

two curves are almost overlapping. To better evaluate this result, the value of the feedback capacitance, extracted by differentiating the CSA transfer characteristic with respect to the output voltage, is shown in Fig. 6. Comparing the plot at −40 °C with that at 30 °C obtained with β = 1.61 mV/°C, the transition between high and low capacitance occurs at almost the same voltage, that is, the same energy, thus confirming the effectiveness of the proposed solution. From the same plot, a change in the slope of the feedback capacitance in the transition region is evident. The slope decreases with increasing temperature, as predicted by (13). This results in a higher value at 30 °C than at −40 °C, with a reduction of the CSA gain in the low-energy region (up to 100 keV), as shown in the inset of Fig. 5. Further simulations were performed at 30 °C, and an empirical value of β = 2.25 mV/°C was found for which the curves at −40 °C and 30 °C exhibit almost the same low-energy gain, as shown in the inset of Fig. 5. However, it is evident that the complete characteristics at −40 °C and 30 °C are no longer overlapped, and the kink shifts with temperature.

To summarize the simulation results obtained by generating a temperature-dependent reference voltage according to (26), two aspects can be highlighted.

1) With β = 1.61 mV/°C, the complete transfer characteristic is almost independent of temperature, but the low-energy gain decreases as temperature increases.
2) With β = 2.25 mV/°C, low-energy gain is independent of temperature, but the transfer characteristic varies in the remaining part of the input energy range.

To highlight this behavior, the data in Fig. 6 were fit with the model in (14). The values of C_m, C_M, a, and b as extracted from data fits are reported in Table III. For each parameter, the mean value and standard deviation obtained from the Monte Carlo simulations are shown. Only process variations affect the extracted parameters, while variations due to device mismatches are almost negligible thanks to the large gate area of the feedback MOS capacitor. The values of C_m and C_M are almost identical across all settings and temperatures. Instead, the value at which the transition between C_m and C_M occurs, that is parameter b, at 30 °C matches the one at −40 °C only

TABLE III
COEFFICIENTS OF THE FEEDBACK CAPACITANCE MODEL EXTRACTED FROM DATA FITS

T_C (°C)	-40	30	30
β (mV/°C)		1.61	2.25
C_m (fF)	136±16	140±12	146±7
C_M (pF)	18.12±0.14	17.89±0.13	18.20±0.13
a (V^{-1})	15.48±0.08	12.04±0.05	11.73±0.05
b (V)	0.250±0.012	0.256±0.012	0.303±0.012

when β = 1.61 mV/°C. The slope of the transition, that is, parameter a, at 30 °C is lower than the one at −40 °C for both values of β, thus confirming the effect of temperature on the MOS capacitance discussed in Section II-B. Since maintaining the gain in the low-energy region is important for the envisioned application, values of α^* = 530 mV and β = 2.25 mV/°C are considered in the following.

As the variable feedback capacitance affects the loop gain, the stability of the circuit was carefully investigated. Simulation results show that, in the worst case scenario (when the detector is not connected to the amplifier input), the phase margin ranges from 70° with no input signal—that is, at minimum feedback capacitance—to 50° with a maximum input signal of 100 MeV—that is, at maximum feedback capacitance.

V. EXPERIMENTAL APPLICATION

In this Section we discuss the architecture adopted for the reference voltage generator and the experimental results obtained with a circuit that has been included in an analog readout channel designed in a 180-nm CMOS technology [13]. The channel is the core of a 32-channel readout ASIC developed for an astroparticle application and discussed in [19].

A. Reference Voltage Generator

As discussed in Section IV, to compensate for the effect of temperature variations on the transfer characteristic of the CSA, the reference voltage of the transconductor must vary with the temperature in accordance with (26). The circuit designed to generate this voltage, hereafter referred to as the reference voltage generator, is shown in Fig. 3(d). The voltage V_{REF} is given by the following equation:

$$V_{REF}(T) = V_{GS1}(T) + V_{GS2}(T) \tag{27}$$

where V_{GS1} and V_{GS2} are the gate-to-source voltages of transistors M_1 and M_2, which are biased with currents I_{D1} and I_{D2}, respectively, with $I_{D1} \gg I_{D2}$. Since both devices are operated in the subthreshold region, these voltages can be expressed according to (18). Therefore

$$V_{REF}(T) = V_{T1} + V_{T2} + n\phi_T \ln\left(\frac{I_{D1}I_{D2}}{I_{D01}I_{D02}}\right). \tag{28}$$

For $V_{REF}(T)$ to be consistent with (23), M_1 was designed to have a drain current density $I_{D1}L_1/W_1$ close to that of M_I so as to reproduce the variation of $V_{GI}(T)$ described by (21). The dimensions and the drain current of M_2, instead, were determined empirically to obtain a device with a threshold voltage $V_{T2} \approx V_{OVF0} + V_{TF0}$ and a threshold voltage variation

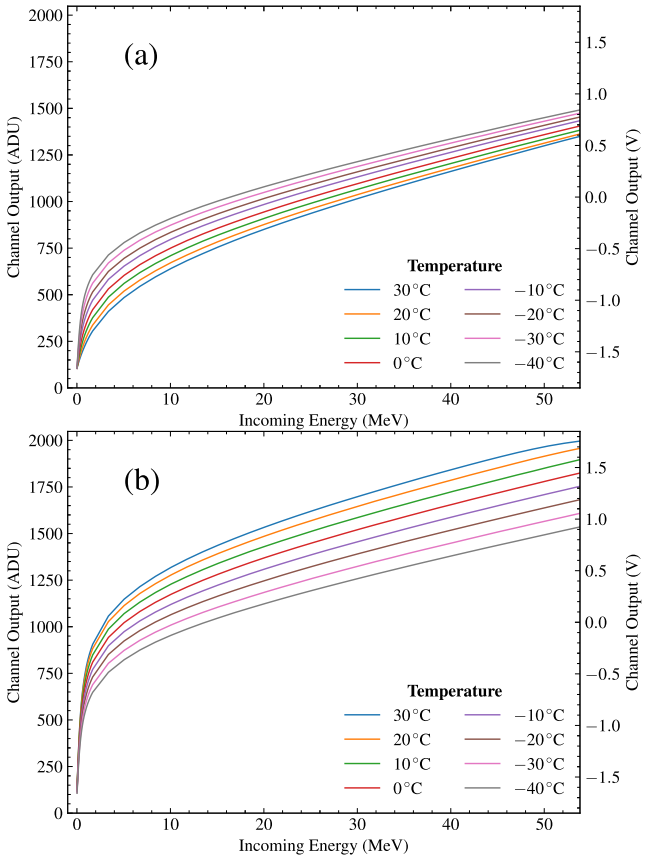


Fig. 7. Transfer characteristic of the channel measured at temperatures varying from −40 °C to 30 °C with steps of 10°C. The reference voltage is (a) constant at V_{REF} = 530 mV and (b) provided by the reference voltage generator.

with temperature $K_F T$. The goal is to achieve α^* = 530 mV, which gives V_{REF} = 530 mV at −40 °C, and β = 2.25 mV/°C, which is the optimal value to mitigate temperature effects related to the low-energy gain.

B. Experimental Results

To validate the circuit proposed in Section IV-A, the transfer characteristic of the readout channel was measured both with a constant V_{REF} = 530 mV and with the temperature-dependent one described in Section V-A. The transfer characteristic was reconstructed at the output of the 11-bit SAR ADC, with the blocks following the CSA providing an additional gain of 7.71 V/V. Measurements are provided in analog-to-digital units (ADUs). An ADU is equivalent to 1.76 mV. Measurements were performed in a climate chamber at temperatures between −40 °C and +30 °C, with steps of 10 °C.

At first, the voltage provided by the voltage reference circuit was measured as a function of T_C. As expected, the voltage decreases linearly as temperature increases. A linear fit yields α^* = 525 mV and β = 2.22 mV/°C, in line with the desired values. Fig. 7(a) and (b) report the transfer characteristics. The measurements provide the mean value calculated over the 32 readout channels available in the ASIC. Results in Fig. 7(a) were obtained with the fixed V_{REF} = 530 mV. The results in Fig. 7(b), instead, were obtained with the temperature-dependent voltage. The difference between the two datasets is evident. With a constant V_{REF}, the gain in both low- and

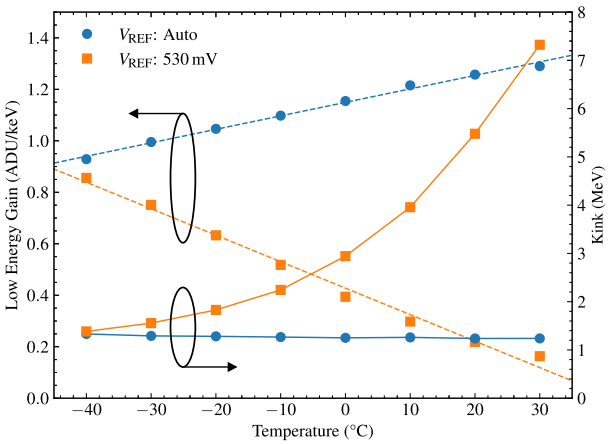


Fig. 8. Low-energy gain and kink point at temperatures from −40 °C to 30 °C with steps of 10°C for the regulated V_{REF} voltage (blue) and the one fixed to 530 mV (orange).

high-energy regions varies significantly, and the energy at which the transition begins also shifts. When the temperature-dependent reference voltage generator is used, only a shift of the curve in the high-energy region is observed, in agreement with the chosen value of β.

The gain in the low-energy range (10–100 keV) was extracted as the slope of the linear fit. Results are reported in Fig. 8. With fixed V_{REF}, the gain decreases by approximately 80% going from −40 °C to 30 °C, with −0.012 ADU/keV/°C (−21 μV/keV/°C). With V_{REF} provided by the reference voltage generator, the gain instead increases by about 40% over the same temperature range, with a slope of 0.004 ADU/keV/°C (7 μV/keV/°C). The variation is still not negligible, but it is half that obtained with a constant V_{REF}.

To complete the analysis, the kink point, corresponding to the energy at which the transition between the high and low gain regions occurs, is evaluated. Values of the kink point extracted for temperatures ranging from −40 °C to 30 °C are shown in Fig. 8. When the reference voltage varies dynamically, the kink remains nearly constant, with a variation of only about between −40 °C and 30 °C points. Conversely, when the reference voltage is fixed at 530 mV, the kink undergoes a 429% variation between the two temperature extremes. These results confirm the effectiveness of the proposed circuit in compensating the temperature dependence of the CSA transfer function.

As a final step, the effect of temperature on the slope of the transition between the minimum and the maximum value of the feedback capacitance was evaluated. Fig. 9 shows the equivalent feedback capacitance as a function of the CSA output voltage, obtained from the transfer characteristics of the CSA shown in Fig. 7(b). The plot clearly shows that the slope of the transition decreases as the temperature increases, in agreement with the behavior predicted by (13). The same holds for the plots obtained with a constant reference voltage. The slope of the curves was extracted from the plots of the equivalent feedback capacitance as a function of the CSA output voltage, at the midpoint of the transition. These values are reported as a function of the inverse of the absolute temperature, as shown in Fig. 10. In agreement with (13), the slope exhibits a linear dependence on $1/T$ with a proportionality coefficient given by $1/4q/k_B W_F L_F C_{ox}$. By fitting these data with a linear function, it is possible to extract

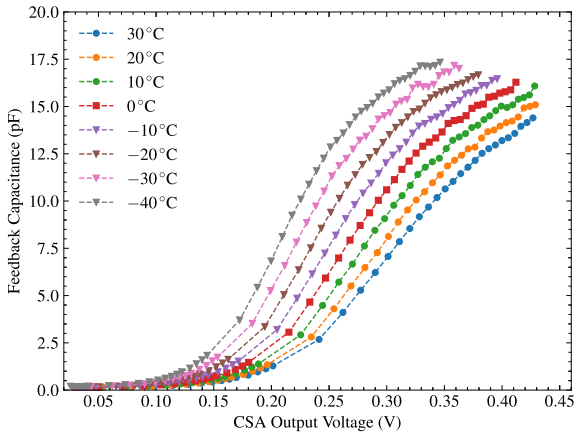


Fig. 9. Equivalent feedback capacitance as a function of the CSA output voltage obtained at temperatures from −40 °C to 30 °C with the reference voltage provided by the reference voltage generator.

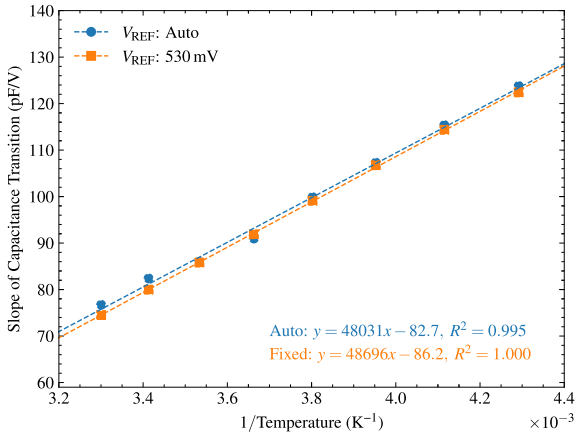


Fig. 10. Slope of the transition between minimum and maximum of the equivalent capacitance at the CSA output voltage corresponding to the midpoint of the transition. Values are reported as a function of $1/T$.

the gate-oxide capacitance per unit area C_{ox}. A value of $10.50 \pm 0.07\ fF/\mu m^2$ is obtained from the measurements with a constant V_{REF}, and $10.36 \pm 0.28\ fF/\mu m^2$ from those using the reference voltage generator. These values are close to that of 8.41 fF/μm^2 expected for the 180-nm CMOS technology node [20, p. 42], thus confirming the validity of (13).

VI. Conclusion

This work presented a study of the effects of temperature on MOS capacitors operated in the inversion mode. The proposed model was applied to the transfer characteristic of a CSA. The stage features dynamic signal compression by exploiting the nonlinear behavior of the MOSFET used as a feedback capacitance. The study highlighted that temperature has two effects: one on the threshold voltage, which in turn determines the energy value at which the transition between the two gain regions occurs, and the other on the slope of the transition of the equivalent capacitance between the minimum and maximum values as a function of voltage. A circuit capable of mitigating the first of these two effects has been proposed, and its effectiveness has been validated through experimental measurements.

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