



OBELIX: A monolithic pixel sensor with triggered readout for the Belle II upgrade

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ABSTRACT

The Upgrade of the Belle II vertex detector (VTX) at the SuperKEKB accelerator in Japan is foreseen to improve tracking performance at the expected high beam backgrounds at target luminosity of $6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$.

The OBELIX-1 chip is specifically developed for this purpose and used as sensor on all VTX layers. OBELIX-1 is a depleted monolithic active pixel sensor in 180 nm technology. The pixel matrix is inherited from TJ-Monopix2, but the periphery of the chip is entirely reworked. A newly designed 2-stage pixel memory matches

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OBELIX

Belle II trigger requirements. OBELIX-1 includes LDO regulators and a precision timing module with less than 3 ns resolution. Furthermore, the chip can also contribute to the Belle II trigger system with low latency, low granularity real-time streaming of pixel data in parallel to regular operation.

Details of the inner working of the trigger memory are presented, as well as performance simulations to validate the requirements for the VTX Upgrade. The trigger memory has been studied in simulation using realistic scenarios, including Landau distributed charge and clustering to evaluate performance.

In order to allow post-production testing, an additional module is presented. This allows the injection of pseudo-random data early in the processing chain, and replaces the need for industry standard scan-chains. It can be used stand-alone or during analog charge injection, in order to reach the full trigger memory during testing.

1. OBELIX-1 chip

Inheriting the pixel matrix and parts of the control logic from TJ-Monopix2 [1,2], the OBELIX-1 chip [3] is being developed currently for the upgrade of the Belle II vertex detector [4,5].

The floorplan of the OBELIX-1 chip is shown in Fig. 1. The pixel matrix is extended to 896×464 pixels at the same pitch of $33.04 \mu\text{m}$ as in TJ-Monopix2. The hit time-stamping has a bin size of 47 ns and 7 bit Time over Threshold (ToT) measurement. The analog amplifier contains a clipping transistor. The bias voltage on this transistor effectively allows to set a saturation value of the maximum ToT, implementing a flexible way of ToT clipping.

To compensate for voltage drop in the supply rails in the final detector, low dropout regulators are developed, allowing an increased range of 2 to 3 V for the digital and analog power domains [6]. Across the chip area a total of 32 temperature measurement cells and 16 supply voltage sensing cells are placed to allow the assessment of temperature gradients and IR drop.

The digital periphery includes the trigger unit (TRU), a dual stage memory capable of buffering data for chip-operation with an external trigger. The TRU is designed to operate at pixel hit-rates of up to $120 \text{ MHz}/\text{cm}^2$ at a nominal latency of $10 \mu\text{s}$ and a nominal trigger rate of 30 kHz.

Furthermore, a precision timing module allows a time resolution of under 3 ns at increased power consumption and hit-rates below $10 \text{ MHz}/\text{cm}^2$ when switched on via configuration [7]. This is acceptable in the outer layers of VTX and allows the time annotation of reconstructed tracks.

A second data output allows the low-latency transmission of low-granularity hit-data to enable the VTX detector to contribute to the Belle II trigger decision. [8]

2. The trigger unit

The trigger unit is organized into 112 Trigger Groups (TRG), each trigger group is responsible for the readout of 4 double columns (DCs) as shown in Fig. 2.

Inside each TRG, the hit-data from the columns are read out by four end of column controllers (EoCs) and the leading edge timestamp is extended by two bits. This increases the overflow time from $6 \mu\text{s}$ to $24 \mu\text{s}$. Subsequently, the four data streams combined into a single one via a round robin arbiter. This arbiter can also read out the peripheral time-to-digital converter module (PTD) or the Digital Injection (DI) module selectively. The EoC controller is capable of slowing down the readout in case of data congestion, effectively using the pixel matrix as additional buffer memory. Neither the PTD nor DI modules are capable of retaining data in a similar way, and therefore a FIFO of size 4 is included in this data path.

After the round robin arbiter, the data is stored in the two stage trigger memory. Stage 1 (S1) is based on an SRAM cell from the technology and configured as a FIFO with space for 128 hits. Stage 2 (S2) performs the actual association with the triggers. To do this, the Leading edge (Le) timestamp in each of the 32 storage cells is continuously compared to a counter. This counter is synchronous to the current timestamp

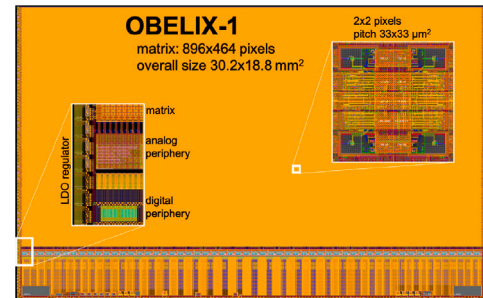


Fig. 1. Floorplan of the OBELIX-1 chip.

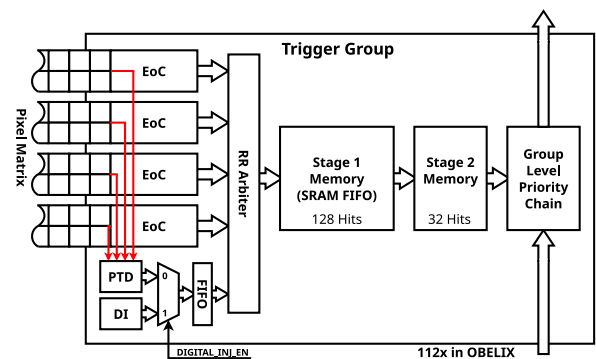


Fig. 2. Block diagram of one TRG block.

S2 Storage Cell FSM

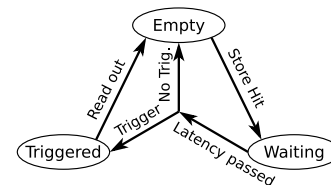


Fig. 3. Finite state machine in each storage cell of S2 in triggered mode configuration.

counter, but delayed by the configurable trigger latency. A matching Le therefore means, that this hit passed its latency and is ready to be processed. If a trigger command is received, the currently processed hits are marked as triggered. If no trigger is received, these hits are discarded and the space is filled by pulling data from S1. Hits that are marked as triggered are subsequently read from S2 and forwarded to the transmission unit. This state machine, present in each storage cell of S2 is shown in Fig. 3.

The two stage design is necessary to allow the design trigger latency of $10 \mu\text{s}$ while reducing power and area consumption via the use of SRAM blocks. The pixels release hits after detecting the trailing edge. This means that the hit-data in the data-stream is not ordered chronologically. Since typical maximal ToT values are around $3 \mu\text{s}$, this creates a local time disorder of the same magnitude.

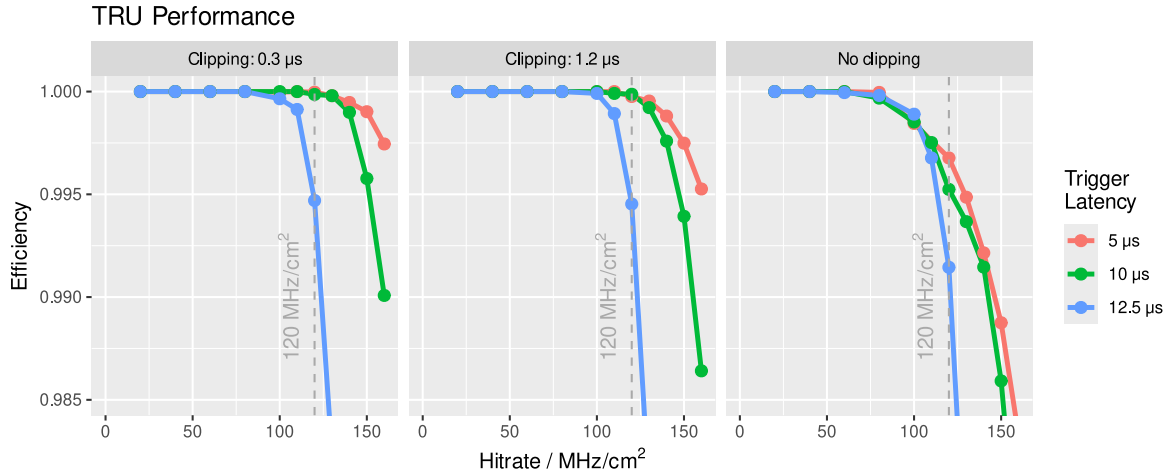


Fig. 4. Results of performance simulation of the trigger unit depending on trigger latency and ToT clipping.

In order to be processed correctly, all hits of a certain event need to reside in S2 when the latency passes, which in turn means that typically the last 1/3 of the trigger latency of each hit needs to be spent in S2. This explains the sizing of the memories, and has been verified with simulations.

2.1. Performance simulation

Extensive simulations have been performed to evaluate the performance of the trigger unit. The algorithm simulates the charge deposition in silicon using a Landau distribution and a cluster decomposition is performed. Subsequently, the resulting charge is converted to ToT and the arrival timing is calculated using a model of the matrix.

The performance simulation was conducted for three different ToT clipping scenarios and results are shown in Fig. 4. In the no-clipping case, the tail of the Landau distribution occasionally creates hits with very long ToTs. This creates losses at high utilization, because these hits might not reach S2 in time, since they appear late in the data stream. With moderate clipping to $1.2\ \mu\text{s}$, the losses to this kind of overflow are below 0.01% at target latency of $10\ \mu\text{s}$ and design hit-rate of $120\ \text{MHz}/\text{cm}^2$. Even higher hit-rates can be tolerated with the extreme clipping of $0.3\ \mu\text{s}$, effectively leaving the chip in binary charge resolution.

Fig. 4 also shows the results for trigger latencies of $5\ \mu\text{s}$ and $12.5\ \mu\text{s}$. For the latency settings of $5\ \mu\text{s}$ and $10\ \mu\text{s}$, the S2 size is the limiting factor, and therefore stronger clipping allows for higher hit-rates. On the other hand, with $12.5\ \mu\text{s}$, the total capacity of S1 and S2 combined is the limiting factor and strong clipping cannot recover the performance.

3. Design for test strategy

Commercial CMOS chips typically rely on scan chains to verify that the final circuit is operational and to filter out the chips with defects. However, the overhead is significant and in a strongly power- and space constrained application like a high energy physics experiment, alternative solutions need to be developed.

In particular, 90% of the area in the digital periphery is occupied by the trigger unit and especially memory cells. Without the access from a scan chain, the tests need to operate the chip in nominal conditions and verify the results. This requires significantly more time in testing.

Using the charge injection circuit, the full data path of OBELIX-1 can be tested, starting from the analog amplifier in the pixels over the readout of the matrix, the trigger unit, and transmission over the LVDS output. However, the trigger unit is designed for hit-rates of

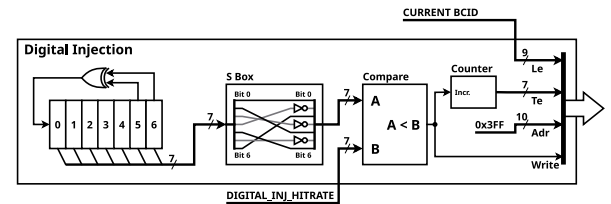


Fig. 5. Block diagram of the DI module.

$120\ \text{MHz}/\text{cm}^2$ whereas the injection circuit typically operates in the range of kHz.

With a bandwidth utilization of less than 1% alone, the test coverage of the trigger unit would be very poor. An additional circuit is therefore included, allowing the injection of hits before stage 1 in the digital domain.

The DI module contains a pseudo random number generator based on a 7 bit Fibonacci linear feedback shift register as shown in Fig. 5. The value of the shift register is rearranged using a substitution box (S Box) and compared against a configurable threshold. If the resulting number is smaller than the threshold, a hit is injected into the data stream. The leading edge timestamp corresponds to the current timestamp, the trailing edge timestamp contains a sequence number, incremented with each injected hit. The row address is set to 1023 which does not correspond to any physical pixel in OBELIX-1.

Each trigger group contains the same DI module, with the shift register initialized to a different starting value. The sequence contains 127 steps (all binary values except all-zero) and each DI module is initialized to a different starting value by default. Alternatively it is possible to individually set a starting value for each DI module.

The threshold therefore allows an injection frequency of integer multiples of $1/127$ of the timestamp clock frequency. This corresponds to a hit-rate resolution of $4.13\ \text{MHz}/\text{cm}^2$.

4. Conclusion

In summary, the trigger unit of the OBELIX-1 chip demonstrates robust handling of high hit-rates, however, under high load scenarios moderate clipping of the ToT is necessary for optimal performance. The inner structure and design decisions are explained in detail.

The introduction of the Digital Injection (DI) module replaces the industry standard of scan chains and is sufficiently scalable to $O(1000)$ chips necessary to build the VTX detector. It allows deterministic tests of the trigger unit memory by adding pseudo-random hits early in

the data flow. This can either be used stand alone or for even higher coverage simultaneously with an analog charge injection into the pixel matrix.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

- [1] K. Moustakas, *Design and Development of Depleted Monolithic Active Pixel Sensors with Small Collection Electrode for High-Radiation Applications* (Ph.D. thesis), Rheinische Friedrich-Wilhelms-Universität Bonn, 2021.
- [2] C. Bespin, et al., Timing performance of a monolithic CMOS pixel detector front-end in 180nm technology, *PACET* (2024) 1–4, <http://dx.doi.org/10.1109/PACET60398.2024.10497069>.
- [3] T.H. Pham, et al., Design of the OBELIX monolithic CMOS pixel sensor for an upgrade of the Belle II vertex detector, *J. Instrum.* 19 (04) (2024) C04020, <http://dx.doi.org/10.1088/1748-0221/19/04/C04020>.
- [4] T. Abe, et al., Belle II technical design report, KEK Rep. 1 (2010) <http://dx.doi.org/10.48550/ARXIV.1011.0352>.
- [5] H. Aihara, et al., The Belle II detector upgrades framework conceptual design report, 2024, [arXiv:2406.19421](https://arxiv.org/abs/2406.19421).
- [6] R. Boudagga, et al., Design of the OBELIX monolithic CMOS pixel sensor for the Belle II vertex detector upgrade, *J. Instrum.* 20 (02) (2025) C02046, <http://dx.doi.org/10.1088/1748-0221/20/02/C02046>.
- [7] M. Babeluk, et al., The DMAPS upgrade of the Belle II vertex detector, *Nucl. Instrum. Meth. A* 1064 (2024) 169428, <http://dx.doi.org/10.1016/j.nima.2024.169428>.
- [8] M. Babeluk, et al., The OBELIX chip for the Belle II VTX upgrade, *Nucl. Instrum. Meth. A* 1067 (2024) 169659, <http://dx.doi.org/10.1016/j.nima.2024.169659>.