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**School of Engineering**
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*Doctoral Programme in Engineering and Applied Sciences*

**CYCLE XXIX**


# Intelligent systems for particle detectors in environmental applications and High-Energy Physics

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**December 2016**

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# Abstract

Over the last decades, improvements in microelectronics technology have fostered significant progress in all fields of engineering, science and also in radiation detection. The main challenge in designing radiation detectors is to develop systems based on front-end electronics that is able to cope with high radioactive environment, satisfy very high resolution requirements and comply with high particle rates. This thesis work focuses on the analysis and development of novel and intelligent solutions for electronics system, especially suited for radiation detectors. In particular, two different applications are considered here.

The first one concerns the design of a portable and affordable detector system for continuous indoor Radon detection, based on SiPM technology. A simple analog front-end with optimized low-noise performances and reduced power consumption has been designed for counting each alpha particle that occurs in the detector after Radon decay. The readout electronics is integrated with a suite of environmental sensors on a full-custom Printed Circuit Board. Compared to all the commercial Radon detector nowadays available, the developed system is able to detect reliable value of indoor Radon concentration within few hours. The system also exploits the recent capabilities of microelectronic devices by including advanced functions such as Bluetooth data transmission and energy harvesting.

In high-energy physics experiments, with particular emphasis on the HL-

LHC environment, pixel detectors have to satisfy aggressive requirements concerning high granularity, high rate capability and low power consumption. With the advent of accessible modern technology such as 65 nm CMOS, the processing speed and reduced power consumption can be achieved. In order to meet such specifications, a new pixel mixed signal ASIC has been designed as a prototype front-end for the HL-HLC pixel readout system, within the framework of RD53 collaboration. The ASIC front-end includes signal processing and synchronous analog-to-digital conversion within one Bunch Crossing period. Thus, the emphasis of the work is on the feasibility of a synchronous ADC within the HL-LHC environment, able to ensure high performances in terms of low noise, power dissipation and high speed. Finally, a novel and intelligent digital architecture has been proposed, in order to focus the efforts of the front-end on the implementations of three main features: a novel data sparsification method, a clusterization scheme at the hardware level itself and fast Region-Of-Interest (ROI) trigger capability.

The manuscript is organized in three chapters. The first one introduces the motivations and main challenges related to radiation detectors in various applications, such as high energy physics experiments, medical digital imaging and space science. Then, the second chapter describes the system developed for indoor Radon detection. In particular, it discusses the motivations that lead to such design, along with an overview on Radon origins and common measurements techniques. It also presents the system requirements and goals before explaining the front-end and Printed Circuit Board design. In addition, preliminary measurements are provided in order to demonstrate the feasibility of the developed intelligent system. The last chapter is devoted to the design and preliminary characterization of pixel front-end Application Specific Integrated Circuit, developed as a prototype front-end for the innermost layer of CMS detector and submitted in June 2016. The first section of this chapter provides an overview on HL-LHC environment, along with details on system requirements. Then, it describes a conceptual operating principle of the synchronous ADC and its advantages and implementation technology. Finally, a detailed explanation over the transistor level and layout design of the front-end is provided along with preliminary test results.

# Acknowledgments

First of all, I gratefully acknowledge my advisor Prof. Valerio Re for believing in me since the beginning of my PhD work, for his guidance, supervision and support during these three years.

I would like to thank Prof. Aurore Savoy-Navarro for her helpful support. She gave me the opportunity to work in a very interesting and stimulating scientific environment.

I owe special thanks to Lorenzo Fabris at Oak Ridge Laboratory (Tennessee, USA) for his fundamental contribution in designing the analog front-end section of the Radon detector, as well as in performing most of the simulations related to the detector. In particular, my gratitude to him goes for all the knowledge he shared with me, and also for his support and valuable technical assistance.

To Luigi Gaioni at University of Bergamo goes my deepest gratitude for the immense knowledge he shared with me about the Integrated Circuit design, as well as for his continuous support, his kind availability, for his patience and encouragement.

I want to thank my colleagues from microelectronics laboratory of University of Bergamo, for their support. In particular to Prof. Gianluca Traversi, Prof. Massimo Manghisoni, Michele Caldara, Francesco De Canio, Daniele Comotti, Michael Galizzi, Patrick Locatelli and Elisa Riceputi.

Special thanks for the great and funny time I spent with them during these last months to Alvin Sashala Naik (Merci!), Leônidas Fernandes do Prado

(Obrigada!), Sergei Lapin and Anton Bogachev (спасибо!) and Chenfan Zhang (Xie Xie!), my colleagues from Astroparticule et Cosmologie laboratory (APC) at University Paris Diderot.

Last but not the least, I would like to thank my parents, my two sisters Miriam and Valeria and all my friends, near and far, for cheering and support me during all these years.

*The research leading to these results has received funding from the People Programme (Marie Curie Actions) of the European Union's Seventh Framework Programme FP7/2007-2013/ under REA grant agreement n [317446] INFIERI "INtelligent Fast Interconnected and Efficient Devices for Frontier Exploitation in Research and Industry".*

CHAPTER 1

# Introduction to particle detectors

## 1.1 Motivation

In general, a *particle detector*, also known as a radiation detector, is defined as a device designed for the detection, tracking and/or identification of ionizing particles, in a multitude of environments and applications. Such subatomic particles are those emitted by radioactive materials, produced by particle accelerators or observed in cosmic rays. They include: electrons, protons, neutrons, alpha and beta particles, gamma rays, and numerous mesons and baryons. In experimental and applied particle physics, nuclear physics, and nuclear engineering, detectors can measure the particle energy and other properties such as momentum, spin, charge, in addition to merely registering the presence of the particle. Most detectors utilize in some way the ionization produced when these particles interact with matter. The first question that arises when dealing with particle detectors is the following: *why do we need radiation detectors?*

In physics, radiation is defined as the emission or transmission of energy in the form of waves or particles through space or through a material medium. This includes:

- Electromagnetic radiation: radio waves, visible light, x-rays, and gamma radiation ($\gamma$);
- Particle radiation: alpha radiation ($\alpha$), beta radiation ($\beta$) and neutron radiation;
- Acoustic radiation: ultrasound, sound, and seismic waves (dependent on a physical transmission medium);
- Gravitational radiation that takes the form of gravitational waves, or ripples in the curvature of spacetime.

Figure 1.1 shows the radiation spectrum for most commonly encountered types of radiation.

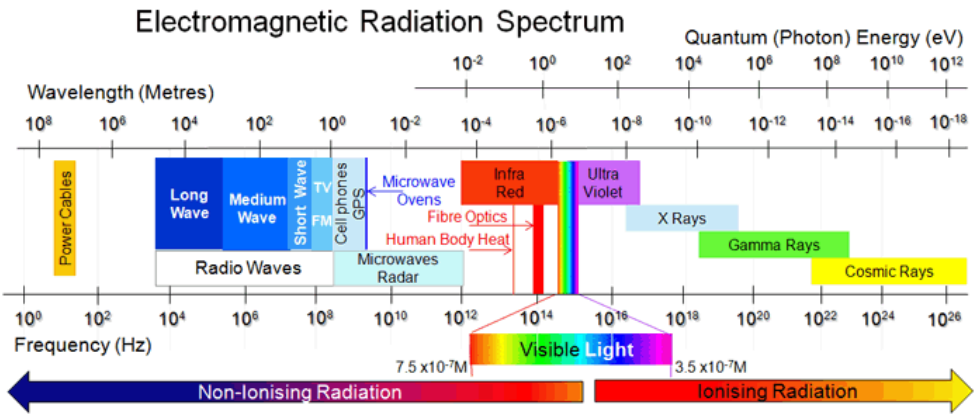



Figure 1.1: Common electromagnetic spectrum.

In general, radiation is categorized as either ionizing or non-ionizing depending on the energy emitted by the radiated particles. In particular, ionizing radiation carries more than 10 eV. Such an energy is enough to ionize atoms and molecules, and break chemical bonds. This is an important distinction due to the large difference in harmfulness to living organisms. A common source of ionizing radiation is radioactive material that emits $\alpha$, $\beta$, or $\gamma$ radiation, that respectively consist of helium nuclei, electrons or positrons and photons. Other radiation sources include X-rays from medical radiography examinations and secondary cosmic rays, such as muons, mesons, positrons, neutrons and other particles. Such secondary cosmic rays are produced after primary cosmic rays interaction with Earth's atmosphere. Gamma rays, X-rays and

the higher energy range of ultraviolet light constitute the ionizing part of the electromagnetic spectrum. On the other hand, the spectrum including visible light, infrared light, microwaves, and radio waves represents the non-ionizing part. The non-ionizing radiation is characterized by lower-energy and longer-wavelength. Its main effect when interacting with tissue is heating. This type of radiation only damages cells if the intensity is high enough to cause excessive heating. Radiation with sufficiently high energy can remove electrons from atoms and create ions. In more details, ionization phenomenon occurs when an electron is stripped from an electron shell of the atom, leaving the atom with a net positive charge. In most of the cases, exposure to ionizing radiation is considered the most important cause of genetic damage, and thus cancer, risk increasing. Indeed, the living cells and specially their DNA can be damaged by the ionization.

Starting from these considerations, is easy to deduct that particle detectors are important devices for personal safety, since ionizing radiation cannot be seen, smelled, heard, tasted, thus is not perceptible. For this reason, routine radiation surveys are required to ensure that radiation exposures are maintained as low as reasonably achievable. In particular this is relevant in such work areas for certain occupations, working with and/or in presence of radioactive materials (mines, cleanup workers, nuclear and medical workers, etc).

However ionizing radiation has many practical uses in medicine, research and construction, but, as explained above, it presents a health hazard if used improperly. As an example, medical diagnostic and therapy procedures used to define and diagnose medical conditions are currently the greatest manmade source of ionizing radiation exposure to the general population. Such a radiation is adopted to generate images of the human body in many types of medical imaging procedures. Indeed, the most common application of a radiation detector is digital imaging: examples of detectors are CCDs or CMOS pixel sensors normally found in digital cameras, which are detectors sensitive to the visible light. These detectors are considered as “pixellated”: they are made up of multiple of small elements (pixels), each one acquiring data independently. The resulting image is a data combination acquired by all pixels. The notion of pixel (short for “picture element”) has been introduced in image processing to describe the smallest discernible element in a given process or devices. A pixel detector is therefore a device able to detect an image and the size of the

pixel corresponds to the granularity of the image. Nowadays, everyday life is surrounded by pixel detectors. Photo cameras, smartphones and X-ray films are just common examples and follow the same working principle: photons of different energies are integrated over each sensing element (pixel) during some exposure time and generate an intensity distribution which is the image [1]. In general, the image quality is determined by X-ray detector characteristics such as sensitivity, spatial resolution, and depth of field, as well as by the examination time, object contrast, and object intensity. In medical imaging the radiation intensity is always severely limited in the interest of a low radiation dose to the patient.

Sensor designed to detect different kinds of radiations are also used in other applications. One of the environment for which there is need of state-of-the-art detector system is High Energy Physics (HEP). HEP is the science that studies the nature of elementary particles that constitute the matter. Thus, detecting particles produced by collisions in accelerators makes it possible to study the basic constituents of matter. Multiple layers of pixellated detectors are used in modern HEP experiments to track and identify particles passing through them. For this application the pixel detectors are now widely used and they constitute a fundamental part of the HEP experiments operating at the most powerful particle accelerators in the world.

Another important application for novel detectors is also space science. In particular, pixel detectors are used for optical and X-ray astronomy and for planetary and solar science. Cameras or imaging devices are often mounted on satellites, both for space and Earth observation. An example in which a radiation sensor can be used in space is as a dosimetry device for astronauts, in order to measure their exposure to potentially harmful radiation [2]. Technology developed for space and HEP applications, especially for X-ray imaging, can be applied in other fields too. The main particular field of application is medical imaging, where pixel detectors are one of the fundamental components of systems for Computed Tomography, Positron Emission Tomography (PET) and other diagnostic techniques.

In general, early detectors used photographic plates to detect the tracks left by nuclear interactions. Moreover, the cloud chambers, used to discover subnuclear particles, needed photographic recording and a demanding measurement

of tracks from the photographs. Advances in microelectronics, particularly in integrated silicon technology over the last decades permitted significant progress in all field of engineering and science, specially for radiation detection. Moreover, advances in materials, particularly ultra-pure materials, and methods of fabrication have been critical to the creation of new and better detectors. The development of new ways of designing circuits ever smaller, with good resistance to damaging radiation favored several progresses in large-scale experiments.

## 1.2 Main challenges

One of the main requirement of a detector system is to being able to reliably work in the operational environment described above. For many applications (space, most of HEP experiments) it means that the electronics must be able to cope with a highly radioactive environment, since it can cause damage to the devices or sudden failures. Other challenges include meeting the requirement on the accuracy of the measurement. One of the most important parameter is the resolution, evaluated as spatial, energy and time resolution. In order to achieve a high spatial accuracy the detector must feature small pixels, so that the pixel matrix has a smaller pitch. The demand for smaller pixels requires the use of newer downscaled CMOS technologies. Other important characteristics for many applications are the speed of the front-end and the dynamic range of the detector. The first one represents the number of particles that can be detected in a unit of time, whereas the second one is the range of particle energy that can be correctly detected by the system. Improvements in the technology, together with smaller pixels, opened the possibility to develop "intelligent" system, able to implement advanced features. Some of the capabilities that can be included are calibration circuits, on-chip data processing or error correction algorithms. Implementation of such intelligent systems comes, of course, at the cost of additional complexity and power consumption. In many different applications a high power consumption has to be avoided, since heat dissipation can be problematic in some conditions. In space, for example, detectors may be used in an airless environment, which reduces the cooling possibilities. In HEP experiments a cooling system may interfere with the measurement being performed, due to a requirement on material budget. Novel techniques allowing

to reduce the power consumption are thus needed.

## 1.3 The operating principle

In order to design a radiation detector, different architectures can be used and are suitable to many applications. One of the main difference between semiconductor detectors is the way they measure the charge deposited by particles, by integrating it over time or by counting single events. In both systems charge is produced by the interaction of a particle with a material layer that can produce electron-hole pairs when exposed to radiation.

In integrating systems the charge is collected in an analog front-end and integrated over time. Currents generated by other sources (such as leakage currents) are also integrated, producing a noise signal. The amount of charge collected in a specific acquisition time is then stored, measured and read out. An event counting system, on the other hand, compares the collected charge with a threshold to detect single events. If the charge is above the preset threshold a counter is incremented, otherwise the signal is discarded. It also makes it possible to perform additional measurements such as acquisition of the arrival time. Moreover, multiple thresholds can be employed to discriminate particles which different deposited charge. This permits their identification. The main disadvantage of such systems compared to integrating devices is that the system must be ready to acquire a new particle after detecting one. This limits the number of particles that can be detected if they arrive at a high rate. Detection systems can also be divided in different categories according to the technology used for charge collection. As an example, the two main technologies for pixel detectors used for HEP applications are mentioned here, but there are many others used in other environments. One way of collecting charge is using the Monolithic Active Pixel Sensors (MAPS) approach. These devices incorporate in the same substrate a thin layer of sensitive material that generate electron-hole pairs interacting with incoming particles. Meanwhile they include the readout electronics, which can be built using standard CMOS technology.

The other main technology used for radiation detectors is the *hybrid pixel* detector architecture. In this kind of detector, the readout electronics is built separately from the sensitive material. The sensor is divided in pixels with

the same pitch as the readout chip and both are connected together. Since the two parts are produced separately, they can be optimized and designed independently from each other. Indeed, any standard CMOS technology can be used to design the readout electronics. The improvements in the lithographic process can be exploited to develop advanced systems, with smaller dimensions and more peculiar features. The main disadvantage of this architecture is the cost of the manufacture process, especially for pixel detectors with very small dimensions.

CHAPTER 2

# Portable Radon detection system

## 2.1 Introduction

The advent of silicon photomultipliers in radiation detection has enabled designing systems with characteristics not achievable with conventional photomultiplier tubes available in the past. Several agencies in the world have classified Radon as a human carcinogen and have demonstrated a correlation between environmental Radon concentration and lung cancer risk. Radon dosimetry supplies valuable information about radioactive health risks in indoor environments. The activity reported along with this chapter concerns the development of a compact system with compatible capabilities to the commercial Radon detectors state-of-art. The device is able to detect real-time indoor Radon concentration and to monitor environmental data, providing a reliable value of Radon concentration within few hours. Such detector could have multiple uses in research and industrial applications. The developed system, with embedded processing and wireless communication capabilities, is based on a scintillator coupled to a Silicon Photomultiplier, low cost read-out electronics and system ventilation.

## 2.2 Motivation and Outlines

Several agencies in the world, including the World Health Organization (WHO) and the International Agency for Research on Cancer (IARC), have already classified Radon as human carcinogen and have demonstrated a correlation between environmental Radon concentration and lung cancer risk.

Radon ($^{222}$Rn) is a colourless, odourless, tasteless radioactive gas that comes from granitic or shale related areas in the ground. It can often be sourced by granite floors materials or even from construction materials, thus polluting indoor air [3]. Radon was identified as a human lung carcinogen in 1986 by the WHO [4]. According to this organization, Radon gas is by far the most important source of ionizing radiation among those that are of natural origin. The carcinogenetic nature of such a gas is due to the fact that the element is an alpha source. The alpha particles readily stop (i.e. deposit all of their energy) in human tissue. Most of the inhaled Radon gas is immediately exhaled, however, if decay occurs in the lungs, the resulting solid radioactive particles can settle onto bronchial epithelial cells causing DNA damage. This gas constitutes the first cause of lung cancer deaths among non-smokers in the United States, and the second for smokers. Each year in the US there are an estimated 20000 deaths from lung cancer. In particular, recent epidemiological studies of the International Commission on Radiological Protection (ICRP), report an increased risk of lung cancer onset of at least 8% for a concentration equal to 100 Bq/m$^3$, considering an exposure period that can vary between 5 and 30-35 years, before the disease diagnosis [5]. It is a significant source of radiation exposure to the population and, in some situations, it may be the main source in the working environment. The exposure levels, however, greatly vary depending on the territorial geology, the type of buildings, their ventilation and their behavior occupants. Just to show some numbers concerning the situation in Italy, Lombardy region has a higher concentration of indoor Radon (116 Bq/m$^3$) than the national average (70 Bq/m$^3$). In particular, the Province of Bergamo, along with that of Sondrio, has the highest concentration. The problem is a deep concern for Regional and State Institutions. In fact, at the end of 2011, Lombardy Region has issued the Decree number 12678 containing the subject: "Guidelines to prevent Radon exposure within indoor environments" [6]. It is now an established fact

that high Radon concentration in the buildings may pose a significant risk of lung cancer to the people living there [7]. For this reason, indoor Radon detection can be used to assess the radioactive health risk in a given place [8]. Furthermore, outdoor detection can be useful in mining to detect concentrations of Uranium as well as for earthquakes prediction studies [9, 10]. In all these applications, portability is a key feature for the detector. A more detailed overview on commercial Radon detectors will follow in the next paragraphs.

## 2.3 Origins of Radon

Radon is generated in the decay chain of $^{238}$U, the most common Uranium isotope at 99.284% abundance in uranium ore. The isotope has a very long half-life, about 4.5 billion years. It decays to the stable element $^{206}$Pb through a long decay chain depicted in Figure 2.1.

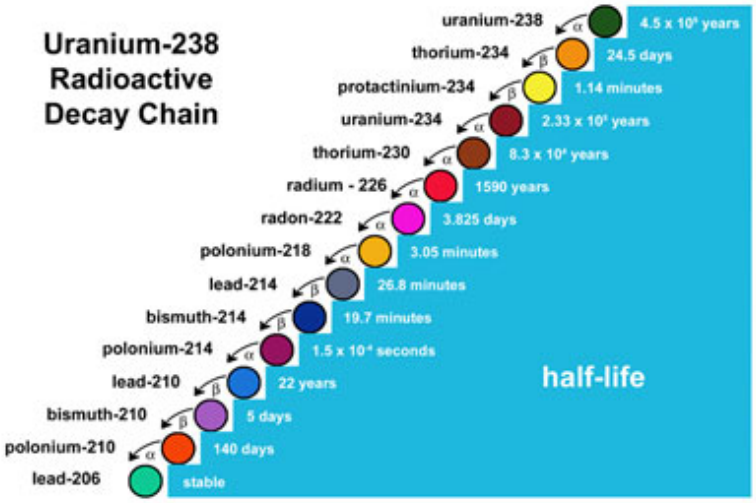



Figure 2.1: Uranium decay chain

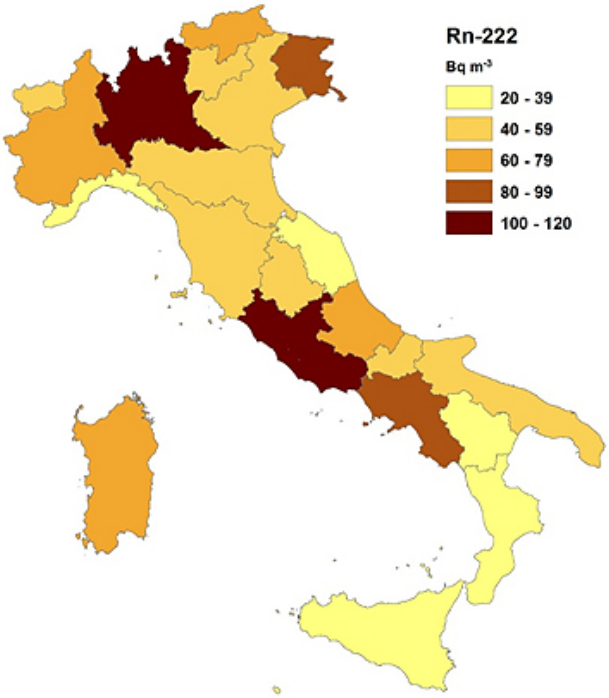
Many branches in the chain decay via alpha or beta emissions, but $^{222}$Rn is the first gaseous element with a short 3.8 days half-life, decaying via 5.6 MeV alpha emissions. These characteristics make Radon a health concern: it can propagate, accumulate areas with little ventilation and, finally, can be breathed into the lungs. Clearly, the abundance of Radon is strongly dependent on the geology. In fact, its concentration shows strong geographical variations: generally a strong presence is found in granitic or shale formations, while lower

concentrations are found in water and sandy soil. Figure 2.2 shows the Radon geology in Italy and in the United States. Typical Radon concentrations are in the 1 pCi/l (or 0.037 Bq/l). From health physics studies, the threshold of concern for Radon concentrations has been set by the Environmental Protection Agency (EPA) to 4 pCi/l (or 0.148 Bq/l).

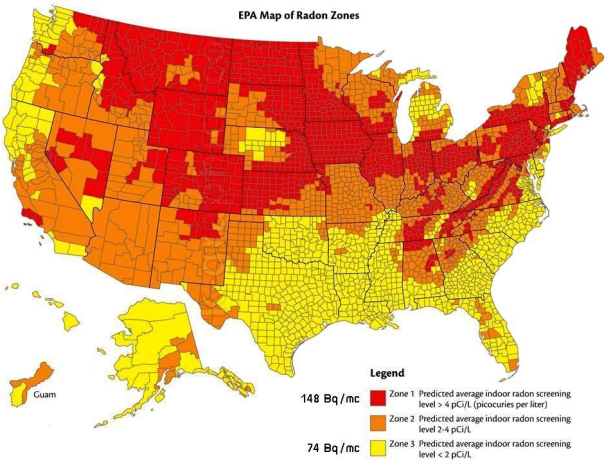
Fortunately, Radon mitigation for the home is rather simple and inexpensive. If a high Radon concentration is found in a house, simple improvements in ventilation will quickly fix the problem. For this reason, agencies recommend that all dwellings be periodically tested for Radon, and if high levels are found, to provide mitigation. Hence, Radon testing is very important. There are several ways homes can be tested for Radon. Testing methods vary from using activated charcoal sponges that trap Radon atoms, to optical detection of alpha tracks in plastic films. In these cases, a specimen is sent to a laboratory for analysis. There are even monitoring methods based on alpha particle spectroscopy and counting. These processes allow for real time measurements of concentrations directly in-situ. A comprehensive description of the techniques and methods is given in the following paragraph.

## 2.4 Measurement techniques for Radon detection

Nowadays many different techniques are available for such a type of application. The main difference is found in the nature of the measurement. A first family of measurements requires some form of sampling into a removable material and a successive laboratory analysis. The classical method consists in a so-called "grab sampling". This technique exploits capturing different samples obtained by filtering air at a test site through a charcoal filter at various time slots. The samples are then analyzed in a laboratory by a gamma spectrometer. It is a typical testing procedure: it represents what happened cumulatively in a certain time frame, and it gives no indication if the concentration values were seen as constant during a certain period or if they were due to a spike during the collection time. For these techniques the typical collection times can be as high as several months. In other words, this type of measurement gives a worst-case scenario, and identifies the total Radon dose a person would have received if he/she stayed in the environment for the whole duration of the collection campaign. Often it is more indicative to have a measurement of how




(a)




(b)

Figure 2.2: Radon geology in Italy (a) and in the USA (b)

a concentration changes as a function of time, as it represents a real scenario. For these purposes, the second family of measurements allows continuous monitoring of the concentrations, so it is possible to establish patterns and relations between concentrations and other factors. Devices belonging to this second family are also known as continuous area monitors (CAM). The principle behind CAM devices is rather simple, as they are mostly based on alpha counting. Alpha particles are a very detectable form of radiation, and the detection can be performed via gaseous, liquid or solid state detectors (both semiconductor or scintillation-based). In fact, there is a great variety of CAM detectors [11]. Nowadays the detection is performed by in-field alpha spectroscopy or passive closed-end cup devices based on polycarbonate detector material, such as PADC or CR-39 [12]. Sensing elements are sealed ionization chambers or surface barrier semiconductor diodes with a sufficiently thin active surface. The alpha particles impinging on the surface will pass the barrier and deposit their energy in the depletion region of the diode. Carefully manufactured diffusion junction diodes have also been proposed [10]. Other devices exploit internal signal amplification based on the bipolar transistor (BJT) effect that can be efficiently used for alpha-ray detection [13]. The main disadvantage is that reliable Radon concentration values are given after days or weeks. It is now an established fact that high Radon concentration in the houses may pose a significant risk of lung cancer to the people living there. Studies from all over the world show that a well-planned and systematic measurement of indoor Radon concentration is necessary to calculate the actual dose received upon indoor Radon concentration exposure. Depending on how air enters the measurement volume, some detectors may be faster than others. In any case, CAM detectors tend to be expensive (several hundreds to thousands of dollars), while the simpler accumulation-based detectors cost only a few tens of dollars (although the laboratory analysis may make up for the cost difference).

In adopting SiPMs and a scintillator as detector elements, it is possible to reduce system costs quite significantly: SiPMs are devices based on well-established silicon processes normally used for making integrated circuits. This is not true for devices such as silicon barrier diodes, as the purity levels required are not compatible with integrated circuit technologies. Further details on SiPMs structure will be presented later in the next paragraphs. In addition, in recent years several studies have been made in relation to the effect of

different parameters on the detected level of indoor Radon. In fact, the Radon concentration and its decay products in dwellings show large temporal and local fluctuations due to the temperature, pressure, humidity, building material, ventilation condition, wind speed, etc [14].

## 2.5 System requirements and goals

Some reasonable requirements for the proposed Radon detection system have been established and major constraints have been identified. These are reported in the following paragraph.
As previously stated, the EPA recommends that all dwellings be periodically tested for the presence of Radon. First of all, two main requirements can be established: the Radon detection system should be as portable and affordable as possible. Periodical testing means that the instrument may be utilized either as a continuous monitor or to make measurements only periodically. Therefore it is unthinkable to baseline an instrument that takes more than a few 100 $cm^3$ of space and requires constant maintenance (such as battery replacement or continuous calibrations). Thus, more requirements are identified: the device must be as maintenance free as possible, and even must be able to function for a long period of time without needing special attention. Currently, the standard Radon measurement requires the measuring device to be left unattended and undisturbed in an area for at least two days. This is due to the fact that in order to reach the statistical significance needed to complete a measurement, a certain number of events have to be collected. Given the activity related to typical Radon concentrations (pCi/l), this is accomplished in the time indicated above. If there were a way of increasing the number of events per unit time, there would be no other reasons why the measurement could not take less time. This is another important point: finding a technique that allows for quicker collection times. The practical impact on the system design is not only obvious time savings, but also less stringent requirements on how long the instrument must be able to operate on its own power source.
An initial set of specifications can be compiled. The application requirements and how they translate into system design considerations can be summarized with the following points:

- *Portability*: total size and weight constrained and low power;

- *Cost*: choice of inexpensive detector and electronics;

- *Ease of operations*: functions without operator intervention or maintenance;

- *Measurement duration*: shorter than two days for conventional applications;

In more details, portability means that the instrument cannot be heavy, its size must be contained and must possess its own internal power source. Commercial systems are available in several form factors, depending on the underlying principles and the performance level. The simplest traditional monitors are comparable to standard smoke detectors in size and weight; they offer limited performance (the reading levels become statistically significant after an average of 7 days) with a cost equal to about 150 Dollars. Professional systems are larger and heavier (4000 $cm^3$ and 1 kg) and cost in the order of 1000 Euros, but it offer the possibility of completing measurements within 48 hours. Recently, new Radon detector designs have hit the market. They are targeted to homeowner at costs of about 200 Euros. The weight is only 130 gr and can execute measurements at 2.7 pCi/l with a 20% precision in one week or 10% in a month. As an example, *RSens* (www.rsens.it) is an innovative Radon gas sensor battery-powered and easily programmable, with small size (16x16x11 cm) and 1.8 Kg of weight, that has achieved success during the last few years. It can carry out Radon measurements with 6% accuracy after 48 hours (with a concentration of 150 $Bq/m^3$). There is clearly room for a comparable-sized device capable of measuring similar concentrations in a few hours at comparable cost. Therefore it is possible to set a goal for a new design to be in the few hundreds $cm^3$, weight a few hundred grams and cost a few hundred of Euros.

Adopting a right technology is important in order to reach such goals. First of all, a simple scenario where air is introduced into a predetermined volume is examined. Such an assumption is without even considering which detector is going to be used. Furthermore, the other hypothesis done is that all of the decays within the volume can somehow be detected. The mitigation threshold is set at 4 pCi/l by EPA, and the unknown variable is the required time to detect 1/10th of such activity as a function of measurement volume. Since 0.4

pCi corresponds to 0.0148 Bq (or 0.0148 decays per second), table 2.1 indicates how many decays per second take place in a given volume.

| *Volume [liters]* | *Decays per second* |
|---|---|
| 0.1 | 0.00148 |
| 0.5 | 0.0074 |
| 1 | 0.0148 |
| 1.5 | 0.0222 |
| 2 | 0.0296 |
| 2.5 | 0.037 |
| 3 | 0.0444 |

Table 2.1: Number of decays per second in different volumes for a specific activity of 0.4 pCi/l.

If, as assumed above, all particles are detected, it is possible to count, for example, 3 events every 20 liters of air. On the other hand, the number of events detected as a function of time can be calculated (see table 2.2). This is done assuming that the entire volume of air every second can be recycled and keeping the activity constant.

| *Times [s]* | *Decays in 0.1 l/s* | *Decays in 1 l/s* | *Decays in 3 l/s* |
|---|---|---|---|
| 1 | 0.00148 | 0.0148 | 0.0444 |
| 2 | 0.00296 | 0.0296 | 0.0888 |
| 5 | 0.0074 | 0.074 | 0.222 |
| 10 | 0.0148 | 0.148 | 0.444 |
| 20 | 0.0296 | 0.296 | 0.888 |
| 50 | 0.0740 | 0.740 | 2.22 |
| 100 | 0.148 | 1.48 | 4.44 |
| 200 | 0.296 | 2.96 | 8.88 |
| 500 | 0.74 | 7.4 | 22.2 |
| 1000 | 1.48 | 14.8 | 44.4 |
| 2000 | 2.96 | 29.6 | 88.8 |
| 5000 | 7.4 | 74 | 222 |
| 10000 | 14.8 | 148 | 444 |

Table 2.2: Total events for a 0.4 pCi/l of volume exchange.

Since these are radioactive decays, they are subject to Poissonian statistics

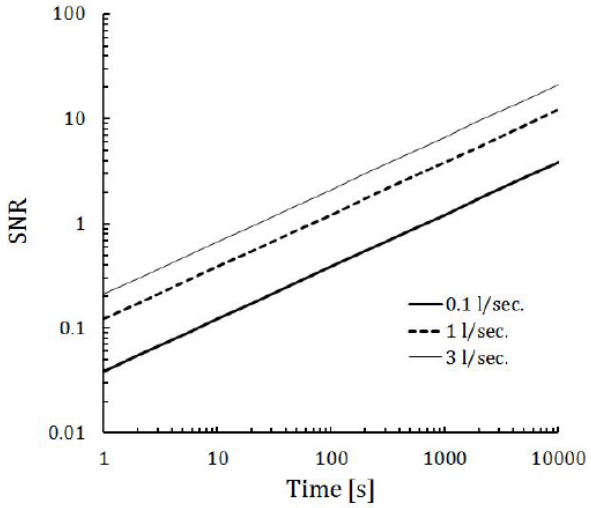



Figure 2.3: Signal-to-noise ratio for different flows at a 0.4 pCi/l activity

which determines that the total uncertainty on a number of events N is $N/\sqrt{N}$. Therefore, the plot shown in figure 2.3 represents a signal-to-noise ratio defined as the inverse of the uncertainty. From the plot it is visible after how long a unity SNR is reached, or how long an acquisition should last in order to achieve a certain SNR. For example, at 1 l/s an SNR of 10 (or a 10% variance) can be reached in less than 10000 seconds, corresponding to less than 3 hours. The important conclusion in this case is that there are no obvious physics reasons why a good detection would require more than few hours. This is, of course, a rough estimate: in a real system only a fraction of the decays is actually collected by a detector. By refining the estimate however, it is easy to determine the ultimate limits of such a technique.

## 2.6 Detector and Front-End design

The choice of the detector will determine what fraction of the total events is collected within the volume. In fact the detector establishes, along many other things, most geometrical constraints. In order to operate this choice correctly, it is useful to consider the main properties of alpha radiation. It is composed by helium nuclei (2 protons), therefore it is quite massive. It will tend to stop within short distances inside materials. Figure 2.4 shows a typical Bragg curve

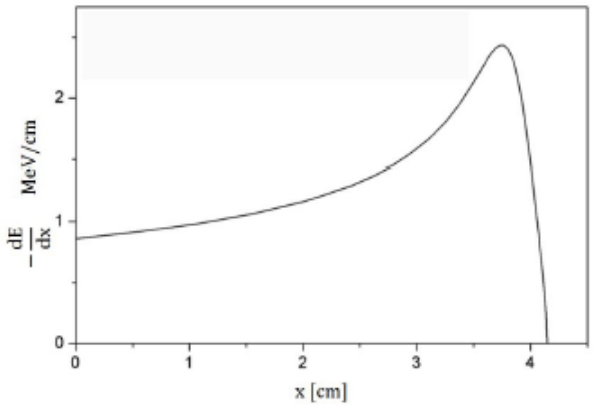



Figure 2.4: Typical Bragg curve for 5.49 MeV alpha particles in air.

for 5.49 MeV alpha particles in air. The peak, known as Bragg peak, is a pronounced peak on the Bragg curve which plots the energy loss of ionizing radiation during its travel through matter. It is dependent on the absorber and the particle characteristics. The most important observation about the Bragg peak is that at the peak there is the highest energy transfer between the particles and the absorber. The Bragg peak occurs at about 3.8 cm. This means that the measurement volume does not have to be too deep beyond 3-4 cm: anything beyond that will only contribute to losses of useful events.

Besides reasonable limits to the detector, size and type do not depend on physical limitation to the surface area of the detector, but on design constraints. Having established this, there is clearly no physical limitation to the surface area of the detector. These limitations are practicality in obtaining certain sizes, cost of the material and of related sensors (such as SiPMs if a scintillator is used). For cost reasons, for this prototype scintillators are used because they usually are inexpensive. Therefore, not to alter the measurements, the detector of choice has to be blind to other radiation (gamma, neutron). For similar reasons, it is good to limit the surface area to about 2.5 $cm^2$ in order to avoid costly choices and unnecessarily growing overall system size. A quick literature survey indicates that the ideal solution is one of the very first scintillators used in alpha spectroscopy (since the 1930s): zinc-sulfide silver activated. This material has practically no sensitivity to gamma rays or neutrons (unless activated with elements that have finite neutron cross-section). It is available as polycrystalline powder that, with the appropriate binders, can be painted

on a transparent backing (usually Mylar) with the thickness of choice. The interesting thing is that the detection efficiency for alpha particles (as measured by detected particles/incident particles) is nearly 100% for thicknesses between 10 $\mu$ m and 30 $\mu$m [15]. The only drawback for this material is the fact that it is not completely transparent due to its polycrystalline form, and its refraction index is high (2.4). In any case, given the alpha particle energy (5.6 MeV), the overall brightness of the events will be sufficient. ZnS(Ag) is readily available from scintillator manufacturers in sheets measuring 216 mm x 279 mm. Its trade name is EJ-440. The scintillator is deposited on a clear plastic sheet that serves as coupling mechanism to a PMT window or to a SiPM. The thickness of the deposited layer is chosen to optimize alpha particle detection (thus, as mentioned above, it is between 10 and 30 $\mu$m). The following table (2.3) supplies a list of the common constants for such a scintillator.

| ***Parameters*** | ***Values*** |
|---|---|
| Light Output (% of Anthracene) | 3 |
| Peak Emission Wavelength | 450 nm |
| Decay Time | 200 ns |
| Density | 3.25 mg/cm$^2$ |
| Polyester Film Thickness | 0.25 mm |
| Refraction Index | 2.4 |
| Cost | 1 \$/cm$^2$ |

Table 2.3: Main characteristics of the scintillator ZnS(Ag) on Mylar backing.

It is common referring to Anthracene to measure light output of certain scintillators. The light output for Anthracene is 17.400 photons/MeV. A complete datasheet is available from [16]. The low cost of this scintillator clearly does not drive the choice for its size. This will be determined by the cost of the light readout. The cost for cm$^2$ of PMTs and a SiPMs is quite comparable, with the outlook for SiPMs to become much cheaper in the near future. It is therefore worth to take advantage of the benefits offered by the latter. Before deeply going in the description of the detector model, a brief explanation of SiPMs working principles is given in the followings.

The radiation detection via scintillation light involves very low levels of light. Thus, the photosensor has to be either very efficient, or provide internal gain,

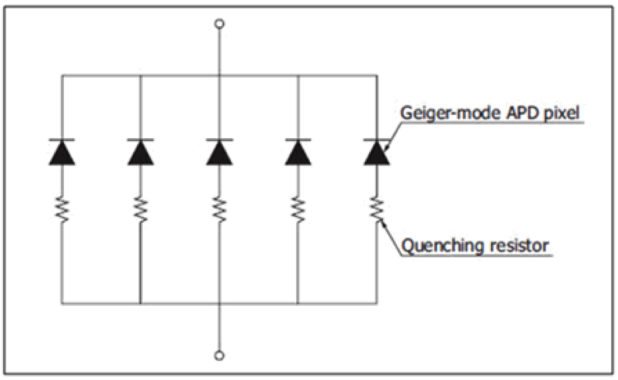



Figure 2.5: Simplified schema of a silicon photomultiplier.

so that the charge photogenerated is amplified to obtain high signal-to-noise ratio (SNR). Photodiodes (PDs) have high quantum efficiency but they have some shortcoming such as no- to modest gain, so that the instrumentation design is complex due to poor SNR. Photomultiplier tubes (PMTs) have very high gain, about $10^6$, but they are bulky, fragile and require high voltages in the order of kilovolts. In the late 90s a new device was envisioned that could offer the high gain of PMTs and some of the advantages of Silicon photodetectors. Such devices are known as Silicon photomultipliers (SiPMs in short). These devices are based on small (about 10 $\mu$m-sized) elementary cells that respond to a single light photon through an avalanche effect in a very similar way to Geiger-Muller counters. If several such elementary cells are constructed on a larger area, they are able to detect the energy deposited in the scintillator in a proportional way. Each cell is pratically a photodiode and a quench resistor in series to limit the discharge current. The photodiode operates a few volts above its breakdown voltage so that electrical breakdown occurs if a photoelectron is generated within the active volume. In order to be sensitive to successive photons every avalanche breakdown is interrupted by the built-in quench resistor. Relevant SiPM properties are low operating voltage (usually lower than 100 V), ruggedness, insensitivity to magnetic fields as well as compact dimensions [17]. Figure 2.5 shows a simplified structure of a silicon photomultiplier.

The market offers several SiPMs in the few $cm^2$. For the detector proposed

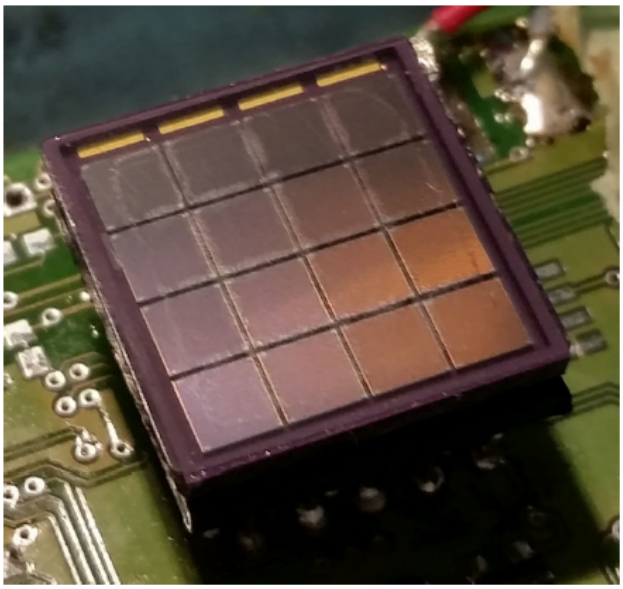


Figure 2.6: SensL Array SB-4, silicon photomultiplier.

a 4x4 array of 9 $mm^2$ cells has been chosen from SensL (model: Array SB-4). The cost is about 400 dollars in small quantities. The array, depicted in Figure 2.6, is conveniently mounted on a low-profile ceramic carrier with through-hole pins to enable easy design and installation on a PC board. Tables 2.4 and 2.5 show the pixel and whole array characteristics respectively. Data are taken from SensL Array datasheet [18].

The interesting parameters of the SiPM are the Photo Detection Efficiency (PDE) and the peak sensitivity wavelength of 420 nm. The SiPM PDE by definition represents how efficient the device ultimately is in detecting photons. Typical PDE values are about 25% (up to 35%) at 450 nm peak wavelength. The efficiency depends also on over-voltage. The two parameters perfectly match with the scintillator chosen for this application. The SiPM has been coupled to the scintillator sheet via optical grease.
The ZnS(Ag) scintillator has a refraction index of 2.4, and, as mentioned above, it is deposited on a plastic film (n=1.67). Since the SiPM light entry window is encapsulated in clear epoxy (n=1.54), most of the light losses will be concentrated in the ZnS(Ag)/Mylar interface, where the strongest mismatch exists. In fact, from the Fresnel equations for normal incidence, the reflected light at this interface is 18% of the incident light. The remaining optics is coupled with standard silicon-based optical grease such as the Saint-Gobain

| ***Parameters*** | ***Values*** | |
|---|---|---|
| | ***Array SB-4*** | ***SPM42H5-60P*** |
| Pixel area | 3.16 x 3.16 $mm^2$ | 3.96 x 4.44 $mm^2$ |
| Pixel thickness | 450 nm | |
| Pixel active area | 3x3 $mm^2$ | |
| Breakdown voltage (VBr) | 24.5 ± 0.5 V | 28 ± 1 V |
| Overvoltage range | 1 to 5 V | 1 to 5 V |
| Microcell recovery time | 130 ns | 78 ns |
| Peak sensitivity wavelength | 420 nm | 400 nm |
| Gain | $3x10^6$ | $6.94x10^6$ |
| Number of cells per pixel | 4774 | 4871 |
| PDE | 31 % | 37 % |
| Dark current | 2.8 $\mu$A | |
| Temperature dependence of VBr | < 20 mV/ C | |

Table 2.4: Pixel characteristics: comparison between the SensL Array SB-4 and STMicroelectronics SPM42H5-60P.

| ***Parameters*** | ***Values*** |
|---|---|
| Active area | 13.4x13.4 $mm^2$ |
| Pixel pitch | 3.36 mm |
| Package size | 15.81 x 15.31 $mm^2$ |
| Package height | 1.5 mm |
| Package type | Alumina $Al_2O_3$ |

Table 2.5: Full array characteristics for the SensL Array SB-4.

BC-630 [19] with a refraction index of 1.47. This is a standard material, widely used in the field. With these choices, the total amount of light transmitted through the interfaces is shown in Table 2.6. For every MeV of incident energy it has been assumed that 52200 photons are generated within the scintillator (see table 2.3) and 50% of them reach the scintillator exit window in the direction of the SiPM. Furthermore the scintillator is supposed to be transparent.

In reality some of the light in the opposite direction bounces back at the ZnS(Ag)/Air interface due to the strong refraction index mismatch for that interface (2.4/1). As can be seen from the table, about 75% (19740 over 26100 photons) of the amount of light in the direction of the SiPM reaches it (or

| *Interface* | *Amplitude reflection coefficient* | *Transmitted photons [photons/MeV]* |
|---|---|---|
| ZnS(Ag)/Mylar | 0.179 | 21.428 |
| Mylar/Bc-630 | 0.06 | 20.143 |
| BC-630/SiPM | 0..02 | 19.740 |

Table 2.6: Total amount of light transmitted through the interfaces.

38% of the total, that means: 19740 over 52200 photons). Since the SiPM has a QE of 30% at these wavelengths, about 6000 photoelectrons are generated for each MeV of energy deposited. Each alpha particle (5.6 MeV) will then produce in the worst scenario an average of 33.600 photoelectrons. So in this situation the signal abounds. However, the analysis holds under the assumption that the scintillator is completely transparent. ZnS(Ag) is basically a white polycrystalline powder or paint, therefore its opacity is non-negligible.

A simple experiment has been set up in order to estimate the total losses due to opacity, in particular to estimate the actual light output of the scintillator in response to the 5.6 MeV alpha events. For this purpose a conventional Hamamatsu photomultiplier tube (R11265U-100) was used, coupled with a ZnS(Ag) screen matching the PMT window size (23 mm x 23 mm). The advantages in using a PMT in this case were that the device was readily available and could be integrated immediately with the bench top instrumentation in the laboratory. Such an experiment has been performed by Lorenzo Fabris at Oak Ridge National Laboratory (Nashville, Tennessee). The arrangement is shown in Figure 2.7.

Initially, the PMT was calibrated by coupling it with a CsI(Tl) crystal. By exciting the crystal with a 662 keV $^{137}$Cs source, energy spectra as a function of bias voltage were recorded. By knowing the light output of the crystal and its coupling to the PMT, it was possible to estimate the number of photons that reach the PMT window. The experiment result confirmed that because of opacity, the actual photon yield is about 1000 photons for a 5.6 MeV signal (or about 180 photons for 1 MeV). The influence of opacity is clearly the dominant factor, and reduces brightness considerably. The comforting observation is that, for the energy of interest, the signal is still abundant and many photons can be detected.

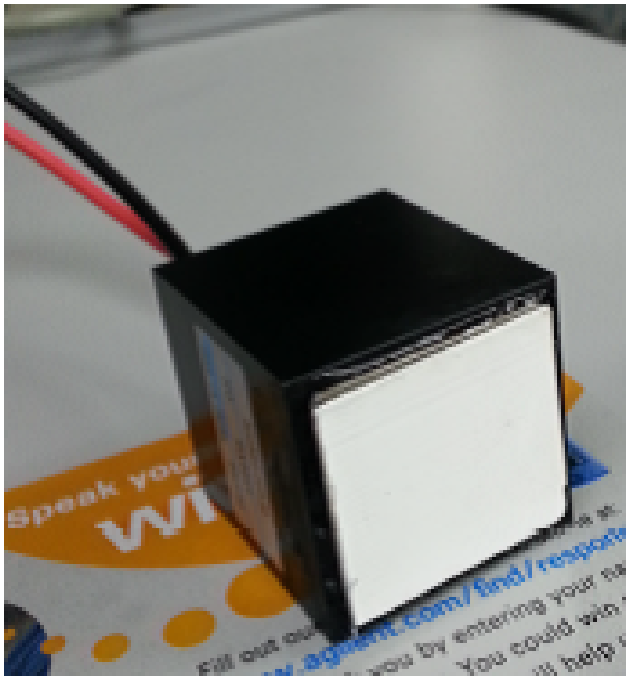
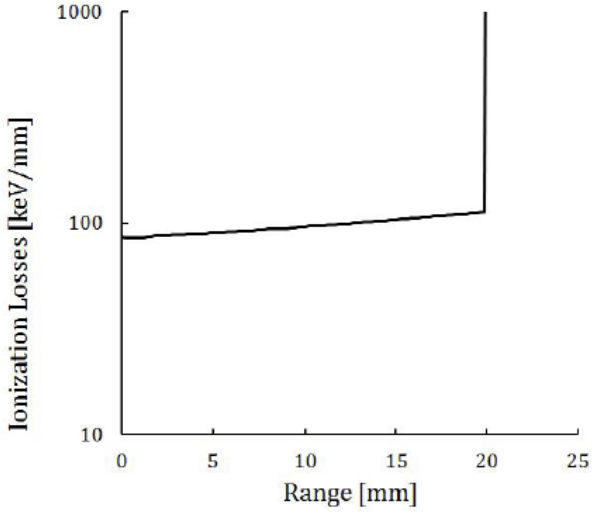


Figure 2.7: ZnS(Ag)/PhotoMultiplier setup to measure the actual light output of the scintillator (in photons/MeV).

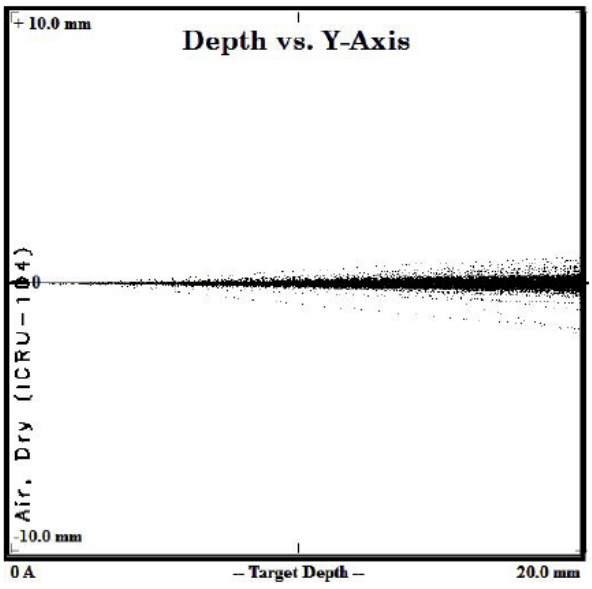
### 2.6.1 Detector model

As can be calculated from Figure 2.3, the detector will be enclosed in a measurement chamber in which the air flow is kept at the appropriate rate. Based on the fact that the mean free path of alpha particles in air is in the few cm range (anything beyond that will not contribute to the measurement), the idea is to concentrate the air within a volume that is 1-2 cm deep. In this case, all the alpha particles travel for a distance shorter than the mean free path. In this way, there is a higher chance for the particles to reach the detector. This has been confirmed with Monte Carlo simulation plotted in Figure 2.8.

During this simulation, a 5.6 MeV alpha beam crosses a 2 cm air volume with an absorber at the end. Figure 2.8(a) shows the ionization losses along the path to be about 100 keV/mm. Despite the sharp increase of ionization losses at the absorber, the behavior never incurs the Bragg losses shown in figure 2.4. This confirm that all of the alpha particles emitted within the volume will make it to the detector. A further confirmation of that is shown in Figure 2.8(b) where the direct Monte Carlo simulation output of the alpha tracks is




(a)



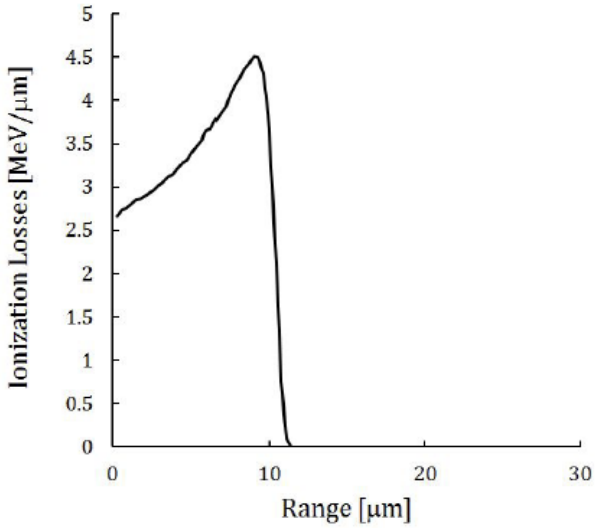

(b)

Figure 2.8: Ionization losses of 5.6 MeV alpha particles in air (a). An absorber is put at a 20 mm distance. Alpha tracks in the same volume of air (b).

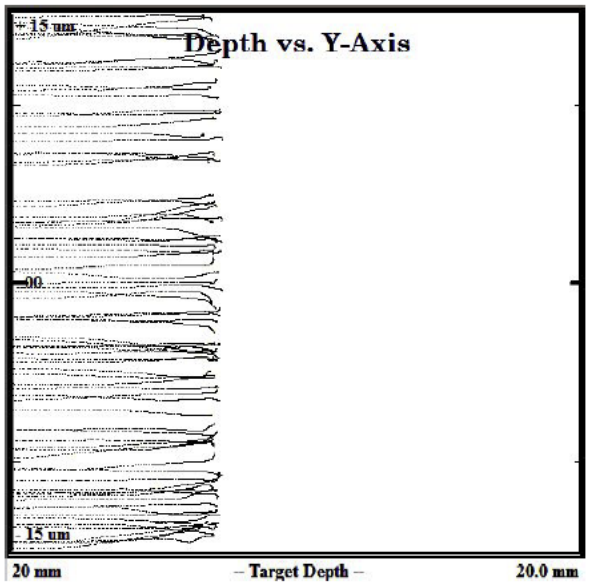
visible. A simple integration indicates that all of the alpha particles reach the absorber.

For what concerns the energy distribution within the detector, the particles of interest are mono-energetic at 5.6 MeV. Moreover, the particles reaching the detector will not all deposit the full alpha energy, but also a continuum of lower energies, since each particle loses about 100 keV each millimeter in air. This can be seen from figure 2.8. The resulting energy distribution in the detector will be the overlap of the distributions of alpha particles with a continuum of energy between 5.6 MeV down to 5.6 MeV less the highest possible energy loss in air. Figure 2.9 shows the ionization losses of the alpha particles entering the detector and a zoom into the particle tracks in a region located $\pm 15$ $\mu$m around the incident beam starting at the entrance window of the scintillator (30 $\mu$m thick). The initial conditions are given by the simulation results of Figure 2.8. From these results it stands out that the energy spectrum collected by the detector is mostly a continuum of energies, without any particular peak.

In order to measure the number of particles that have been detected, the simplest way is to count each event in the detector. This is done by simply counting anything above a predetermined threshold, without energy discrimination. Not requiring energy discrimination in the electronics is an advantageous simplification. The sizing of the chambers cross-section where the SiPM is intended to be placed, has to match the SiPM surface area at a minimum (13.4 x 13.4 $mm^2$). Furthermore it could be somewhat larger so that alpha particles from off-axis directions can contribute to the measurement as well, but not so large that the particles are never detected. The measurement volume chosen was thus set to be 26.7 x 26.7 $mm^2$ for the surface where the detector is mounted, times 17 mm depth. With these dimensions set, is it possible to finally determine how many decays reach the SiPM area. An upper bound can be determined by completely neglecting any alpha particle absorption in air, and observing that the radioactivity of the air within the measurement volume is homogeneous and constant with an activity $a$ (in Bq). The number of particles that hit the photodetector area is proportional to the ratio of the detector area to the total area. In other words, the number of particles hitting the SiPM, N (in particles per second) can be estimated with




(a)




(b)

Figure 2.9: Alpha particle ionization losses in the detector after transit in the air volume (a). Tracks within the detector (b).

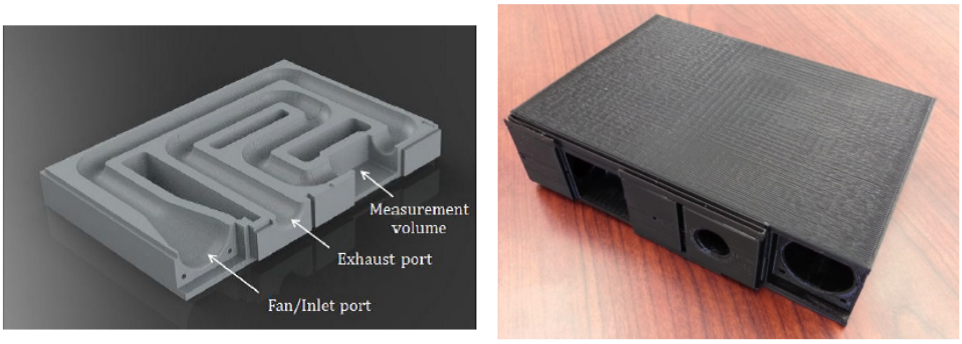
the following fraction:

$$N = a \times \frac{\{\text{SiPM area}\}}{\{\text{total area}\}} = \frac{179.56\ mm^2}{3251.6\ mm^2} = 0.055a \tag{2.1}$$

To confirm this, a Geant4 simulation has been run under the same assumptions, except for the fact that the influence of air on alpha particles was considered. A geometry representative of the measurement chamber was set up and filled it with 1 atm of air with uniform, isotropic emission of 5.6 MeV alphas. The total alpha particles in the chamber resulted to be $2\text{x}10^5$ and the alphas detected in an area equal to the SiPM were $1.3\text{x}10^4$. Therefore the calculated fraction of particles reaching the SiPM was 0.065, in good agreement with the geometrical calculations shown above. As already described with the plot of Figure 2.3, the minimum detectable activity is 0.4 pCi/l (one 10th the EPA threshold for remediation). This means 0.0148 Bq within the measurement volume. Considering the value calculated with the equation 2.1 (the least optimistic estimate), the number of decays that will reach the detector every second is $8.14\text{x}10^4$. In order to have a 10% precision, the SNR is equal to 10, thus, is necessary to count enough decays to ensure that $\text{N}/\sqrt{\text{N}} = 10$. This means 100 counts, which is easily done in 122.850 s, or 34 hours on average. The result obtained compares very favorably to commercial devices that are currently achieving the same level of precision in one month of continuous measurement. The underlying result is also that a level comparable to the EPA threshold can be detected in just a little longer than 3 hours. It is worth pointing out that, as originally stated, the half-life of radon decays is only 3.8 days, so it is not advisable to simply compress 1 liter of air into the measurement chamber and wait for the evaluation to complete. Designing a simple ventilation system around the measurement volume permits to bypass this potential issue, that allows for a constant air exchange equal to 1 liter per second.

### 2.6.2 Ventilation system design

There are several small (2.5 cm or so) DC fans capable of low power (less than 1 W) and low rates in the liter per second. Such a fan, coupled with proper air transport, can be used to ensure the desired flow rates within the measurement volume. The SiPMs are light sensitive, therefore precautions must be taken to prevent light from propagating into the measurement chamber. The simple proposed geometry in the model cutout of Figure 2.10(a) could work, provided




(a) (b)

Figure 2.10: 3D model section of the tubing system (a). Tubing system developed by 3D printer (b).

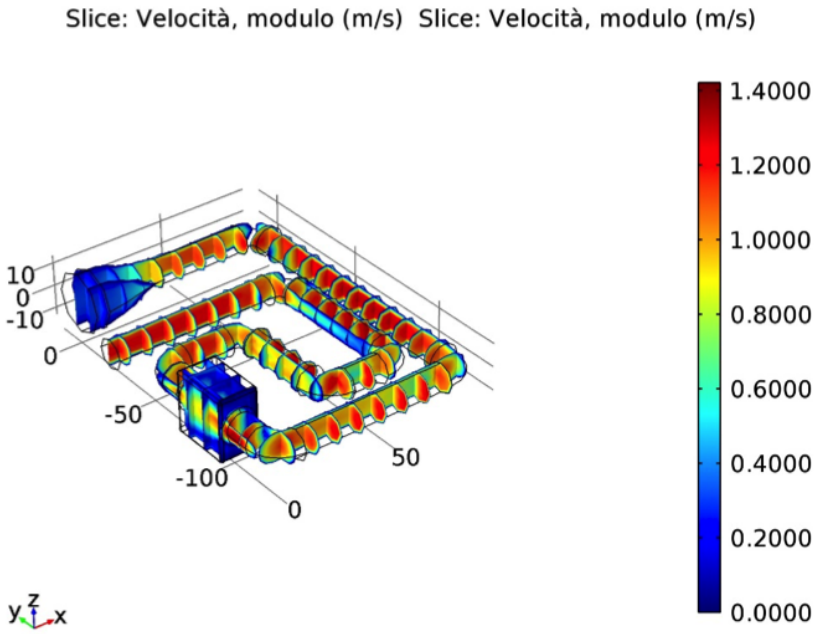
the transport losses are kept to a minimum. A fan is connected to the converging duct at the inlet side. The first section of the tube runs into the measurement volume after three right-bends. In this way, any light coming from the outside should be removed completely. The exhaust tube, after the measurement chamber, folds five times before reaching the exit port. The diameter of the tubes is 12.7 mm. It is easy for such a system to estimate the pressure drop along the pipes by using standard calculators (www.pipeflowcalculations.com).

For these simple calculations, losses in elbows can be expressed as equivalent-lengths of pipe from empirical tables or calculators. In this case, the eight elbows and the two sudden enlargements (the measuring volume), are equivalent losses introduced by 370 mm of extra pipe. The overall length of straight pipe is 408 mm as measured on the model. Thus, the pressure losses from inlet to outlet for the whole system are equivalent to those of a 0.5 inch diameter pipe that is 778 mm in length. From the calculation indicated above, the total expected pressure drop for this piping system is about 0.086 mbar. We can safely assume that the overall air flow will be preserved within such system. This calculation has been also verified directly on the model by Computational Fluid Dynamics (CFD) analysis, using Comsol software (www.comsol.com). The total drop pressure calculated as the difference between the pressure value at the ventilation inlet and the outlet is equal to 0.14 mbar. Figures 2.11 (a) and (b) respectively show the outline of the velocity and pressure inside the tube ventilation, in normal condition. The simulations confirm that with such

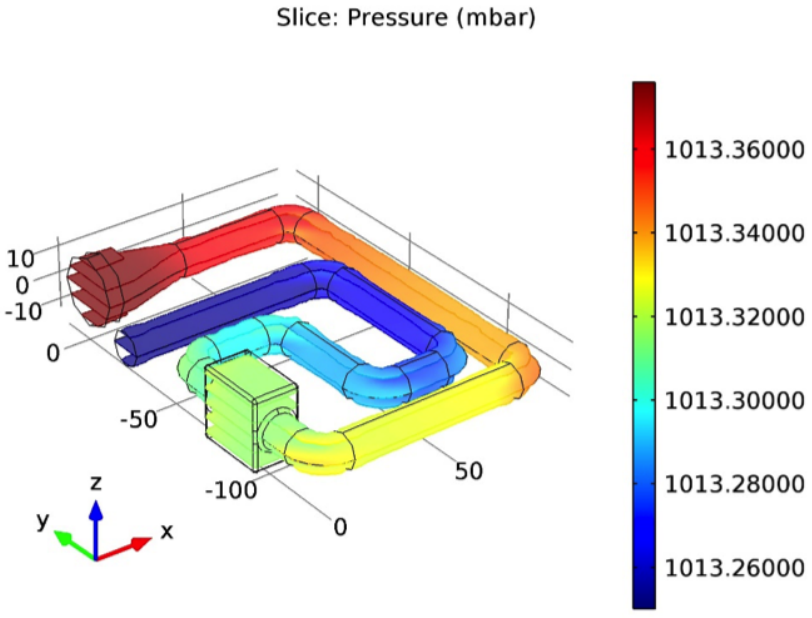
a pipe system design the flow imposed at the inlet is conserved without major losses. Therefore this confirm to have a simple way of maintaining a constant air flow within the measurement volume.

### 2.6.3 Electronics readout design

According to the estimation made in the paragraph 2.5, each alpha particle generates about 1000 photoelectrons with a high SNR. The conventional technique for detecting particles is based on the simplest circuit with 50 Ω resistor to ground. This would match cable impedances and allow for easy handling of the information. However, the resistor will be directly in parallel with the whole 13.6 nF sensor capacitance, introducing a time constant of 50 Ω x 13.6 nF = 680 ns. Moreover, a fairly long exponential current waveform with an area equal to the total charge produced is expected. The total amount of charge generated by an alpha particle and amplified by the SiPM (assuming a gain of $10^6$), would be 0.16 nC. This mean the voltage drop on the 50 Ω resistor would have peak amplitude of 11.8 mV. While this may be an acceptable solution in some case, it falls short of two characteristics in this application. First, it is a full-bandwidth signal, so the noise content is expected to be relatively high: it is always good practice to limit the bandwidth to what is really needed. Second, the waveform is highly asymmetrical. This has implications when attempting to identify the presence of an event via counting pulses at a comparator output: the fast edge requires fast triggering circuits. These circuits will respond equally fast to the slow edge, creating possible oscillatory conditions due to the noise present on the tail. A more elegant solution would allow for only as much bandwidth as is needed, a more symmetric waveform, and lower noise. A charge amplifier and a properly designed filter would accomplish these tasks quite nicely, but there would be some complexity due to the high SiPM capacitance. The effect of such a high capacitance on the charge amplifier would be to introduce an undesired bandwidth limitation in a similar way to having the 50 Ω resistor. The situation could be improved by having more current in the amplifier, but this would mean an increased power demand on the system. Overall, this solution will likely require the use of many components. On the other hand, a current amplifier would offer lower input impedance for a relatively low standing current, making the current waveform more symmetric. In fact, the input impedance of a bipolar transistor in a common base configuration is, to first approximation,




(a)




(b)

Figure 2.11: CFD analysis for piping ventilation system related to velocity (a) and drop pressure outline (b).

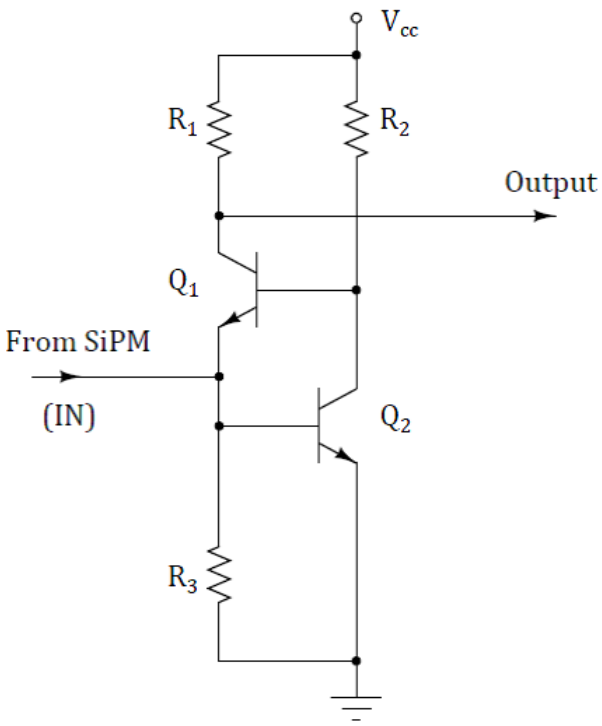



Figure 2.12: First stage of the SiPM readout channel.

the inverse of its gm, with transconductance gm = 40 mS for each mA of collector current. This, in practice, means 25 Ω per mA. With additional feedback, the input impedance can be made even lower. This means that the SiPM's original signal can be preserved without influence from the preamplifier, and the same amount of charge would be available in a shorter waveform.

The first stage of the circuit designed for this application is inspired by the circuits proposed in [20] and it implements a feedback common base architecture. Shown in Figure 2.12, the circuit accomplishes a very low input impedance, good bandwidth and low noise. Furthermore it easily allows implementing any amplification and signal conditioning in later stages. The transistor Q1 would normally be a common base configuration, but in this case, the transistor Q2 implements a feedback loop around Q1 that has the effect of lowering its input impedance. The current output is then taken on the collector of Q1. The output impedance of the circuit is R1 in parallel with the impedance seen at the collector of Q1, which is much higher of R1. In order to design a portable

application, the component parameters have been selected to guarantee low power levels and good performance at the same time.

By indicating with $I_1$ and $I_2$ the bias currents in Q1 and Q2 respectively, by neglecting the base currents, the assumption done is that the base-to-emitter voltages is equal to $V_{BE}$ for both transistors. Moreover, $I_1$ and $I_2$ are calculated with equations 2.2 and 2.3.

$$I_1 = \frac{V_{BE}}{R_3} \tag{2.2}$$

$$I_2 = \frac{V_{CC} - 2V_{BE}}{R_2} \tag{2.3}$$

If $V_{CC} > 2V_{BE}$, the current $I_2$ can flow in the desired direction. Arbitrarily considering $V_{CC} = 2.8$ V, is it possible to set the currents, as $I_1 = 0.35$ mA and $I_2 = 0.81$ mA. The values for these currents set the bipolar transistors transconductance. The choice made for the currents optimizes power consumption. The current values imply a power consumption of 3.3 mW total. Consequently, the resistor values are R3 = 2.05 kΩ, R2 = 1.65 kΩ. As for R1, its value sets the voltage on the collector of Q1. The bipolar transistors selected for this circuit design are standard BFR92A, available in surface mount package. These transistors are the preferred choice for many applications due to their versatile characteristics and very low cost [21]. The stages that follow the preamplifier are chosen to ensure that the signal has a shape that can be easily handled for the purpose of identifying events in the detector, and to make sure the available dynamic range is fully exploited. As mentioned previously, the detector signal has a fast initial rise and a slower exponential decay. For the choices made, the fast rise will be limited by the bandwidth of the preamplifier, while the exponential decay will be identical to the scintillator relaxation time. In this case, that time is slower than the cell recovery time constant of the SiPM. Such a low symmetry in the signal imposes somewhat stringent requirements on the pulse detection circuits. Without much impact on power consumption, it is possible to introduce stages that properly shape the signal into something more manageable. Typically, these are active filters, so they accomplish amplification as well.

In order to evaluate the functionality of the circuit, some Spice simulations have been done with the components values set previously. The analysis and simulation circuit are reported below. The software used for such simulation is LTSpice (www.linear.com/designtools/software). The initial bias point simula-

tions simply confirm the values calculated and the power consumption that was anticipated during the design step. The parameters of interest are the input impedance and the dynamic response of the circuit. Thanks to the feedback provided by Q2, the impedance is more than an order of magnitude lower than what could be obtained from a single common-base transistor operated at the same total current (in that case, the impedance would be 21 Ω).

The intrinsic signal from the SiPM sensor, as already observed before, have a fast edge followed by a slower, 130 ns trailing edge (see Table 2.4). The light signal, on the other hand, will be similar, except for the fact that the trailing edge will be set by the relaxation time of the scintillator, 200 ns. The total charge delivered for a 5.6 MeV signal is 0.16 nC; this is also the area of the current signal coming from the sensor. It is easy to simulate such signal in a first order approximation. Such an approximation is done by using a triangular waveform with a fast (a few ns) leading edge and a 200 ns trailing edge. The peak value of this signal is such that the area over the time axis is equal to 0.16 nC. Thus, the current peak is 1.6 mA. As for the output signal, if we were to read the voltage signal developed on R1, we would have a peak of 1.6 V. Given the biasing point conditions, this amplitude swing may bring some transistors outside of their linear regions. In order to avoid that, the preamplifier has been used as current buffer instead of voltage amplifier, by reading out the signal current in the collector of Q1 directly as the output variable. For this design the simplest solution has been adopted; such a solution is using an operational amplifiers inverting input. This particular choice allows also to build some filtering into the operational amplifier design itself, thereby saving in power and overall component count. The benefits of introducing filtering (or shaping) on a signal are discussed in depth in [22] [23] [24]. As normally the process of shaping reduces the overall bandwidth to what is necessary to correctly process the information of interest and nothing more. This way, the total output r.m.s. noise (equal to the integral of the noise spectral density over the bandwidth) is reduced compared to having a wideband output. This leads to better signal-to-noise ratio, improving the identification of signal pulses. Normally, the filtering is implemented through the use of standard active filtering blocks. The characteristics of the pulse vary with the number of poles used to implement the filter. The simplest filters have two coincident poles and one zero (second order filters). As already explained, in this design the

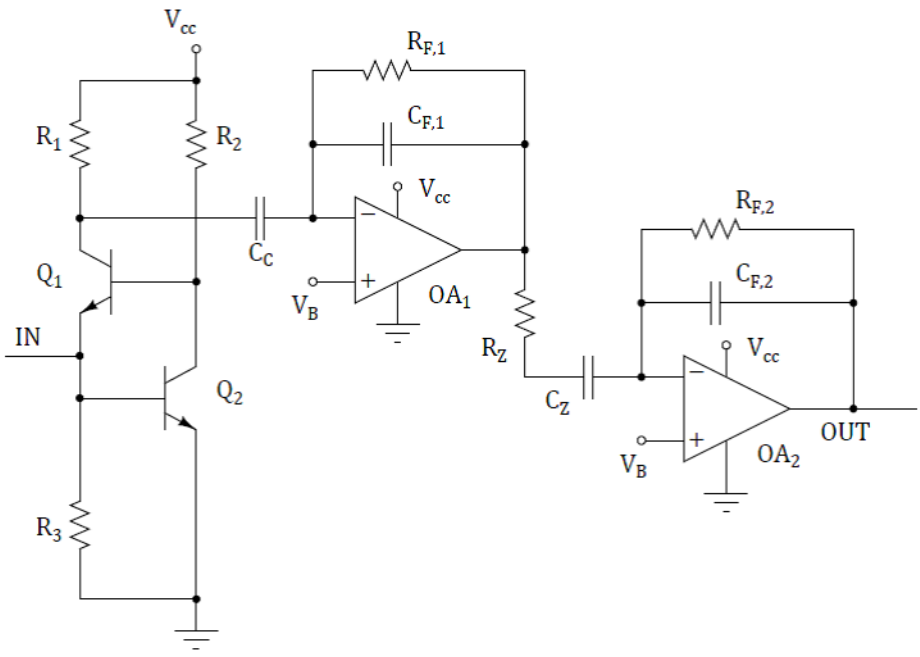



Figure 2.13: Preamplifier, first stage and second stage of readout.

chief requirements are low power and simplicity. Therefore, the obvious choice is the simplest filter designed with the fewest possible components. For this reason a simple exponential second order filter has been selected. The resulting preliminary circuit is shown in Figure 2.13.

The first operational amplifier, $OA_1$, transforms the current pulse (a delta) into the step function required for the filter to present the desired exponential response, via integration on the feedback capacitor $C_{F,1}$ chosen to be 250 pF. This introduces a transimpedance gain equal to $1/C_{F,1}$, or $10^9$ times the amount of charge generated by the SiPM (thus the voltage step is expected to be in the mV range). The resistor $R_{F,1}$ simply restores the output voltage of $OA_1$ to the baseline value and does not affect the subsequent shaping process, so long as the time constant $R_{F,1}$ x $C_{F,1}$ is $\gg \tau_p$. The second stage has been AC-coupled to the input amplifier via the capacitor $C_C$. For this stage the following parameters have been selected: $C_C = 10$ $\mu$F and $R_{F,1} = 1\text{M}\Omega$. The second stage is the actual filter. The transfer function is calculated in terms of Laplace formalism. In particular, for an operational amplifier with negative feedback the gain equals the ratio between the impedance located from the output to the virtual ground, and the impedance from virtual ground to the

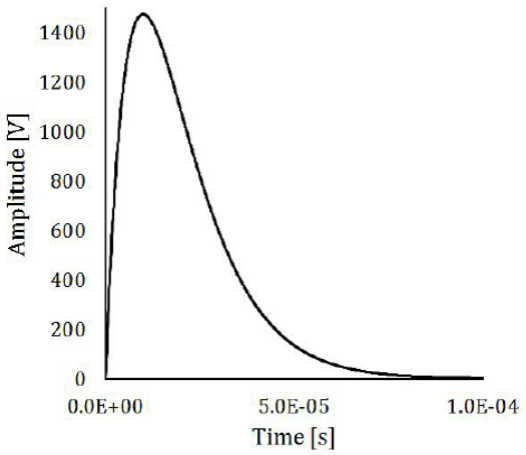



Figure 2.14: Calculated filter time response to a unity voltage step for a peaking time of 10 $\mu$s.

input. Thus, the transfer function for $OA_2$ is expressed with equation 2.4.

$$T(s) = \frac{sC_z R_{F,2}}{(1 + sC_z R_z)(1 + sC_{F,2} R_{F,2)}} \tag{2.4}$$

In this equation, s is the Laplace complex variable. Such a transfer function is based on one zero at the numerator and two poles at the denominator.

TSV732, made by ST-Microelectronics, is the high accuracy, micropower CMOS dual operational amplifier that has been chosen for the second stage. The detailed description is given in [25]. Important parameters to highlight for this purposes are the bandwidth (900 kHz), the power consumption (60 $\mu$A at 5 V supply) and the fact that the device is able to swing rail-to-rail input and output. This is important as one of the prototype requirements is low power, where the supply voltage is only 2.8 V. The voltage $V_B$ in Figure 2.13 is simply a DC baseline shift to account for the fact that the nominal baseline zero is not an actual ground in our single-supply design. The value for $V_B$ was chosen to be 1.4 V, the midpoint of the DC bias, but could be optimized later on to a different value to improve the use of the operational amplifier's dynamic range. The plot in Figure 2.14, shows the calculated response of the filter stage only to an ideal unity step at the input, with a 10 $\mu$s peaking time. Further details on simulations and readout design are provided here [26].

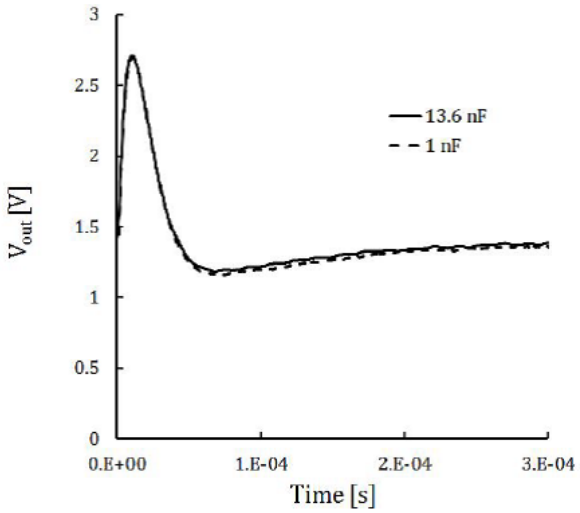



Figure 2.15: Comparison between the measured response with a 1 nF and 13.6 nF detector capacitance.

After Spice simulations, several different tests have been conducted on the circuit. The aim was to verify the functionality in response to ideal electrical pulses and compare the results to simulations. In order to do so, a charge pulse was injected into the circuit without the SiPM sensor to simulate a charge event. The easiest way of doing this was to apply a voltage step to a capacitor connected in series with the circuit input. The amount of charge to be delivered is arbitrary, but should be representative of a real event and within the limits of the circuit dynamic range. For sake of testing, 3.4 MeV-equivalent has been chosen. With a 1 nF injection capacitor, the step needs to be 96 mV in amplitude. This is the most basic test to verify circuit functionality, but it is also a simple way of finding the correlation between simulations and actual response.

Another important measurement to perform, before moving to the test with the sensor coupled to the circuit was the simulation with a larger capacitance, in order to simulate the sensor presence. Figure 2.15 shows the comparison between the peak output of the measured signal under the two different load conditions (1 nF and 13.6 nF). No significant differences are visible between the two peaks under the two load conditions. Finally, the electronics noise of

the circuit for a 13.6 nF capacitive load was measured with an r.m.s. meter and found to be about 1.6 mV r.m.s. over the circuit bandwidth. The tests just described has been performed using the PCB presented later.

### 2.6.4 Noise analysis

In order to properly design the electronics readout described above, some considerations on noise analysis are reported in this paragraph. Beyond the white noise, other noise sources can be taken into account for such analysis. As an example, the sensor may have shot noise related to leakage current. The way the sensor noise is processed depends also on the specific filter adopted. The equivalent circuit in Figure 2.16 highlights the main noise sources of the preamplifier. CD models the detector capacitance. The current source

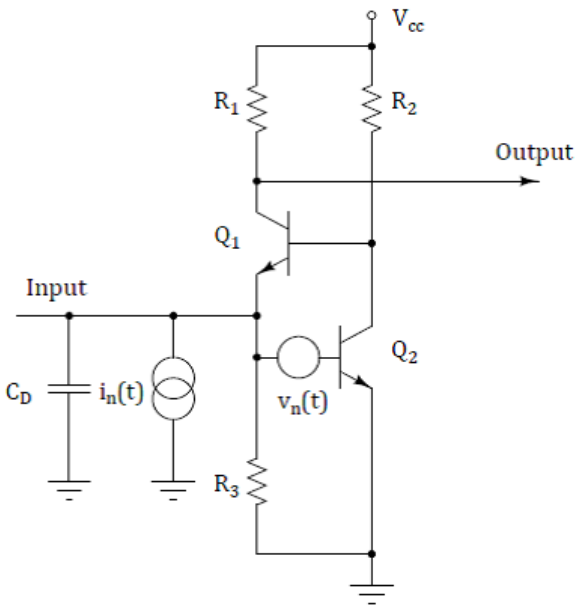



Figure 2.16: Equivalent noise circuit for the preamplifier in Figure 2.12.

$i_n(t)$ accounts for the noise associated with the circuit's input current and the detector leakage current. The power spectral density is:

$$\overline{i_n^2} = 2qI \tag{2.5}$$

The voltage source $v_n(t)$ with power spectral density is equal to:

$$\overline{v_n^2} = \frac{4KT}{g_{m,2}} \tag{2.6}$$

It accounts for the input noise of the transistor Q2, the dominant noise contribution within the preamplifier. Thus, considering the schematic in Figure 2.16, the general expression for the output noise, with series, 1/f and parallel noise contributions, is as follows:

$$\overline{v_n^2} = a \int_0^\infty |A(f)|^2 df + \int_0^\infty \frac{|A(f)|^2}{f} df + \int_0^\infty \frac{2qI}{(2\pi f C_D)^2} |A(f)|^2 df \qquad (2.7)$$

where A(f) is the filter's transfer function in the Laplace domain. Assuming a simple two-pole filter, the resolution can be expressed by:

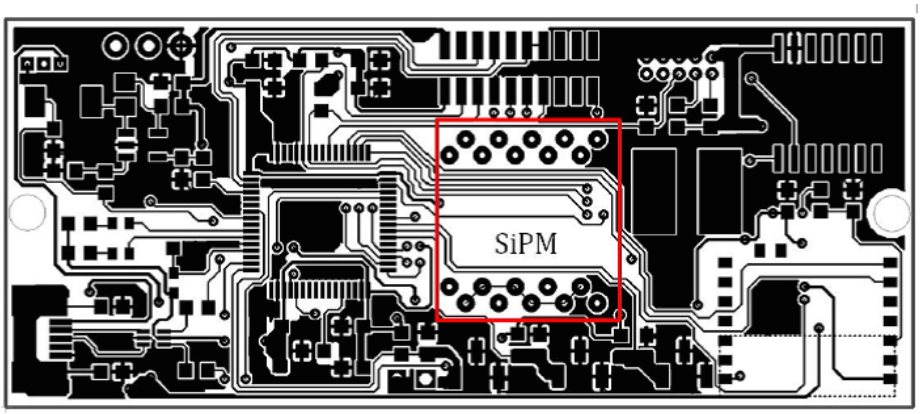
$$\overline{\sigma_n^2} = \frac{\epsilon^2 C_D^2}{q^2} \cdot \frac{4kT}{g_{m,2}} \cdot \frac{1}{\tau_0} \cdot r_D + \frac{\epsilon^2}{q^2} \cdot \frac{qI\tau_0}{2\pi^2} \cdot r_S \qquad (2.8)$$

In this expression, $g_{m,2}$ is the transconductance of $Q_2$, $I$ is the input current and is mostly identifiable with the sensor's leakage. In this design the 1/f term is negligible. The equation highlights the dependence of the noise on capacitance and peaking time. The integral of the transfer function *A(f)* produce terms dependent on a time constant $\tau$, characteristic of the filter. During the design phase these aspects have been considered in selecting an appropriate filter stage. The equation shows that the white term depends on $1/\tau$; the 1/f term is independent of $\tau$ and that the parallel noise term is directly proportional to $\tau$. The constants from the integration ($r_x$) are the parts that determine the weight of each of the three types of noise. As a general rule it can be shown that the area of the filter determines the low frequency noise contributions, while the derivative determines the weight for the series noise.

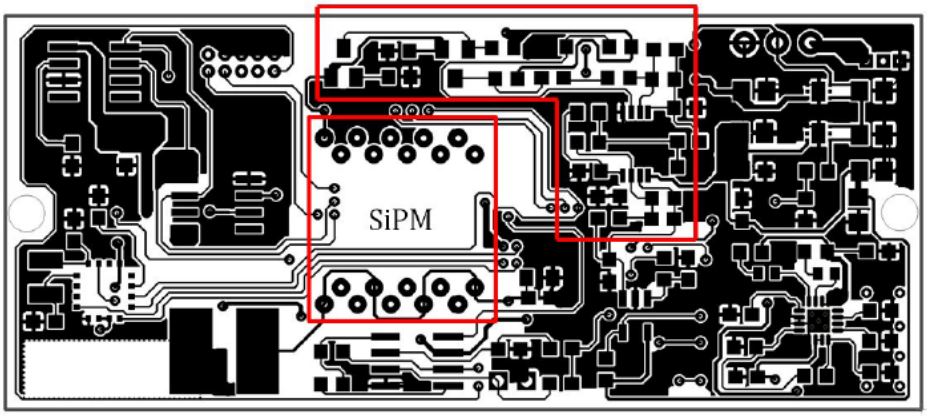
## 2.7 Printed Circuit Board design

The following paragraph describes the implementation of the physical design into a test board and it shows the validation tests that have been performed. The layout of the board, designed with Eagle Layout Editor (www.cadsoft.io) is shown in Figure 2.17.

The board has 2 layers and measures 7 cm x 3 cm. The analog front-end section and the SiPM location can be seen from Figure 2.17. The remaining sections on the board include DC-DC converter to generate the necessary bias to the circuits and the SiPM from a Li-polymer battery. It also includes a comparator that triggers on events, a microcontroller to coordinate between sensors and the external world, and communication circuits (USB, Bluetooth




(a)




(b)

Figure 2.17: Prototype board with top (a) and bottom (b) layer.

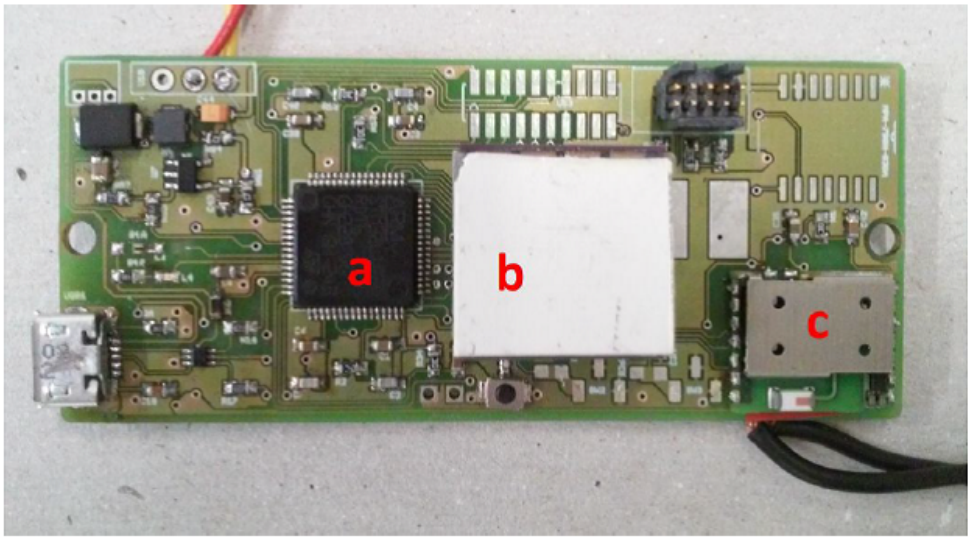



Figure 2.18: Picture of the fully assembled board. The microcontroller (a), SiPM coupled with a ZnS screen (b) and Bluetooth module are shown. The front-end electronics are located on the bottom layer.

and NFC). A picture of the assembled board is shown in Figure 2.18.

The readout electronics, in the preliminary design previously examined has been integrated with a suite of sensors as the application requirements mandate. The block diagram of the developed system is depicted in Figure 2.19. Additionally to the electronic read-out components, previously described, the device includes an ultra-low-power 32-bit micro-controller (STMicroelectronics, STM32L162RD) that directs the operations of all the sensors presents on-board. The main features of such a micro-controller are reported in Table 2.7. It features a current consumption per MHz down to 238 $\mu$A/MHz, a dynamic core voltage scaling, a very fast wake-up time from stand-by mode and an almost negligible leakage from GPIOs. Moreover, the power consumption in stop mode with an active Real Time Clock is only 1.7 $\mu$A. Such a low power consumption is a key feature for the prototype, in order to have a portable, compact and long-term functional device. For obvious reasons not all the specifications are reported in Table 2.7, but can be found at [27]. The micro-controller has been programmed in order to receive the comparator signal from the analog front-end circuit and to collect environmental data from temperature, humidity

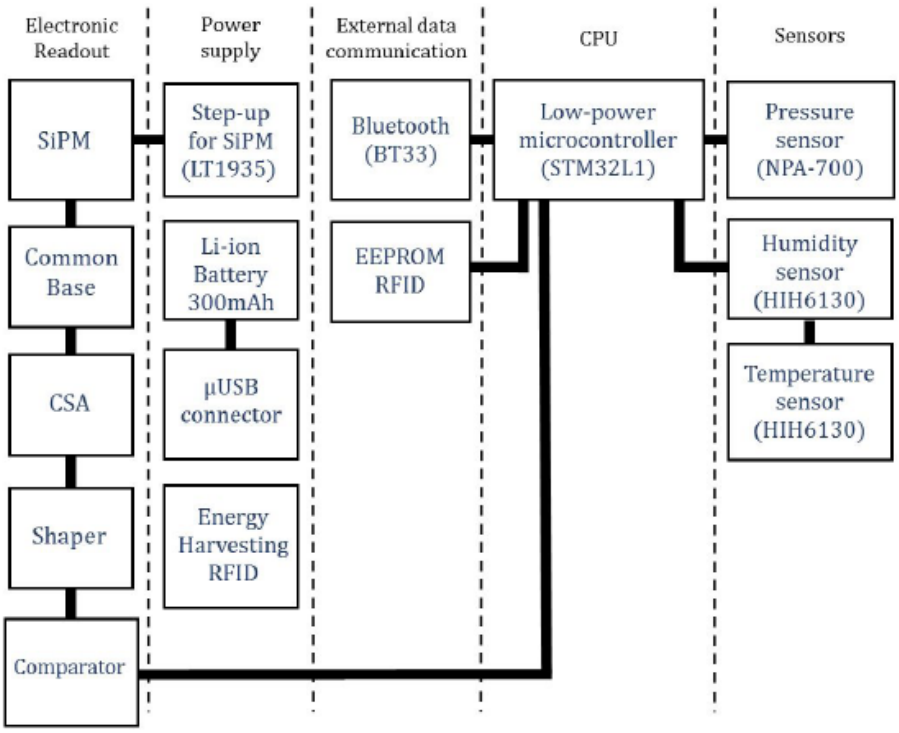



Figure 2.19: System block diagram.

| *Parameters* | *Values* |
|---|---|
| Power supply | 1.65 V to 3.6 V |
| Current consumption | 238 uA/MHz (Run mode) |
| Core | ARM 32-bit Cortex-M3 CPU |
| Frequency | 32 kHz up to 32 MHz max |
| Memories | 46 KB RAM, 384 KB Flash |
| Clock main source | 1 to 24 MHz |
| Rich analog peripherals | 12-bit ADC, 2 12-bit DAC |
| Timers | 11 |

Table 2.7: Main characteristics of the micro-controller.

and pressure sensors.

Wireless communication is implemented by a Bluetooth module (BT33, Amp'ed RF, [28]). Table 2.8 reports the main features of such a module. The

| *Parameters* | *Values* |
|---|---|
| Version | v 3.0 |
| Dimensions | 11.6 x 13.5 $mm^2$ |
| Supply voltage | 2.5 V (typ) |
| Current consumption @32 MHz | 23 mA (transfer), 9.1 mA (connection) |
| Core | Cotex-M3 microprocessor up to 72 MHz |
| Memories | 256K bytes Flash and 48K bytes RAM |
| Interfaces | SPI and I2C |

Table 2.8: Main characteristics of the Bluetooth module used for wireless transmission.

BT33 is a surface mount PCB module that provides fully embedded, ready to use Bluetooth wireless technology. The standard abSerial and Amp'edUP protocol Stack are pre-flashed into the integrated flash memory, supporting the SPP and IAP profiles. This transfers to an external device (PC or mobile devices) the acquired sensors data and the Radon concentration value calculated by the system. The wireless transfer can also works through radio frequency communication (RFID) thanks to a dual interface EEPROM memory (STMicroelectronics, M24LR64, [29]) present on-board and connected with a planar antenna. Infact the RFID communication, compliant with ISO-15693

protocol, offers the possibility of reading the processed data (Radon concentration) via an external RFID reader, without additional power consumption in the system. Basically, this technology uses communication via electromagnetic waves to exchange data between an interrogator (also known as the reader) and an object (transponder or tag). The communication must respect given standards, as the protocol ISO 15693. The 13.56 MHz carrier electromagnetic wave is ASK (Amplitude Shift Keying) modulated for data transmission [30]. In general, the transponder is composed by an integrated circuit for storing and processing data and an antenna for receiving and transmitting them. The electromagnetic field generated by the interrogator provides the power to the transponder for the data communication, achieving a wireless link with no power consumption on the transponder side. This feature is rather important for reaching the system requirement related to low power consumption. Unlike other wireless technologies, the obtainable data rate is quite limited, suggesting a one-shot measurement operation or an on-board data processing in order to optimize the transmission time.

The platform is powered by a Li-ion rechargeable battery with 300 mAh capacity. It also has small dimensions: 33x28x3.5 $mm^3$. The battery can be recharged either via micro-USB connector or energy harvesting RFID devices, according to the most modern charging standards. In order to supply the system, according to methods described above, the PCB includes a battery charger (STMicroelectronics, L6924D), a $\mu$USB and two Low Drop Out (LDO) voltage regulators (STMicroelectronics, LDLN015PU28R). Having two different LDO permits to better manage the power supply and to discriminate the supply from Analog Front-End to the micro-controller. Furthermore, the breakdown voltage of the SiPM, equal to 29 V, is provided thanks to a boost DC/DC converter (Linear Technology, LT1935ESTR), working with 1.2 MHz switching frequency. In particular, it steps up voltage (while stepping down current) from its input to its output. In normal condition, with an input voltage of 5 V and output of 12 V, the current is equal to 600 mA. The board is assembled on a two layers 80x34 $mm^2$ standard FR4 PCB with commercial components (see Figure 2.18). It also hosts a RTC clock external to the micro-controller, that permits to perform a chronological record of the acquired data. In this way, it is possible to process data and store them according to the accurate and precise instant of time.

The aim of the firmware is to control SiPM bias, each configured timer and interrupts and to monitor the output comparator voltage for the signals. First of all, the micro-controller sets the DC threshold for the comparator ($V_B$ in schema 2.13), through an internal DAC. The threshold is equal to 1.4 V. As previously described in paragraph 1.5.3, this value correspond to the midpoint of the DC bias of the circuit. When the system is enabled, the micro-controller receives the pulses coming from the output comparator and it increments a variable. The number of pulses represents the count of alpha particle that reaches the SiPM active area. In order to calculate the mean value of the counted particles and then the number of Radon decays per second (in Becquerel), we configured an internal Real Time Clock (RTC), that enables an interrupt for reading the incremented variable every 60 seconds. The calculated value is transmitted by Bluetooth to an external device, previously paired with the platform. In addition to Radon concentration, the Bluetooth module transmits each minute humidity and temperature values given by the humidity sensor (Honeywell, HIH6130, [31]) and of the absolute pressure by the pressure sensor (General Electric, NPA-700, [32]). The fully assembled system is shown in Figure 2.20.

## 2.8 System measurements

Preliminary system measurements were carried out in the laboratory setting, in order to validate the readout electronics connected to the Silicon Photomultiplier. First of all, some tests have been performed in order to count the number of events seen by the detector. The experiments have been executed placing an alpha source (1nCi Am-241) on the active area of the ZnS scintillator coupled with the SiPM (see Figure 2.21). The system and the radioactive source have been placed in a dark enclosed box without system ventilation, in order to prevent incoming light photons from outside. Figure 2.22 show the alpha response of the analog front-end with one pixel and the whole matrix (16 pixels) of the SiPM connected at the input. It is worth mentioning that the peak duration of one alpha signal is less then 1 ms. RMS values of the baseline were calculated when 1 pixel is connected (2 mV) and with the whole SiPM-array linked (63.5 mV). High SNR allows easy discrimination between alpha pulses and noise. Furthermore, the peaks count was performed varying the distance

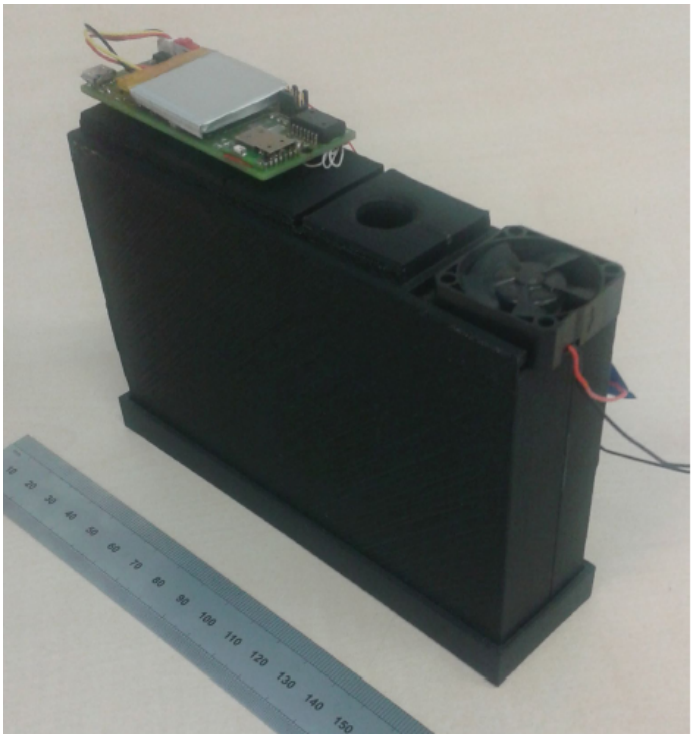


Figure 2.20: Fully assembled system.

between the alpha source and the detector. Data acquisition are reported in Table 2.9. The plot in Figure 2.23 shows the cumulative histogram of the peak

| ***Distance Source-Detector (cm)*** | ***Duration (hours)*** | ***Event rate (Counts/sec)*** |
|---|---|---|
| 3 | 1 | 0 |
| 0.5 | 1 | 788 |
| Contact | 1 | 1048 |
| Contact | 8 | 1168 |

Table 2.9: Data acquisition.

counts obtained during a 1 hour long acquisition where the source was placed on the detector. The mean count value is 1048 counts per second. The 10% difference between the 1-hour and the 8-hours acquisition demonstrates that the system gives a sufficiently reliable value of alpha decay rate within one hour.

After that, preliminary system measurements were done in the laboratory on

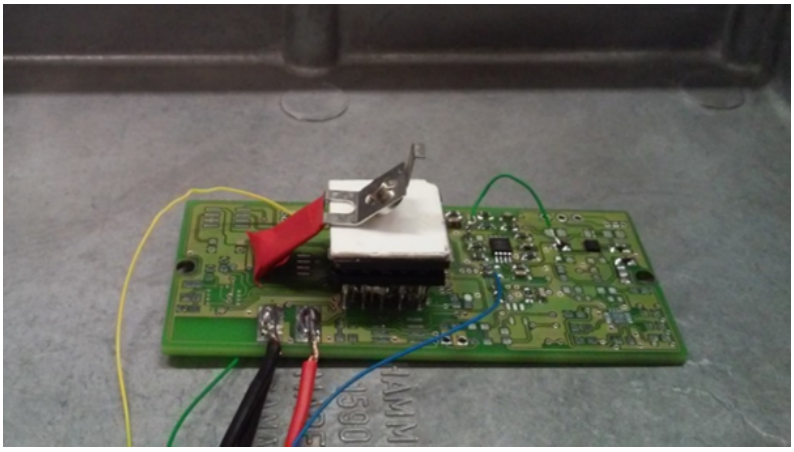
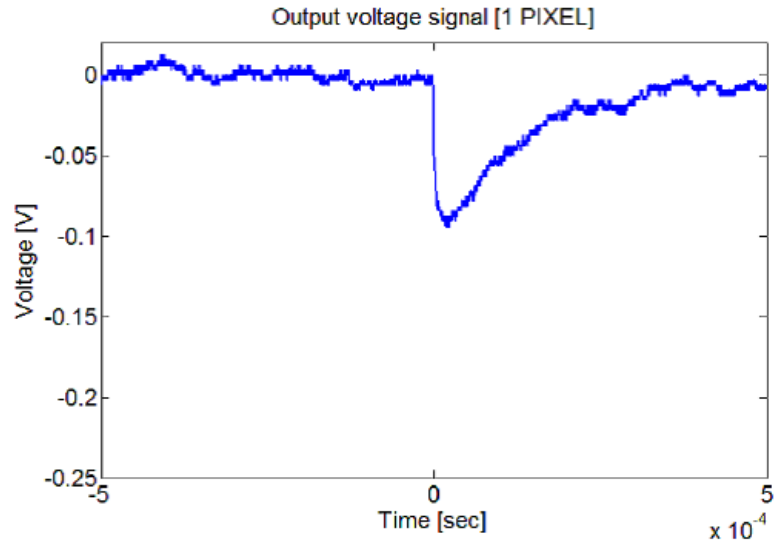
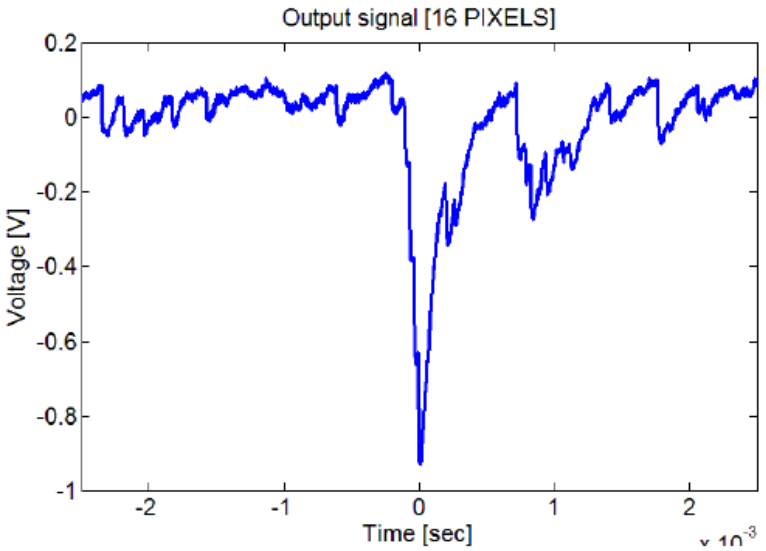


Figure 2.21: Preliminary measurement setup.

a time span of about 167 hours (roughly 7 days), in order to validate the whole system with tube ventilation, fan and the electronic platform. Radon counts and data from humidity, temperature and pressure sensors were extracted. The resulting plots are shown in Figure 2.24. Note that the count rate is of the order of 100 Bq/m$^3$, or about 10 counts per minute in the detector. This number corresponds to 2.7 pCi/l, quite comparable to the rates expected to measure in many practical scenarios. The statistics associated with this count rate is of the order of $10/\sqrt{10} = 3$ counts per minute. Thus, significant variance in the data is expected, if plotted as a series of one minute-long acquisitions. For this reason, some smoothing have been applied after collection. After that, some attempts were made to establish if a correlation exists between the radon dataset and humidity, temperature and atmospheric pressure. Access to the laboratory was controlled by a normally closed door. The system was programmed to record Radon activity, temperature, relative humidity and absolute atmospheric pressure each minute for about 167 hours. The stored results of Radon concentration was averaged hourly. The resulting plot is shown in Figure 2.25, where the patterns present in the original data series are still clearly visible. Of course, the data can be smoothed further by, for example, opting for hour-long averages. This is a practical system choice to be optimized after more measurements have been done. Some attempts to establish if a correlation between the Radon dataset and humidity, temperature and atmospheric pressure exists were made, but no obvious correlation was found (0.4, -0.7 and 0.4 for the respective correlation factors). This is expected, as the




(a)




(b)

Figure 2.22: Output voltage signal with 1 pixel (a) and 16 pixels (b) connected to the analog front-end.

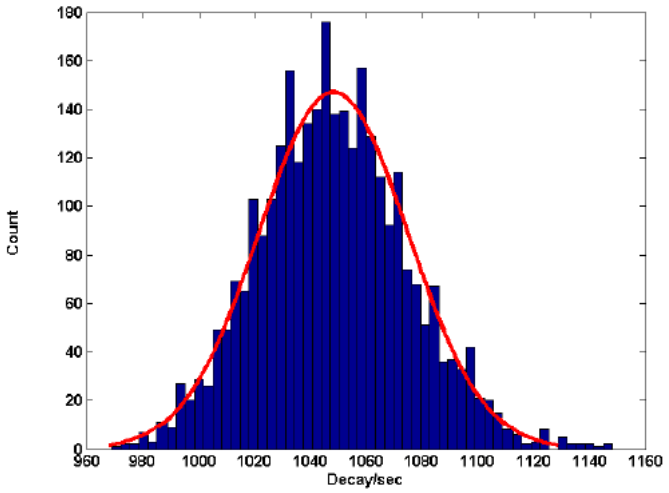



Figure 2.23: Histogram of the event rate.

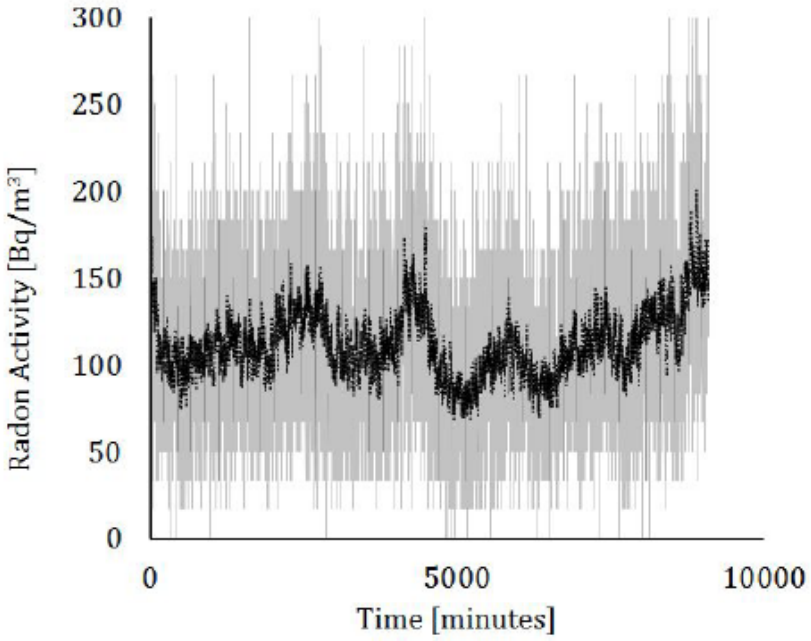



Figure 2.24: Acquired radon activity data before (black line) and after (gray line) smoothing.

variations in values are rather small. The most interesting result is the weak correlation between the temperature curve and the Radon counts. A strong correlation would indicate that either the Radon concentration depends directly

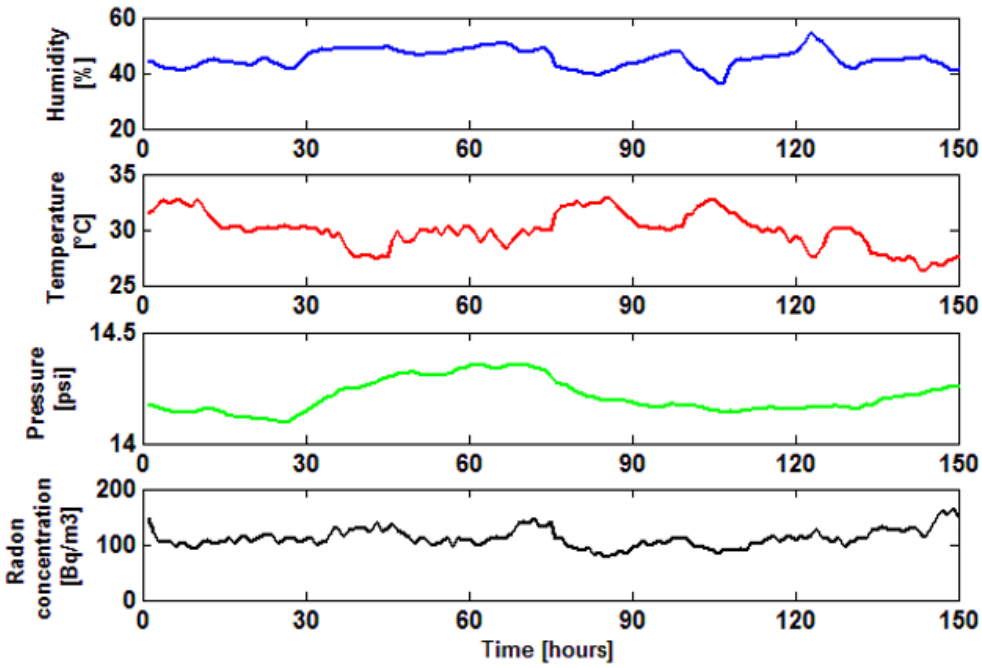



Figure 2.25: Smoothed radon activity data and environmental data.

on temperature (not substantiated by research), or that some of the electronics readout settings drift with temperature (most likely the SiPM gain and/or the low-energy threshold). Obviously, if temperature behavior were a concern, a more in-depth analysis would be necessary. Moreover, the acquisition shows that the maximum Radon level in the laboratory was observed during the night, when the doors are closed and there is no exchange between indoor and outdoor air. The averaged Radon activity values obtained from the previous acquisitions resulted to be comparable with the mean value (110 $BQ/m^3$) measured by a commercial device (Corentium Canary [33]) (90 $BQ/m^3$). However, further studies and long term acquisitions and calibrations are needed for obtaining an efficient comparison between both the results. The reason of this is that Corentium device is able to give reliable values of Radon concentration only after several weeks. Moreover, the developed platform, currently, doesn't detect the amplitude of the alpha peaks, so it is unable to discriminate the overlapping alpha particles that simultaneously hit the sensitive area of the scintillator.

The last step of the process has been the development of a simple software for

continuous visualization of trend data. The PC software has been implemented with C# programming language. The logical process behind the software includes the following steps:

- Bluetooth coupling between the board and software, in order to establish the connection;
- Importing of raw data concerning Radon concentration, temperature, atmospheric pressure, humidity from the platform;
- Conversion and smoothing of such data;
- Continuous visualization on 4 different plots;
- Data saving on text file.

## 2.9 Conclusion

In this chapter an application of the design criteria for SiPM-based systems to a very simple case, where a relatively large SiPM is used to read out a scintillator, has been shown.

A wireless, battery-powered portable prototype of Radon sensor has been built featuring a SiPM as the alpha particle detector and a simple readout electronics. The developed system composed by fan, ventilation tube, a SiPM coupled with a scintillator as alpha detector and electronic components, has been designed. The aim is to measure continuous Radon indoor concentrations and to provide reliable values in a few hours (about three). The platform is able to record environmental data (relative humidity, temperature, absolute atmosphere pressure) each minute and to communicate them via Bluetooth to a smart device (PC or mobile devices). This permits to give a correlation between environmental parameter fluctuations and Radon concentration. Preliminary measurements have demonstrated a weak correlation between the temperature curve and the Radon counts.

CHAPTER 3

# Design of Analog Front-End for future pixel detectors

## 3.1 Introduction

The second part of this thesis work is dedicated to the development of a new CMS Pixel (called IFCP65) mixed signal ASIC that has been designed as a prototype front-end for the HL-LHC pixel readout system. The ASIC requirements for sensor development are to have fine pitch and be compatible with thin sensors which translate to operating with low thresholds. The ASIC front-end includes signal processing and synchronous analog-to-digital conversion (ADC) within one Bunch Crossing Clock (BXClk) period.

The emphasis of the work presented during this thesis is on the feasibility of a synchronous ADC within the HL-LHC environment. In particular, the aim of this chip is to demonstrate the feasibility of the third generation of pixel front-end ASICs using for the first time the 65 nm CMOS technology in the High Energy Physics (HEP) community. The feasibility demonstration is done despite the very harsh radiation environment, the very high resolution requirements and the necessity to comply with very high particle rates. Using synchronous approach for processing within 25 ns, power consumption is the

limiting factor. With the advent of accessible modern technologies with minimum gate length of 65 nm and below, the processing speed can be achieved without the prohibitive expense of power. Such a technology is confirmed to be suitable for radiation hard analog design [34]. Together with others pixel front-ends, in the framework of RD53 collaboration, IFCP65 has been proposed as one candidate for the next generation of HL-LHC pixel readout systems.

The chapter is organized in eight sections. The first section describes the motivation and outlines. The second part provides more details on system requirements. Thus, the third section offers a conceptual description of the synchronous ADC, along with its advantages and implementation methodology. The fourth section discusses the transistor level design details of the preamplifier with a leakage current compensation technique along with an innovative auto-zero comparator design and verification simulations. The fifth section explains the designed layout, thus post-layout simulations performed. Test results are reported in the sixth section. The seventh section discusses a possible design of the readout digital section, but not yet implemented. Finally, the last section of the chapter concludes and summarizes the material presented.

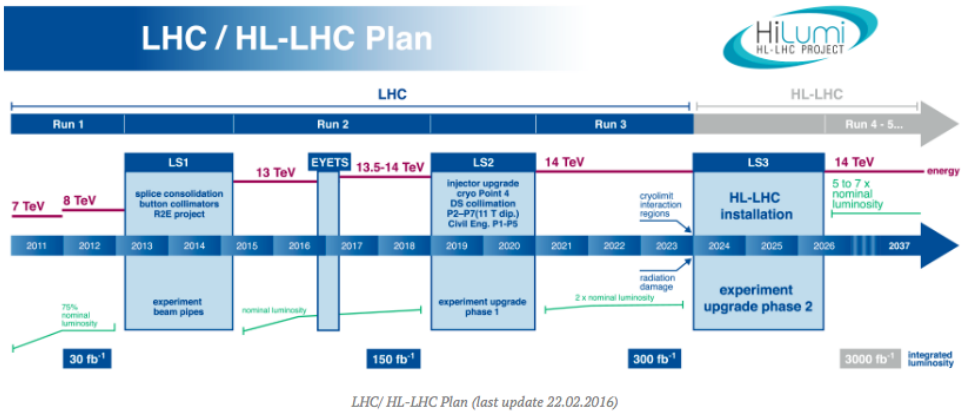
## 3.2 Motivation and Outlines

### 3.2.1 The Large Hadron Collider (LHC)

The Large Hadron Collider (LHC) at CERN is the world's largest and most powerful accelerator. The main goal of this experiment is to study the basic constituents of matter and the fundamental particles. The particles are made to collide together at close to the speed of light. The process gives the physicists clues about how the particles interact, and provides insights into the fundamental laws of nature. LHC consists of a 27-kilometer ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles along the way. Inside the accelerator, two high-energy particle beams travel at close to the speed of light before they are made to collide. The beams travel in opposite directions in separate beam pipes: two tubes kept at ultrahigh vacuum. They are guided around the accelerator ring by a strong magnetic field maintained by superconducting electromagnets. The electromagnets are built from coils of special electric cable that operates in a

superconducting state, efficiently conducting electricity without resistance or loss of energy. This requires chilling the magnets to -271.3 ℃, a temperature colder than outer space. For this reason, much of the accelerator is connected to a distribution system of liquid helium, which cools the magnets, as well as to other supply services. Thousands of magnets of different varieties and sizes are used to direct the beams around the accelerator. The beams inside the LHC are made to collide at four locations around the accelerator ring, corresponding to the positions of four particle detectors: A Toroidal LHC Apparatus (ATLAS), Compact Muon Solenoid (CMS), A Large Ion Collider Experiment (ALICE) and Large Hadron Collider beauty (LHCb) [35]. Although they use different technical solutions and magnet-system designs, they have the same scientific goals: studying the Standard Model (including the Higgs boson) to search for extra dimensions and particles that could make up dark matter.

In 2013-2014, the LHC underwent the first planned Long Shut-down, called LS1. The aim of this operation was to improve the machine performance. After the first shut-down, beam energies between 7 TeV and 14 TeV were achieved. A second shut-down (LS2) is foreseen in the 2018-2019 period. In that occasion, the LHC luminosity will be raised to twice the nominal luminosity. This performance improvement, called 'phase 1 upgrade', will also require an upgrade of the detectors, because the present version of the detector could not be operated in the environment of the upgraded accelerator. A new version of the pixel detectors will be introduced in 2018- 2019. Figure 3.1 shows the LHC upgrade timeline. LHC will undergo another long shut-down period, called LS3, from 2023 to 2025, during which the High Luminosity HL-LHC will be installed. Its name comes from the huge luminosity of the collider: the beam energy will reach about 14 TeV and the luminosity will be increased by a factor of 5 to 7 with respect to the nominal luminosity. During such a long shut-down LS3, the CMS experiment, and also the ATLAS itself, will be upgraded (Phase-2 upgrade), to comply with the increased environment hostility. In the ALICE and LHCb experiments, major detector upgrades are instead foreseen during LS2 [36].




*LHC/ HL-LHC Plan (last update 22.02.2016)*

Figure 3.1: LHC timeline.

### 3.2.2 CMS: The particle detector

Coming into details on one of the four particle detectors, i.e. CMS, the structure of it is shown in Figure 3.2. The CMS detector has approximately the shape of a cylinder 21.6 m high with a diameter of 16.6 m. The total weight of the detector is about 14000 tonnes. It is located in an underground cavern at Cessy in France, just across the border from Geneva. In July 2012, along with ATLAS, CMS discovered the Higgs boson. As most of the elementary particles detectors, CMS is made up of different subsystems for detecting the type of particle and measuring energy and momentum of photons, electrons, muons and other phenomenas (i.e. jets of hadrons) produced during proton-proton collisions. The detector is built around a huge solenoid magnet, in order to take advantage of the properties of the charged particles: the higher a charged particle momentum, the less its path is curved in the magnetic field. Thus, once its path has been tracked, its momentum can be calculated. A strong magnet is therefore needed to enable accurate measurements even of the very high momentum particles, such as muons. The solenoid takes the form of a cylindrical coil of a superconducting cable that generates a magnetic field of 4 T.

It is based on several layers, from the innermost layer to the outside there are:

- a tracker entirely in Silicium;
- an electromagnetic calorimeter (ECAL), composed of about 80000 scin-

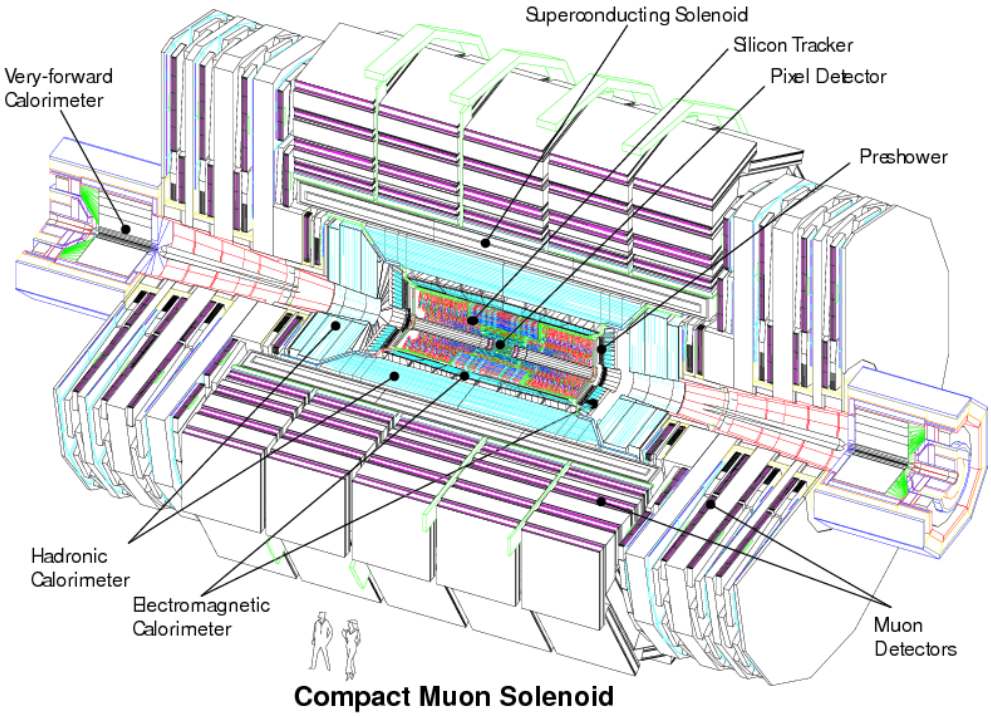



Figure 3.2: An exploded view of the CMS detector

tillating crystals of lead tungstate ($PbWO_4$);

- an hadronic calorimeter (HCAL), composed of interrelated layers of dense material and plastic scintillators or quarts fibers;

- a superconducting solenoid magnet that incorporates the three previous subdetectors and dunk them into a strong and homogeneous magnetic field of 4 T;

- outside the magnet, there are muons chambers (only such particles are sufficiently penetrating and able to pass through the overall internal detectors) placed inside the yoke of the magnet.

Figure 3.3 presents the transverse section of the CMS detector, where the layers just described are clearly visible.

The tracker can reconstruct the paths of high-energy muons, electrons and hadrons. It needs to record particle paths accurately yet be lightweight so as to disturb the particle as little as possible. It does this by taking position measurements so accurate that tracks can be reliably reconstructed using just

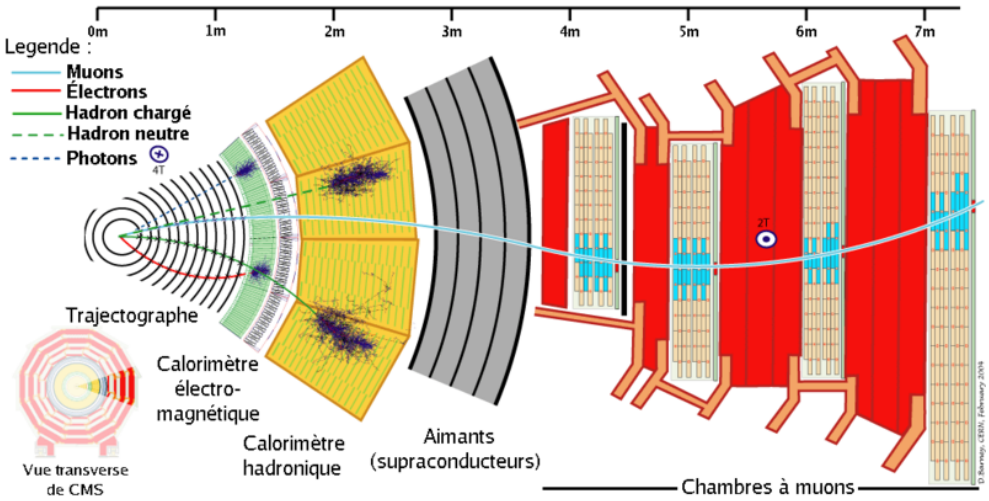



Figure 3.3: Transverse section of the CMS detector.

a few measurement points. Each measurement is accurate to 10 $\mu$m. It is also the inner most layer of the detector and so receives the highest volume of particles: the construction materials were therefore carefully chosen to resist radiation. The final design consists of a tracker made entirely of silicon: the pixels, at the very core of the detector and dealing with the highest intensity of particles, and the silicon microstrip detectors that surround it. As particles travel through the tracker the pixels and microstrips produce tiny electric signals that are amplified and detected. The tracker is composed by 13 layers in the central region and 14 layers in the endcaps. The innermost three layers (up to 11 cm radius from the interaction point) consist of 100x150 $\mu$m pixels. The next four layers (up to 55 cm radius) consist of 10 cm x 180 $\mu$m silicon strips, followed by the remaining six layers of 25 cm x 180 $\mu$m strips, out to a radius of 1.1 m. With a total active silicon area of 205 m$^2$, the CMS tracker is the largest full-silicon tracking system, with 1440 pixel-modules and 14148 strip modules, corresponding to 66 million pixels and 9.3 milion silicon strips.

The tracking system is followed by the electromagnetic calorimeter (ECAL), which is designed to measure with high accuracy the energies of electrons and photons. The ECAL, made up of a barrel section and two "endcaps", forms a layer between the tracker and the HCAL. For extra spatial precision, the ECAL also contains preshower detectors that sit in front of the endcaps. These allow CMS to distinguish between single high-energy photons (often signs of

exciting physics) and the less interesting close pairs of low-energy photons. At the endcaps the ECAL inner surface is covered by the preshower subdetector, consisting of two layers of lead interleaved with two layers of silicon strip detectors. Its purpose is to aid in pion-photon discrimination.

The third detector is the hadronic calorimeter (HCAL), which it measures the energy of hadrons, particles made of quarks and gluons (for example protons, neutrons, pions and kaons). Additionally it provides indirect measurement of the presence of non-interacting, uncharged particles such as neutrinos [38].

The fourth layer is the CMS magnet, the central device around which the experiment is built, with a 4 Tesla magnetic field. This allows the charge/mass ratio of particles to be determined from the curved track that they follow in the magnetic field. It is 13 m long and 6 m in diameter. The job of the big magnet is to bend the paths of particles emerging from high-energy collisions in the LHC. The more momentum a particle has the less its path is curved by the magnetic field, so tracing its path gives a measure of momentum. CMS began with the aim of having the strongest magnet possible because a higher strength field bends paths more and, combined with high-precision position measurements in the tracker and muon detectors, this allows accurate measurement of the momentum of even high-energy particles.

The last detector is the one dedicated to muon detection and is the farthest from the beam interaction point, because muons can penetrate several meters of iron without interaction. As the name "Compact Muon Solenoid" suggests, detecting muons is one of CMS's most important tasks. Muons are charged particles that are just like electrons and positrons, but are 200 times more massive. Because muons can penetrate several metres of iron without interacting, unlike most particles they are not stopped by any of CMS's calorimeters.

### 3.2.3 The CMS pixel detector

The pixel vertex detector is the center of the particle detector and it is located very close to the interaction point (about 4 cm from it). For Phase-2 upgrade, pixel detector has stringent requirements with respect to spatial resolution, radiation hardness (up to the level corresponding to integrating luminosity of 3000 $fb^{-1}$), event pile-up (up to 200) and data bandwidth. The data measured by the pixel detector is of special importance in the reconstruction of the track starting point for both ATLAS and CMS. It is arranged in 4 layers in a barrel

geometry (see Figure 3.4).

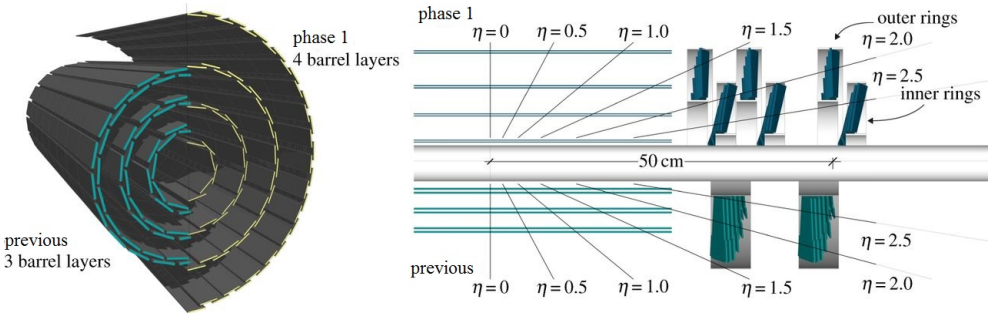



Figure 3.4: Barrel geometry of Phase-1 upgrade pixel detector compared to the previous phase.

The planned luminosity upgrade of the LHC to the High Luminosity LHC (HL-LHC) is proposed to operate at an instantaneous luminosity at $5x10^{34}$ $cm^{-2}s^{-1}$, and to deliver 250 $fb^{-1}$ per year for a further 10 years of operation. Thus it presents an extremely challenging environment to the experiments. Proton-proton collisions at the LHC occur synchronously with a period of 25 ns (40 MHz), which defines the bunch crossing clock (BXClk).

During the Phase-1 and Phase-2 upgrade, each pixel sensor cell that compose the pixel detector, is bump-bonded to a full-custom Application Specific Integrated Circuit (ASIC). Figure 3.5 represents the structure of hybrid pixel detector solution that is used by CMS.

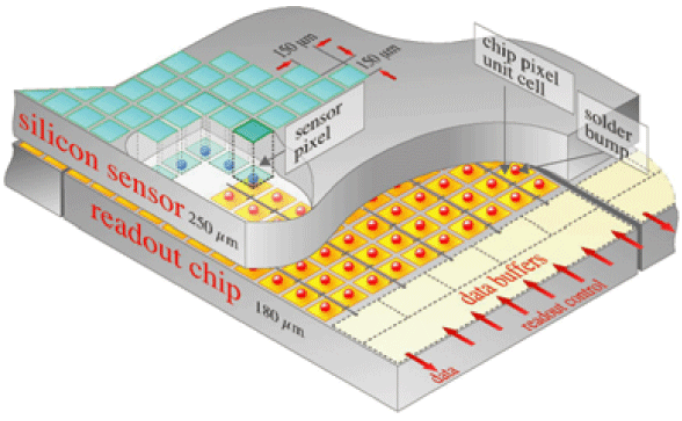



Figure 3.5: CMS silicon pixel detector.

The chip has been designed in a 250 nm CMOS technology for the primary

version and for Phase-1 upgrade, using special layout techniques which ensure the required radiation hardness. The lifetime of the tracker is limited by the damage in the silicon sensor. The innermost layer of the silicon pixel tracker has been designed in order to survive at least 2 years at the nominal LHC luminosity, while 10 years of lifetime is expected for the third layer. The ASIC chip for CMS Phase-1 upgrade is called PSI46DIG. Such an ASIC is an upgrade of the so called PSI46V2 ASIC, which was developed for the previous phase and it inherits the main features. Such improvements, including digital readout blocks, have been incorporated, in order to guarantee the high tracking performance required by the Phase-1 upgrade. The pixel sensor is composed by 52 columns x 80 rows. Each pixel has an area of 100 $\mu$m x 150 $\mu$m. The signal generated when a charged particle passes through the sensor is processed and read out by the ASIC bump-bonded to the sensor. The front-end system is composed by a charge sensitive amplifier (CSA) and a shaper. The area of PSI46DIG is 7.9 mm x 10.2 mm. In the chip, two adjacent columns are assembled in order to share services, such as power distribution, bias and data-buses. Each pixel cell has to provide some storage and buffering capabilities for the signals coming from the sensors. Moreover, the readout is performed in digital form, using a 40 MHz serial analog link. The PSI46DIG can be considered the second generation of the hybrid pixel detector for the Phase-1 CMS upgrade silicon tracker [39].

During the third long shutdown (LS3) of LHC, the collider will be upgraded to the High Luminosity LHC stage with a luminosity up to 5-7 times the nominal luminosity and energy of 14 TeV. Thus far, certain significant performance characteristics have been defined. The event pile-up is a major challenge with hit rates of up to 2 GHz/cm$^2$ for the inner pixel barrel requiring the increase of tracker granularity by a factor of four [40]. Furthermore, it requires the pixel vertex detectors to accurately track particles in the presence of and withstand a total ionizing dose (TID) of 1 Grad and a 1 MeV equivalent neutron fluence of 2x10$^{16}$ n/cm$^2$ over 10 years.

The pixel size is a critical aspect and the chosen one represents a trade-off between physics performance requirements, sensor technology, scale of integration of the front-end chip process and interconnection technology. The pixel size of the sensor for the inner tracker is 50 $\mu$m x 50 $\mu$m or 25 $\mu$m x 100

$\mu$m in order to guarantee the required resolution. In each pixel cell for the pixel detector ASIC, an analog front-end chain is integrated in order to perform the signal amplification and hit discrimination with a minimum detectable charge (close to 1 ke$^-$). Additionally, each pixel is required not to exceed a hit loss probability of $10^{-3}$ during its entire operational lifetime, which includes any loss of data caused either by the readout electronics or readout dead-time. Considering a pixel area of 2500 $\mu$m$^2$, the hit rate per pixel approximately ranges between 25-50 kHz. The rate of fake hits (noise hit rate) is required to be significantly less than the particle hit rate by at least a factor of three [41]. Furthermore, all hits within $\pm$2 ns of bunch collisions [40] must be assigned to the correct bunch crossing so that they can be accurately associated with related events. So a hybrid pixel detector located close to the interaction region of the colliding beams will provide high resolution tracking and vertex identification which will be crucial for b quark identification.

Pixel sensors similar to the ones used in the first generation LHC pixel detectors [42], [43] could be made sufficiently radiation tolerant if the active thickness were reduced from about 300 $\mu$m to 100 $\mu$m [44]. However, this would reduce the signal size by a factor of three. Since the signal size will be further reduced by radiation damage, this type of sensor will not be capable of efficient operation unless a pixel readout chip is developed in order to allow stable operation with a low threshold.

To summarize, the main requirements of the new pixel detector ASIC are:

- increased granularity, with pixels 50 $\mu$m x 50 $\mu$m in area;
- higher radiation hardness for the innermost layer. Indeed the working period in very harsh radiation environment is supposed to be 10 years with up to 1 Grad total dose;
- low power consumption, with a power budget around 0.4 W/cm$^2$ and an estimated front-end chip area of 4 cm$^2$.

Integrated circuit design in such harsh environment is challenging and unique and has been discussed in detail [45]. 65 nm CMOS technology has been chosen as the technology for the design of the new pixel detector for the Phase 2 upgrade. Such a technology retains good degree of tolerance to ionizing radiation that is typical of CMOS processes in the 100 nm regime.

Different experimental measurements have been carried out in order to confirm the radiation tolerance [34], [46], [47]. As compared to the 250 nm CMOS technology used for the previous generations of front-end chips, it can offer larger speed and low power consumption. The 65 nm CMOS technology is used for the first time in High Energy Physics (HEP) experiments. Nevertheless, it is a mature technology, used in many commercial applications and it guarantees long-term availability. The latter characteristic is very important, because it will have to be available for the time the Phase 2 upgrade becomes operational (2022-23) and for several years after that.

Figure 3.6 shows the block diagram of the hierarchical organization of the front-end chip for the innermost layer of CMS silicon tracker. A small signal must be detected and amplified in each pixel by a low noise charge sensitive amplifier and digitized for further processing. The large number of pixels (100k - 1M) implies that the analog circuit design has to address some critical aspects for physical layout area and for very low power consumption. To overcome these limitations, a design approach based on subdividing the chip array in regions of 4x4 pixel cells will be explored in order to share digital resources.

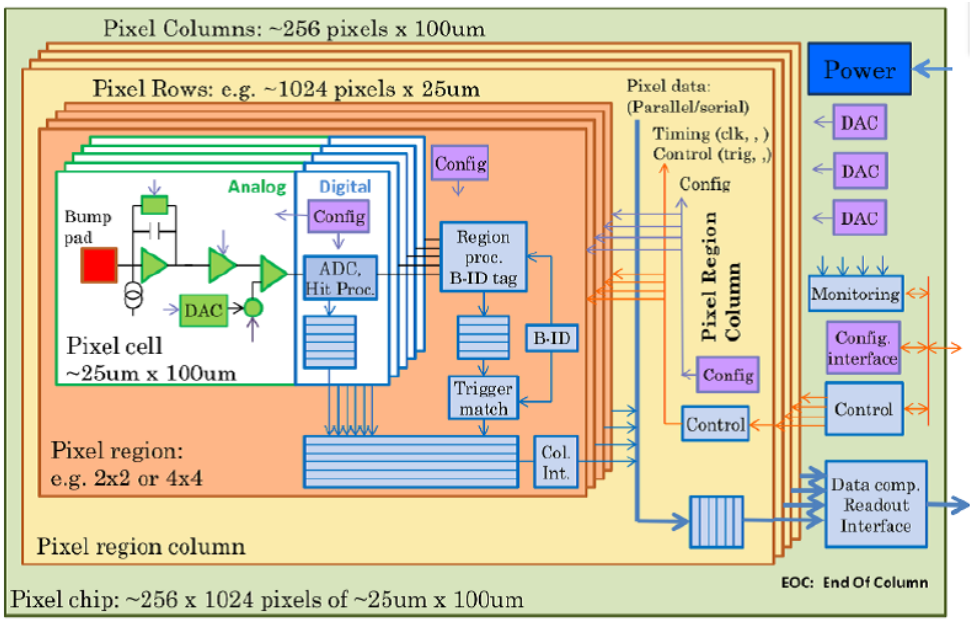



Figure 3.6: Block diagram of pixel chip for the inner layer of the CMS silicon tracker.

The CERN RD53 collaboration has been setup to investigate new pixel detectors for this proposed environment [37]. In particular, the aim of such a collaboration is to design the next generation of hybrid pixel readout chips to enable the ATLAS and CMS Phase 2 pixel upgrades. This collaboration, started in 2013, includes different research groups and is specifically focused on design of hybrid pixel readout chips. Thus the target is not on more general chip design or on other aspects of hybrid pixel technology. In particular, the goals of RD53, using 65 nm technology, are the followings:

- Development guidelines for radiation hardness in 65 nm CMOS technology;
- Development of tools and methodology to efficiently design large complex mixed signal chips;
- Design and characterization of circuits and building blocks needed for pixel chips;
- Design and characterization of full scale demonstrator pixel chip (called *RD53A*). Such a demonstrator will contain 3 different analog readout channels, and is not intended to be a production chip. Moreover, it will contain design variations for testing purposes.

Thus, the aim of RD53A chip is to demonstrate, in a 65 nm CMOS technology, stable low threshold operation and compatibility with high hit and trigger rate, as required for HL-LHC upgrades of ATLAS and CMS, in a large format Integrated Circuit (IC). The requirements for pixel detector ASIC for CMS and ATLAS, while not identical, are quite similar. Table 3.1 shows the increase in design complexity, upgrading from LHC to HL-LHC pixel.

The preliminary floorplan of the RD53A chip is based on the pixel matrix, where each pixel is an analog island, surrounded by a digital sea. Such design methodology is a new approach used in High Energy Particle community, which enable the use of place. In particular, each pixel region is composed by a 4x4 analog pixel cell that shares the digital function (i.e. buffering and time-stamp generation). For each two columns of pixels, there is a column base block at the end of the column. Such block provides the biasing, voltage reference and the calibration levels for the pixels in the columns. The pixel matrix will include three topologies of analog front-end, each one with a bump-bond pad

| *Parameters* | *LHC* | *HL-LHC* |
|---|---|---|
| Luminosity | $6x10^{33}$ $cm^{-2}s^{-1}$ to deliver 25 $fb^{-1}$ per year | $5x10^{34}$ $cm^{-2}s^{-1}$ to deliver 250 $fb^{-1}$ per year |
| Radiation dose (10 years) | 10-30 MRad, $10^{15}$ neutron/$cm^2$ | 1 GRad, $2x10^{16}$ neutron/$cm^2$ |
| Hit rate for inner pixel barrel | 200 MHz/$cm^2$ | 2 GHz/$cm^2$ |
| Pixel area | 20000 $\mu m^2$ | 2500 $\mu m^2$ |
| Number of pixels | 100 M | 650 M |
| Power | 0.25 W/$cm^2$ | 0.5 - 1 W/$cm^2$ |
| Data bandwidth | 160 Mbps/$cm^2$ | $>$ 1 Gbps/$cm^2$ |

Table 3.1: CMS pixel detector parameters.

at the channel input for interconnection with the sensor. Such analog front-end are designed by three different Institutes: the Lawrence Berkeley National Laboratory (LBNL), the Universities of Bergamo and Pavia and also INFN of Pavia and Torino.

## 3.3 Design requirements

In order to design a pixel front-end, able to work in HL-LHC environment, it is necessary to define a set of analog requirements and specifications which the circuit has to comply with. These requirements and specifications were dictated by RD53 collaboration.

While the experiments plan to use one readout chip throughout the entire pixel detector, the critical performance requirements are defined by the innermost layer, which will be at a radius of 3-4 cm from the HL-LHC interactions. Use in outer layers introduces additional requirements, such as large format for low cost assembly, aggregation of multi-chip module data, possibility to operate with reduced power and larger pixels, etc. However the performance requirements are generally less demanding at higher radius. In simplest terms, the hybrid modules (readout chip plus sensor) must record the hit pixels and crossing times of 99% of incident charged particles, must hold this information until a trigger decision is received, and must read out the triggered information without loss, negligible fakes, and in a short enough time as needed for

higher level triggering. These requirements give rise to the quantitative main specifications in Table 3.2. Further details are provided in [50].

| ***Specification*** | ***Value*** | ***Test Conditions*** |
|---|---|---|
| Interior pixel capacitance | <100 fF | |
| Interior pixel leakage current | <10 nA | |
| Min. stable threshold setting | 600 $e^-$ | With 50 fF load, 4 $\mu$A/pixel analog. |
| Min. charge above Vth (result <25ns time walk) | 600 $e^-$ | With 50 fF load, 4 $\mu$A/pixel analog. |
| Min. in-time threshold (if use sync reset) | 750 $e^-$ | With 50 fF load, 4 $\mu$A/pixel analog. |
| Hit loss from in-pixel pileup | $\leqslant$ 1% | 75 kHz avg. hit rate. |
| Trigger rate | 1 MHz | |
| Trigger latency | 12.5 $\mu$s | |
| noise occupancy per pixel | $<10^{-6}$ | 50 fF load; in a 25 ns interval |
| Radiation dose | 500 MRad | |
| Analog current consumption | 4 $\mu$A/pixel | |
| Digital current consumption | <4 $\mu$A/pixel | |
| Total current consumption | <500 mA/cm$^2$ | 1 W/cm$^2$ |

Table 3.2: Main specifications related to critical performance requirements. Note that these specifications are to be met after 500 Mrad dose.

### 3.3.1 Radiation tolerance

The radiation hardness of the device is a key point to be taken into account in the design of Front-End for HEP applications, especially when devised for harsh environments. The chosen 65 nm technology has so far been extensively radiation tested up to a total dose of 300 MRad with very promising results [34]. For the Phase 2 upgrade in the pixel inner layer this characterization needs to be extended to 1 GRad. Initial indications have shown that certain P-MOS transistor parameters may experience a significant degradation above the 3 MGy level. These studies need to also be extended as a function of temperature. Significant additional work is required to develop an understanding of such effects. The HEP community has in the last few years been evaluating IC technologies to identify the appropriate one for the next generation of HEP

experiments. The current LHC experiments are primarily based on a 250 nm CMOS technology and on-going developments for Phase 1 upgrades have to a large extent moved to a 130 nm technology. The 65 nm CMOS technology node has been identified as a particular promising technology for long term Phase 2 developments. The 65 nm technology has by several foundries been defined as a "strong technology node" that will be available for a long time. It is also a technology that has excellent low power characteristics and has been shown to be well suited for the low noise analog functions needed in HEP applications. Thin gate oxides are a key ingredient for radiation tolerance [49]. The low power version of the 65 nm technology is used for the design of pixel front-end, since it is more suitable for this application.

### 3.3.2 Noise

The analog pixel front-end must be carefully optimized for the lowest possible power consumption with acceptable noise and detection thresholds. In particular, obtaining a low effective detection threshold (1000 $e^-$) with good uniformity across the whole pixel matrix in the presence of large amounts of digital logic is a main common challenge. Small pixels, thin sensors, and high radiation damage will result in significantly smaller signals than available today. For efficient chip design, some noise specifications have been defined. A 600 $e^-$ threshold should be efficient for signals from 50 $\mu$m MIP path length in silicon even with 50% charge loss after radiation damage. This means that a 600 $e^-$ signal will have a 50% probability of firing the discriminator, without any timing constraints, in a free-running discriminator design as used in present pixel detectors. At the HL-LHC with 25 ns bunch crossing period, time-walk is important, and a 600 $e^-$ overdrive has therefore specified, which means that (for the 600 $e^-$ minimum threshold setting) a 1200 $e^-$ signal will have a 50% probability of firing the discriminator with a time delay within 25 ns of very large signals. This does not mean that signals smaller than this 1200 $e^-$ in-time threshold will be lost, because digital processing will be used for time-walk compensation. However, such compensation may not be 100% efficient, so having an overdrive that is not very large is still important. Note that the 600 $e^-$ threshold (and 1200 $e^-$ in-time threshold) was specified for 50 fF capacitance per pixel, while the maximum pixel capacitance is specified as 100 fF. This reflects the need to have specifications that cover operation with a variety of

sensor options. This means that a sensor with capacitance close to the 100 fF limit must also provide more signal charge than one with 50 fF/pixel, so that one can operate with a slightly higher threshold to achieve the same required hit efficiency of 99%. A minimum in-time threshold of 750 $e^-$ was also specified a for 50 fF capacitance in case of a front end design that is synchronously reset with each bunch crossing, and thus signals that do not fire the discriminator within 25 ns are permanently lost.

Another key point concerning the noise is the noise occupancy, because it is important to have a low contamination of noise hits in the data. RD53A specifies this as a maximum noise occupancy per pixel of $10^{-6}$ (a dark count probability in an arbitrary 25 ns interval). Note that $10^{-6}$ noise occupancy means 0.1 noise hits per bunch crossing in a $10^5$ pixel chip, while the number of real hits from tracks in such a chip will be of the order of 100 in the inner layer or 10 in the outer layer. Translating this into a dark count rate gives 1.6 MHz/cm$^2$.

It is reasonable to even talk about the equivalent input noise charge (ENC) needed to achieve $10^{-6}$ noise occupancy at 600 $e^-$ threshold. For definition, the equivalent noise charge (ENC) is the number of electrons one would have to collect from a silicon sensor in order to create a signal equivalent to the noise of this sensor. Such parameter is calculated by injecting a known signal charge at the input and determining the signal-to-noise ratio at shaper output. The ENC is equal to the input charge for which S/N is equal to 1. The two main noise sources contributing to ENC are an input noise current ($i_n$) and an input noise voltage ($v_n$). The ENC is calculated by the following equation 3.1, considering both white and 1/f noise contributions:

$$ENC^2 = i_n^2 T_s F_i + C_i^2 v_n^2 \frac{F_v}{T_s} + C_i^2 \frac{F_v}{f} \tag{3.1}$$

Where:

- $T_s$ is the characteristic shaping time (e.g peaking time);
- $F_i$, $F_v$ the "Form Factors" that are determined by the shaping function of the pulse (calculated in the frequency domain for white terms or time domain for 1/f term);
- $C_i$ total capacitance at the input node (detector capacitance + input capacitance of preamplifier + stray capacitance + ...).

In particular, the current noise contribution increases with T and the voltage noise contribution decreases with increasing T, while considering white voltage and current noise sources, whereas 1/f voltage noise contribution is constant in T.

Coming back to the noise specification, clearly one must have ENC $< 126$ $e^-$, since a $10^{-6}$ probability corresponds to a Gaussian tail beyond $4.75\sigma$, but this is not sufficient. It is the quadrature sum of the ENC, the static threshold dispersion, and the RMS threshold fluctuations vs. time that must be less than 126 $e^-$ equivalent input charge. Simply assuming that these three contributions are equal results in a 73 $e^-$ ENC estimate, which is a reasonable target, but it is not a strict specification, as the importance of the other two contributions can be traded off. Threshold dispersion of the order of 40 $e^-$ after tuning is achieved in current detectors, and therefore a similar value should be achieved by RD53A, the full scale demonstrator pixel chip.

### 3.3.3 Power consumption

Because of constraints in the global power dissipation and power delivery to the pixel readout chip, the maximum current consumption for each pixel is set to be equal to 4 $\mu$A for the analog part and 4 $\mu$A for the digital itself (without including consumption in the periphery). In this way the total current consumption should be $< 500$ mA/cm$^2$, thus considering 1 W/cm$^2$ with 2 V input. Note that the global voltage is set to 2 V, whereas is decreased to 1.2 V within the pixel.

## 3.4 The synchronous ADC concept

This section describes in details the concept that inspired of the pixel front-end circuit that has been developed as a prototype for the HL-LHC pixel readout system.

### 3.4.1 Motivation and Basics

Most radiation detectors require pulse (or signal) processing electronics so that energy or time information involved with radiation interactions can be properly extracted. Traditionally the pixel electronics consists of a preamplifier followed by a continuous time shaping filter.

A preamplifier is the first component in a signal processing chain of a radiation detector. It collects the charge created within a detector and it acts as an interface between the detector and the pulse processing electronics that follow. The current pulse associated with the charge released into the sensor is brought to the pixel through the bump bond pad which connects to the input of a charge sensitive amplifier. The main function of a preamplifier is to extract the signal from the detector without significantly degrading the intrinsic signal-to-noise ratio. The schematic diagram of a common RC feedback charge sensitive preamp is shown in Figure 3.7. In the charge sensitive preamplifier

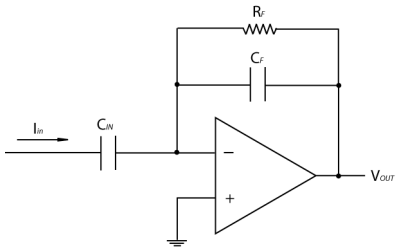



Figure 3.7: Block diagram of a common charge signal preamplifier (CSA).

(CSA), charge from the detector is collected on the feedback capacitor $C_f$ over a period of time, effectively integrating the detector current pulse. As the charge is collected, the voltage on the feedback capacitor rises and produces a step change in voltage. The output voltage is then proportional to the total integrated charge as long as the time constant $R_f C_f$ is sufficiently longer than the duration of the input pulse. In normal operation at ordinary counting rates, the rising step caused by each detector event rides on the exponential decay of a previous event due to the long decay time, thus the preamplifier output does not get a chance to return to the baseline. This does not create a serious problem since the significant information of the output pulse is in its rising edge and the shaping amplifier is capable of extracting the pulse height from the rising edge of each pulse. In order to count the pulses reliably, the preamplifier output signal must be shaped and amplified by a shaping amplifier and then the shaped linear pulses must be converted into logic pulses. The integral discriminator is the simplest unit that does this operation. It normally consists of a device that produces a logic output pulse only when the linear input pulse height exceeds a preset threshold, i.e. discriminator level. The logic

output pulse is normally produced shortly after the leading edge of the linear pulse crosses the discriminator level. The pulse shaping amplifier performs several essential functions. Its primary role is to magnify the amplitude of the preamplifier output pulse. In addition, the amplifier shapes the pulses to optimize the energy resolution, and to minimize the risk of overlap between successive pulses. Most amplifiers also incorporate a baseline restorer to ensure that the baseline between pulses is held rigidly at reference potential in spite of changes in counting rate or temperature. The output pulse rises slowly and reaches its maximum at $\tau$. This time interval, the time taken for the signal leading edge to rise from zero to maximum, is defined as the *peaking time*. Another conveniently used time interval is the *rise time*, which is defined as the time taken for the signal leading edge to rise from 10 to 90% of maximum. Frequently, the requirement to handle high counting rates is in conflict with the need for optimum energy resolution and low power consumption. For most radiation detectors, achieving the optimum energy resolution requires long pulse widths. On the other hand, short pulse widths are essential for high counting rates. In such cases, a compromise pulse width must be selected so that the detection system can be optimized.

In the case of LHC, obviously, the highest data rate means that the pixel needs to differentiate between two hits within two successive bunch crossings. This requires that the peaking time of the signal is less than 25 ns. However, fast shaping requires large power consumption stressing the available cooling capacity of the system. An alternative is to use a slower shaping time and compensate with sampling and post-processing techniques. As an example, in CMOS processes of minimum gate length larger than 250 nm, ASICs such as the APV family [51], use a slower shaper with 50 ns peaking time. After that they use a deconvolution mode to reconstructs the fast signal. Unfortunately, this technique results to be in higher noise. The main purpose is to reach a good trade-off between fast shaping, low power consumption and lower noise. A fast shaper necessitates a faster preamplifier. At the same time it further increases power consumption. Moreover, lower speed in the preamplifier prevents the amplitude of shaped signal to reach the maximum value as shown in Figure 3.8 due to ballistic deficit [52], which degrades signal-to-noise (SNR) ratio. In fact, such a ballistic effect occurs when short processing times are used to

permit high rate operation. This results from the fact that rise-time variations in the detector signal are reflected in amplitude fluctuations after the signals pass through pulse shapers. The ballistic deficit varies with time and hence inevitably leads to a loss of peak resolution in the final spectrum.

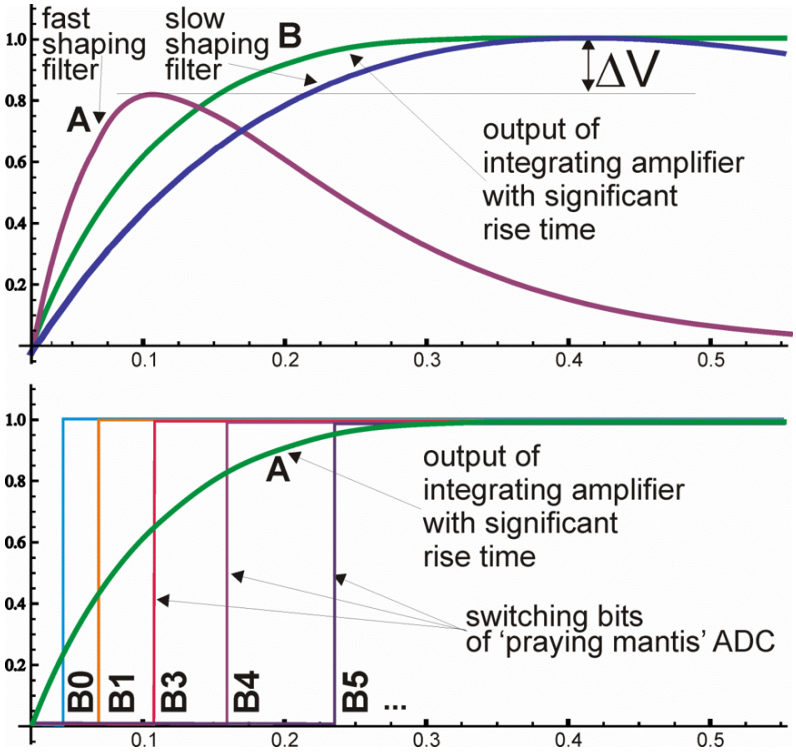



Figure 3.8: Trade-off of fast and slow shaping (a). Synchronous ADC concept (b).

Generally, the early digitization of the signal in the processing chain maintains good SNR, so the fast preamplifier, followed by a fast shaper, must be followed by the discriminator. In order to reach an accurate time allocation of hits, this requires the discriminator to detect the smallest signal within the BXClk period. In a system with continuous time shaping, this is difficult to fulfill. A slow rise time of the preamplifier and the response time of the discriminator lead to a time walk. Therefore hits just above threshold, can improperly be assigned to the subsequent BXClk period. It is worth noting that small signals could be due to either really small charge generated by the sensor or may result from charge sharing among the pixels [53]. Finally, the signal in continuous time processing needs to be compensated for baseline drifts

either due to charge pile-up or DC coupling of consecutive processing stages.

The FEI family developed for ATLAS pixels [54] is an example of a front-end concept which utilizes continuous time processing but, at the same time, eliminates the shaping amplifier. This is mainly dictated by saving of power consumption and area. The FEI pixel is based on a preamplifier with constant current discharge and an analog to digital conversion achieved with time-over-threshold (ToT) measurement. Such a ToT provides an analogue information of every hit and is measured in FEI in units of the bunch crossing clock (25 ns). It takes up to 16 BXClk cycles for full conversion for large signals which are too slow. Additional investigations of the FEI3 readout architecture indicate that the front-end is unable to meet the HL-LHC hit rate [55]. Because of the slower architecture requiring further processing, FEI also employs time walk correction by exploiting the correlation between small amplitude and large time walk. In fact, every hit must be associated with the correct bunch crossing. This means that the discriminator must not fire later than 25 ns after the charge has been deposited in the sensor. This requirement is difficult to fulfill when hits have small amplitudes, just above the threshold. The rise time of the amplifier and the response time of the discriminator then lead to a "time walk" so that hits just above threshold may be detected too late. The correlation of small amplitude and large time walk is exploited in a digital time walk correction in FEI: the leading edge time stamp is corrected by one if the ToT amplitude is below a programmable cut value. The successor ASIC, FEI4, improves upon the speed requirement, but has a large pixel size of 50 $\mu$m x 250 $\mu$m in a 130 nm process [56] and higher power consumption.

The goal of the novel design proposed here is to efficiently use the synchronous environment of the LHC to detect an incoming particle and determining the amplitude of associated signal within one BXClk period of 25 ns. The proposed synchronous ADC approach eliminates the need of a classical shaper. Furthermore it allows analog-to-digital conversion to begin as soon as the charge is generated and continues until signal reaches its maximum value or time for conversion runs out, as shown in Figure 3.8(b). In this way, the analog-to-digital conversion is performed with no dead time. The concept relies upon a simple charge integrator AC-coupled to a synchronous discriminator. The time walk issue never arises as the discriminator resets at the end of the

BXClk period. Although the classical shaping filter is absent, noise filtering is achieved with correlated double sampling (CDS) technique [57]. For definition, CDS is a method to measure electrical values such as voltages or currents that allows removing an undesired offset. It is used often when measuring sensor outputs. The output of the sensor is measured twice: once in a known condition and once in an unknown condition. The value measured from the known condition is then subtracted from the unknown condition to generate a value with a known relation to the physical quantity being measured. The low-power correlated double sampling reduces the low frequency noise components. CDS also automatically removes offsets and increases pile up immunity.

Furthermore, the synchronous front-end uses a simple charge integration which does not rely on precisely designed absolute parameters, and is followed by digitization with self-correcting features. The proposed digitizing at an early stage in the processing chain, imports the industrial trend to high-energy physics. In summary, the designed front-end, called IFCP65, incorporates the following features:

- No continuous time filtering;
- Insensitivity to ballistic deficit;
- Insensitivity to absolute design parameters (e.g. shaping time);
- Insensitivity to event pileups;
- Signal filtering based on correlated double sampling;
- Increased noise immunity due to digital conversion immediately after preamplifier;
- Data conversion within 1 BXClk cycle (25 ns);
- Leakage current compensation per pixel;
- Auto-zero comparators without the need for offset trimming DACs;
- 3-bit flash ADC;
- Low power consumption;
- Shift register for digital readout.

### 3.4.2 Analog Front-End implementation

*IFCP65* (INFN Fermi CMS Pixel) is a collaboration between University of Bergamo (IT), INFN sezione di Pavia (IT) and the Engineering Department of the Particle Physics Division at the Fermi National Accelerator Laboratory (FNAL), Batavia (USA). The readout channel inherits the general architecture adopted in the design of the so-called Fermi CMS Pixel Test Chip (FCP130), designed by Fermilab in 130 nm CMOS technology. It implements performance improvements mainly related to the most innovative block of analog chain, namely the comparator. A prototype chip including this analog processor has been submitted in June 2016.

The analog front-end includes a low noise, fast charge sensitive preamplifier with detector leakage current compensation, a feedback capacitor, and an active transistor feedback resistor. It is AC-coupled to four synchronous comparators forming a flash-type ADC. Every comparator in the ADC is based on a compact, single ended design featuring very good performances in terms of channel-to-channel threshold dispersion. The simplified block diagram of IFCP65 analog processor is shown in Figure 3.9.

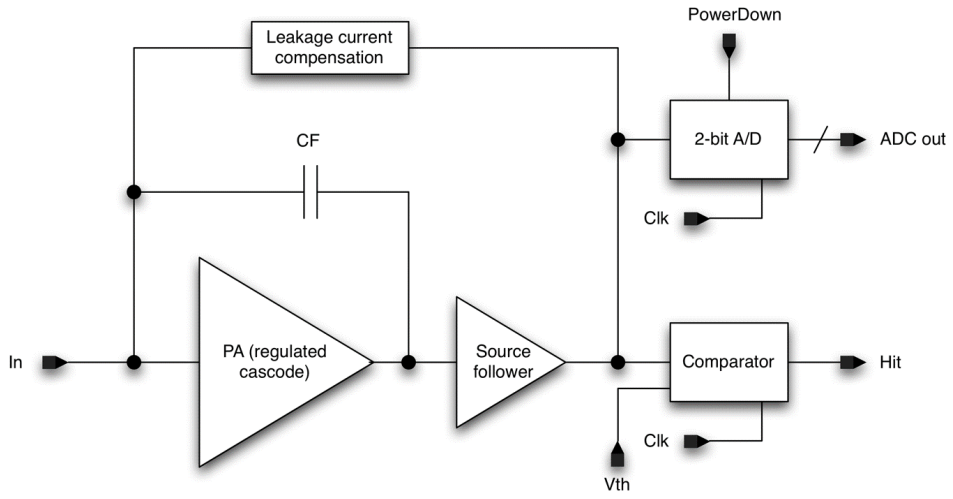



Figure 3.9: Block diagram of the analog front-end containing a preamplifier with leakage current compensation, an AC-coupled synchronous comparator and 3-bit flash ADC.

The first stage of the processing chain is a charge sensitive amplifier (CSA),

implementing a regulated cascode scheme in its forward gain stage [59]. It also includes a source follower stage able to properly drive the CSA load. The charge amplifier features a feedback leakage compensation network. Such a circuit compensates the induced increase in the detector leakage current, mainly due to the expected large radiation levels. The choice of a single amplification stage in the front-end channel has been simply dictated by power consumption constraints. The signal at the CSA output is fed to a compact and single-ended threshold discriminator that features auto-zeroing and provides a pure hit or no-hit (binary) information at the channel output. Compared to a typical implementation of the discriminator, where voltage comparison takes place exploiting a differential MOS pair with a mirrored load, this implementation is ideally insensitive to device threshold voltage mismatch. For this reason, the comparator, run with a 40 MHz clock, does not require any threshold fine-tuning system. A flash ADC, whose architecture is based on the same circuit used for the hit comparator, can be exploited for digital conversion immediately after the charge sensitive amplifier. The comparator, connected to threshold voltage $V_{th}$, generates the Hit signal, which is used to indicate valid data in the pixel and hence triggers readout of the pixel. Comparators connected to thresholds $V_{th}$1-3 generate ADC output as shown in Figure 3.9. All thresholds $V_{th}$0-3 are externally controlled. In this first version of IFCP65 analog readout, no in-pixel charge injection circuit is incorporated in IFCP65. The injection is performed with 15 fF capacitance connected to the preamplifier input.

## 3.5 Analog Front-End design and performances

As previously described, the analog front-end is based on two key components: a charge integrating preamplifier and an auto-zeroing comparator. The preamplifier consists of a core amplifier with leakage current compensation, a feedback capacitor, and an active transistor feedback resistor. The unidirectional comparator consists of two stages that are AC-coupled to each other. The first stage is an amplifier which allows setting of the threshold and the second stage adds further gain with positive regeneration. What follows in this subsection is the transistor level design detail of the preamplifier along with the innovative auto-zero comparator and verification simulations.

### 3.5.1 Charge sensitive amplifier

A simplified diagram of the preamplifier section is shown in Figure 3.10, with particular emphasis on its feedback network. The goal of this circuit is to integrate a detector charge signal and convert it to a voltage step that can be digitized.

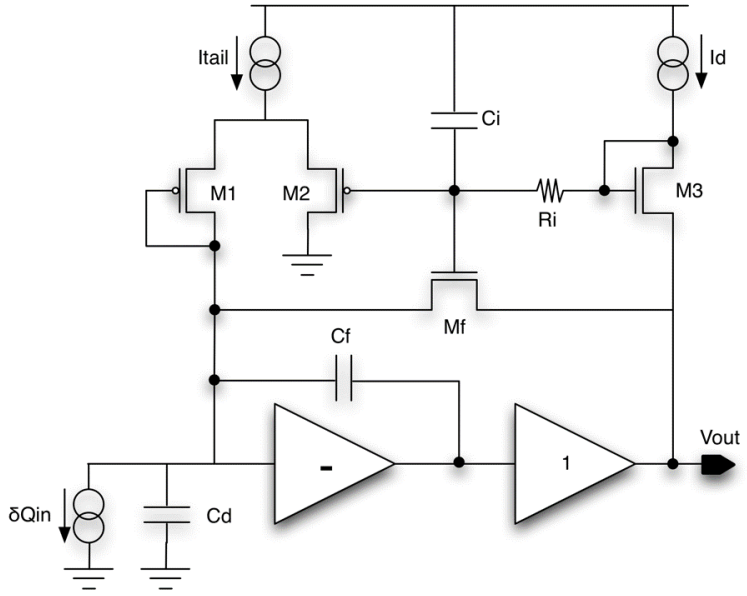



Figure 3.10: Simplify schematic of the IFCP65 charge sensitive amplifier, featuring a leakage current compensation network.

The capacitance $C_d$ emulates the detector capacitance, shunting the CSA input. The open loop gain of the preamp should be large so that the transfer gain is dependent only on the value of the capacitance feedback $C_f$. As mentioned in the previous section, the CSA is based on a regulated cascode gain stage, whose DC open loop gain is equal to 52 dB, with a cut-off frequency close to 3.6 MHz (see plot 3.11). For the regulated cascode, 2 $\mu$A are allocated for the input branch, 2 $\mu$A for the source follower and 0.1 $\mu$A for the remaining branch. A regulated cascode is a simple cascode circuit with the Gate voltage of the cascode transistor being controlled by a feedback amplifier. In comparison to the standard cascode circuit, the minimum output voltage is lower by about 30 to 60%, while the output conductance and the Miller capacitance are lower by about 100 times. Moreover the output impedance is even higher than that

of the simple cascode. With adopting a regulated cascode, the Drain-Source voltage of Mn1 is regulated to a fixed value.

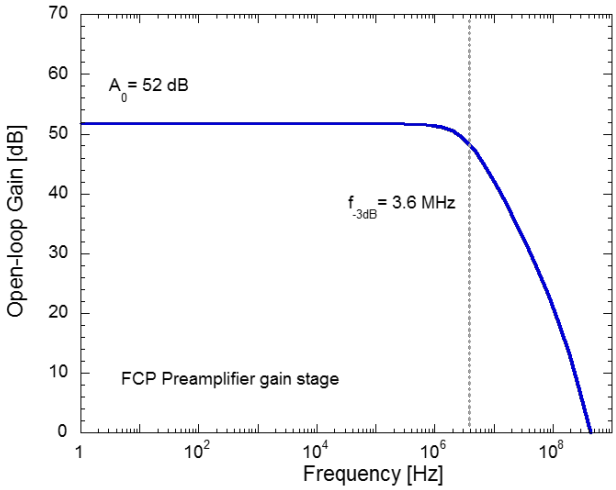



Figure 3.11: DC open loop gain.

In addition, the output should be fast (a few ns rise time) and capable of driving four subsequent ADC comparators in parallel. The required reset rate depends on the average hit rate, since it must be fast enough to avoid integrator saturation. Note that it must not be so fast as to distort a detector signal. Incorporated with the continuous reset function is a DC detector leakage current cancellation circuit. Figure 3.12 represents the transistor level schematic of this preamplifier. Since the input collects only electrons, the output always goes positive with a signal, and the design is optimized for unipolar operation.

The NMOS input gain transistor Mn1 feeds a regulated cascode (Mn2 - Mn3) in order to achieve high open loop gain. The closed loop transfer gain is therefore determined only by $C_f$. The source follower Msf2 is also an NMOS device, which can easily pull up the output and drive all the comparators, even with relatively low DC bias current. The NMOS transistor Mf is the active continuous feedback element. It acts as a $1/g_m$ resistor for small signals, where $g_m$ is the transconductance of $M_f$, whereas it behaves as a constant current source for large signals. The action of differential pair M1 and M2 is to set same DC voltage at the gate and drain of $M_f$. For large signals that fully turn off $M_f$, the constant current $Id$ is diverted to the input to discharge $C_f$ until the $M_f$ bias is restored. Before signal arrival, and neglecting the detector leakage, a

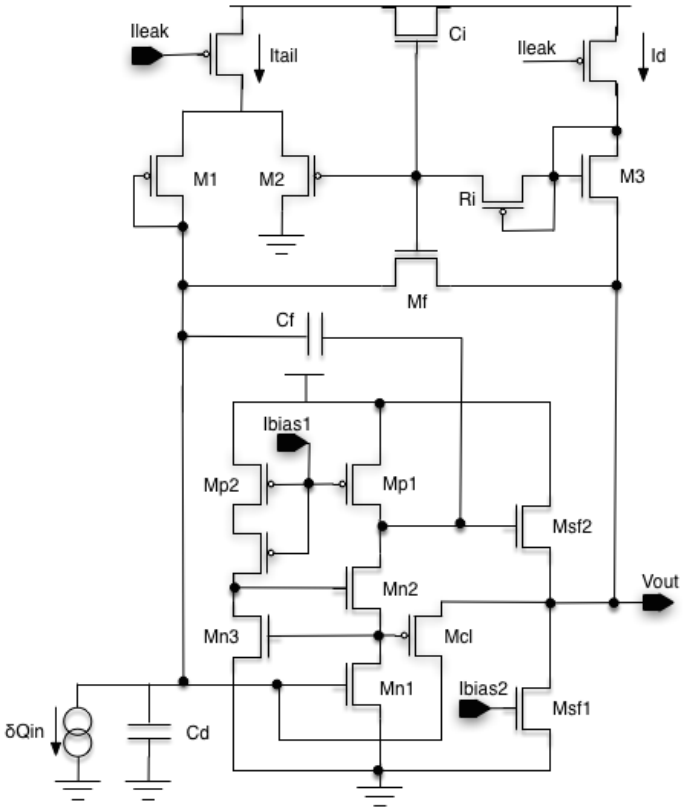



Figure 3.12: Transistor level preamplifier design showing a regulated cascode core amplifier.

current equal to $kI_d$ flows in $M_1$ and $M_f$ transistors. The so-called $k$ represents the current mirror factor between $M_f$ and $M_3$. Upon large-signal arrival, the output voltage $V_{out}$ increases, turning off the active feedback transistor $M_f$. In this way, and thanks to the low-pass filter action occurring in the feedback network, the current flowing in $M_1$ discharges the feedback capacitance $C_f$. The low-pass filter is implemented by means of resistor $R_i$ and capacitor $C_i$, thus ensuring low frequency operation of the leakage compensation circuit. The transistor $M_1$ also provides a DC path for the detector leakage current. The same differential pair M1 and M2 also acts to supply both Id and Ileak (the detector DC leakage current), by forcing the M2 gate and the preamplifier input to be at the same DC voltage. Therefore, the differential pair bias current $I_{tail}$ must be large enough to supply both of these currents to the input. In fact, for proper operation of the feedback network, the value of $I_{tail}$ must be

greater than the sum of the expected detector leakage current and the current $I_d$, multiplied by the mirror factor $k$. A low pass filter ensures that the circuit responds only to DC shifts and not to transient signals. In this configuration, the DC output voltage is lower than the input voltage by the Gate-Source voltage (VGS) of Mf, which helps to maximize the dynamic range. Table 3.3 enlists the key design and performance parameters of the preamplifier.

| ***Parameters*** | ***Values*** |
|---|---|
| Input transistor dimensions | W/L = 4$\mu$m/200nm; |
| Feedback capacitor (Cfb) | 12.1 fF |
| Feedback resistor (Mf) | W/L = 300nm/1$\mu$m; |
| Current in core amplifier | 2$\mu$A |
| Current in source follower | 2$\mu$A |
| Total power consumption | 4.8 $\mu$W |
| Preamplifier rise time (1000 $e_-$ charge) | 3 ns |
| Open loop gain | 53 dB |
| Cut-off frequency | 2.3 MHz |

Table 3.3: Key design and performance parameters of the preamplifier.

With a total current flowing in the amplifier equal to 4 $\mu$A, the CSA is responsible for half of the overall power consumption in the analog front-end featuring a 2-bit flash ADC. Figure 3.13 shows the simulated charge sensitive amplifier response to an input charge equal to 1000 electrons. The simulation has been performed for different values of the detector leakage current, ranging from 0 to 14 nA. A total of 15 curves are almost overlapped in the plot, pointing out that the compensation circuit works fine for leakage currents up to 14 nA. On the other hand, a slight decrease in charge sensitivity is detected for currents greater than 14 nA. The detector leakage does not affect the rise time of the CSA output response, which is close to 3 ns for a 1000 electrons input signal. The charge sensitivity of the CSA is defined as the slope of the straight lines of Figure 3.14. It shows the four corners simulation of the amplifier peak amplitude as a function of the injected charge. The charge sensitivity ranges from 10.9 mV/ke in the Slow-Slow (SS) corner to 14.7 mV/ke in the Fast-Fast (FF) corner, with a typical (TT) value equal to 12.6 mV/ke.

The non-negligible changes in the charge sensitivity have to mainly be ascribed to the contribution of the metal-insulator-metal (MIM) capacitance

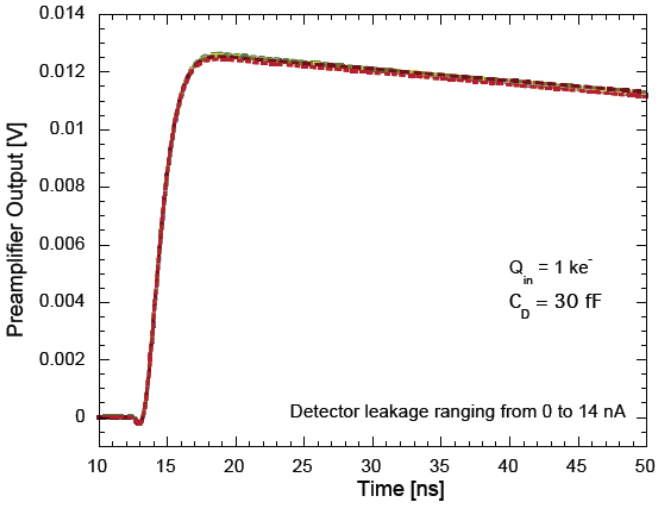


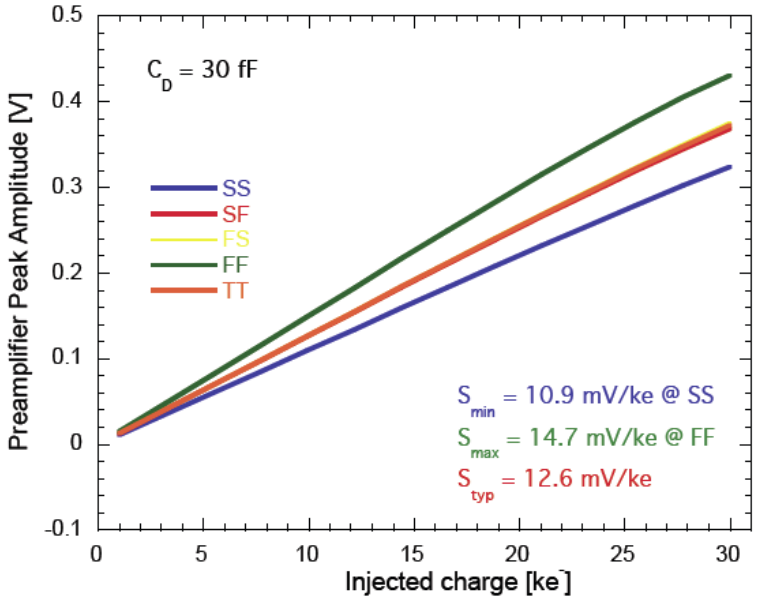

Figure 3.13: CSA response to an input charge equal to 1000 electrons, for different values of the detector leakage current, ranging from 0 to 14 nA.

$C_f$, used as the feedback element in the CSA. Such a capacitance has high density and lower parasitic, compared to the other typical type of capacitance. The circuit also shows a good linearity: in fact, in the TT corner simulation an integral non linearity (INL) equal to 1.6% has been obtained (see Figure 3.15).

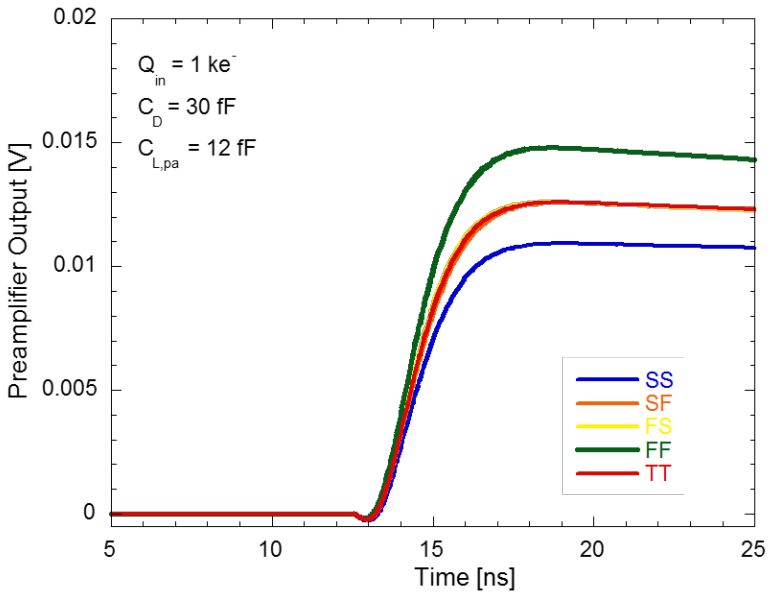
In addition, Figure 3.16(a) shows the equivalent noise charge (ENC) as a function of the detector capacitance $C_d$. As expected, the ENC increases by increasing the detector capacitance, reaching a maximum value close to 110 electrons for the maximum value of $C_d$, namely 100 fF. The equivalent noise charge increases with the detector leakage current as well (see Figure 3.16(b)). As an example, the ENC evaluated at $C_d$ equal to 30 fF, in the presence of a detector leakage equal to 5 nA, is close to 80 electrons. Such a value has to be compared with an ENC equal to 75 electrons obtained in the same condition, but without the detector leakage. The increase of the equivalent noise charge with the detector leakage current has to be ascribed to the increase of the parallel noise contribution of the CSA feedback network.

### 3.5.2 Small signal analysis

Figure 3.17 shows the small-signal equivalent circuit of the preamplifier, where the regulated cascode gain stage is modeled as a voltage DC generator: -A$V_{in}$.




(a)




(b)

Figure 3.14: Four corners simulation of the CSA peak amplitude as a function of the input charge (a) and of CSA response to an input charge equal to 1000 electrons.

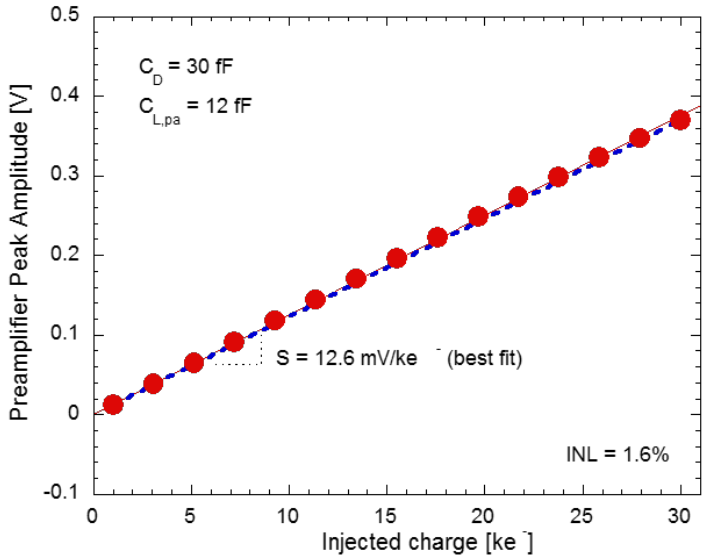



Figure 3.15: CSA peak amplitude as a function of the input charge in TT corner.

As far as the low frequency small signal response is concerned, it can be shown that the transfer function, in terms of Laplace formalism, is as follows:

$$\frac{Vout(s)}{Iin(s)} = \frac{(1 + sR_iC_i)}{\frac{gm_1 gm_2}{gm_1+gm_2} + s(R_iC_igm_f + C_f) + s^2R_iC_iC_f} \tag{3.2}$$

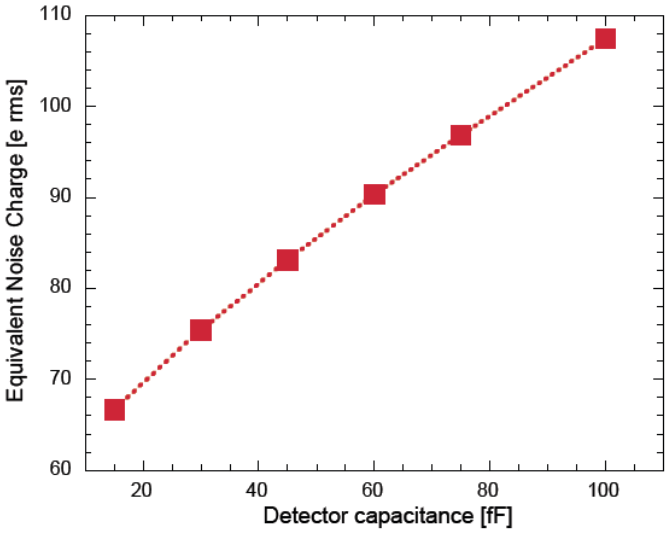
where $gm_1$, $gm_2$, $gm_f$ are respectively the transconductance of Mosfets $M_1$, $M_2$, $M_f$ related to the circuit 3.12. Note that the NMOS $M_3$ in circuit 3.12 operates as a small-signal resistor (whose value is $1/gm_3$). In the small-signal model since it is placed with the resistance $R_i$ it can be considered as negligible. For such a small-signal analysis, the transfer function that defines the response of the system to an input charge signal, is obtained by combining the following current evaluations calculated in 3 circuit nodes:

$$(V_{in} - V_a)gm_1 = (V_a - V_b)gm_2 \tag{3.3}$$

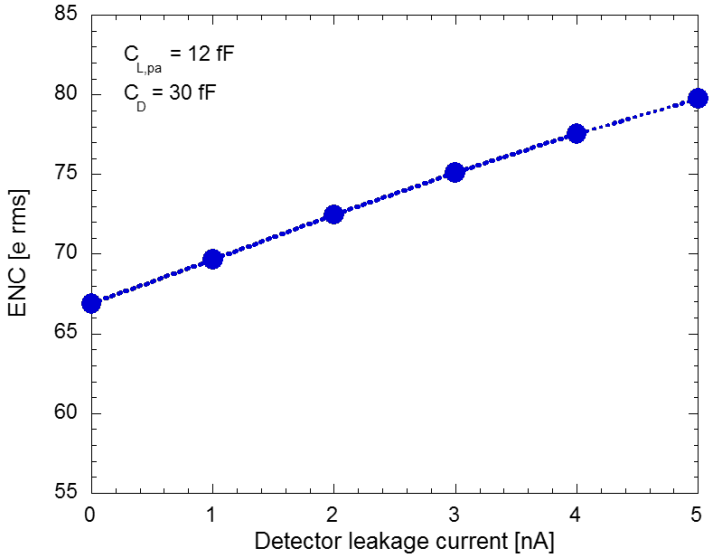
$$V_b = \frac{1}{1 + sR_iC_i}V_{out} \tag{3.4}$$

$$I_{in} + (V_{in} - V_a)gm_1 + (V_{in} - V_{out})sC_f + gm_f(V_b - V_{out}) = 0 \tag{3.5}$$

Furthermore, it is important to calculate the inverse transform in time domain. By imposing that the resistance $R_i$ tends to infinity, eq. 3.2 can be expressed




(a)




(b)

Figure 3.16: Equivalent noise charge as a function of the detector capacitance $C_D$ (a) and as a function of leakage current (b).

by:

$$\frac{Vout(s)}{Iin(s)} = \frac{1}{gm_f + sC_f} \tag{3.6}$$

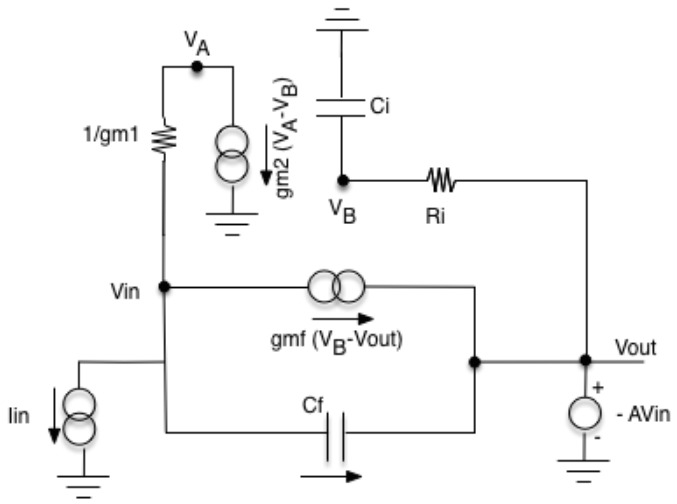



Figure 3.17: Small-signal equivalent circuit of the charge sensitive preamplifier.

In particular, the response of the stage to a delta at its input in time domain is equal to:

$$Vout(t) = \frac{Q_{in}}{C_f} e^{-\frac{gm_f}{C_f}t} \tag{3.7}$$

From this expression, is it possible to calculate any characteristic of the output: from the gain to the peaking time. The decay time has been set to the ratio of $gm_f$ and $C_f$. As far as the gain, defined as the ratio of the output peak to the input step size, is equal to $Q_{in}/C_f$.

### 3.5.3 Comparator

As far as the comparator, there are several important criteria for the design that are critical for proper functionality of the IFCP65 circuit.

First of all, the preamplifier and comparator system must be insensitive to all DC offsets so that threshold values do not require trimming in each pixel. The comparator must be insensitive to charge pileup at the preamplifier output, and must be looking only at the change of that output in every bunch crossing. Therefore, a configuration with discrete reset and AC-coupling between stages is chosen, which performs CDS and comparator auto-zeroing, as previously described. Second, since, with this configuration, the threshold must somehow be re-established in all comparators every BXClk period, a method of setting comparator thresholds that minimizes current transients is required. Third,

the comparator current consumption should remain as constant as possible at all times to avoid large ASIC-wide current transients. Fourth, the comparator must have relatively fast response, compared to the 25 ns bunch crossing time while consuming little power (about 1.2 $\mu$W per comparator). Figure 3.18

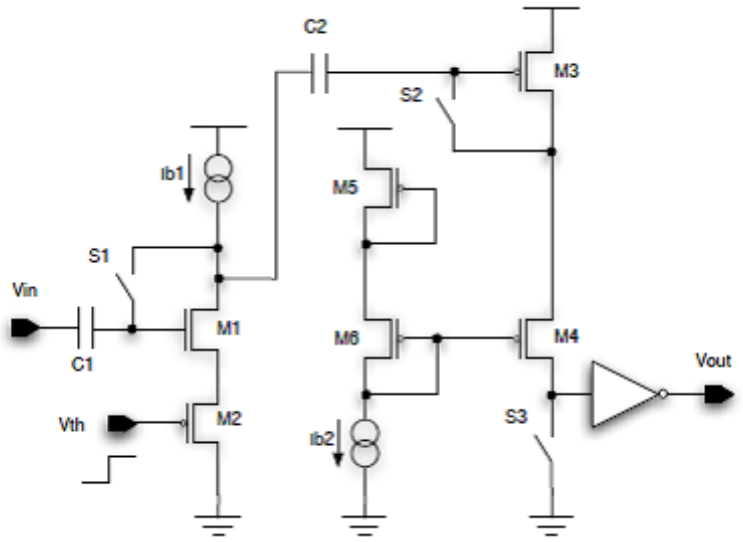



Figure 3.18: Simplify schematic of the IFCP65 comparator, based on two stages.

is a simplified diagram that shows comparator design configuration based on two stages. Both stages are single-ended for simplicity and with low power consumption. Such a circuit is used both for the hit comparator and for the set of the comparators making up the flash ADC.

The first stage of the comparator is AC-coupled to the preamplifier output, and is able to provide a binary information at its output. This configuration implements the CDS function on the preamplifier output. The comparator operates in two different phases, controlled by a clock signal driving the comparator switches. The time for the first comparator stage to fully reset is approximately half of the bunch crossing time (12.5 ns). So, for convenience, the first half of the bunch crossing is designated for reset and the remaining 12.5 ns for integration and comparison. During the first phase, called for convenience "reset phase", a proper bias is provided to the two discriminator stages. The timing of the preamplifier signal is therefore constrained to the beginning of the second half of the bunch crossing. The second stage of the

comparator amplifies the first stage output and converts it to a digital signal. It is AC-coupled to the first stage and reset at the same time, thereby removing the offset between the two stages. Figure 3.19 represents the simulation timing scheme of the concept just described, considering 40 MHz as reset signal. Typical implementations of the discriminator are based on a comparison of the

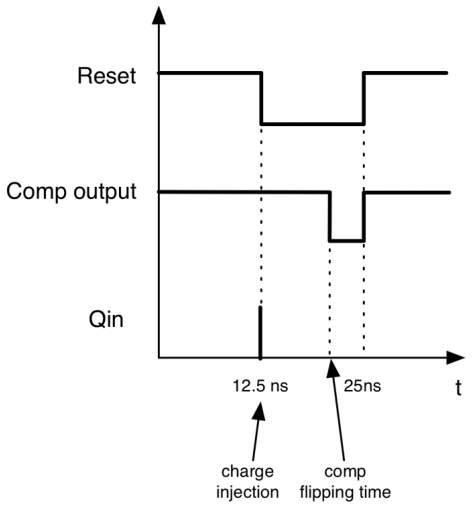



Figure 3.19: Simulation timing scheme. Charge injection takes place as soon as the reset is released.

CSA output signal with a DC threshold voltage. Normally both the signals are provided at the inputs of a differential CMOS pair with a mirrored load. A novel method of setting the comparator threshold is employed in the first stage. The novel approach drives the source of M1 with a small threshold source follower M2. In fact, in the IFCP65 comparator, the threshold is provided at the discriminator input as a step signal, called $V_{th}$, processed and compared with the one coming from the CSA output. The positive-going threshold step is created at the gate of the follower when the reset is released by switching from ground to a DC threshold voltage level $V_{th}$, which is routed to all pixels. Thus the threshold step drives only a very small capacitance in each pixel. During the "reset" phase, the so-called $S_1$, $S_2$ and $S_3$ switches are closed. During the "comparison" phase, an active comparison takes place by injecting both the CSA and the threshold signals at the comparator inputs. All the switches are open during this phase. A more detailed transistor level schematic of the first stage is shown in Figure 3.20. Transistor M1 acts as a common source amplifier

for the signal coming from the CSA, whereas it behaves as a common gate stage for the threshold signal provided to its source by means of the source follower transistor M2. As long as the threshold rise time is minimized with respect to the CSA output signal rise time, the first stage provide a negative voltage step at the drain of M1 when the CSA output signal is greater than the threshold signal. However, the drain voltage does not go to the power rail, but engages clamp transistor Mc, which keeps the current consumption constant and also limits the voltage swing at node X, improving the speed of the first stage. M1 and M2 are low threshold (Vth) transistors in order to preserve as much dynamic range as possible. The voltage step at the drain of

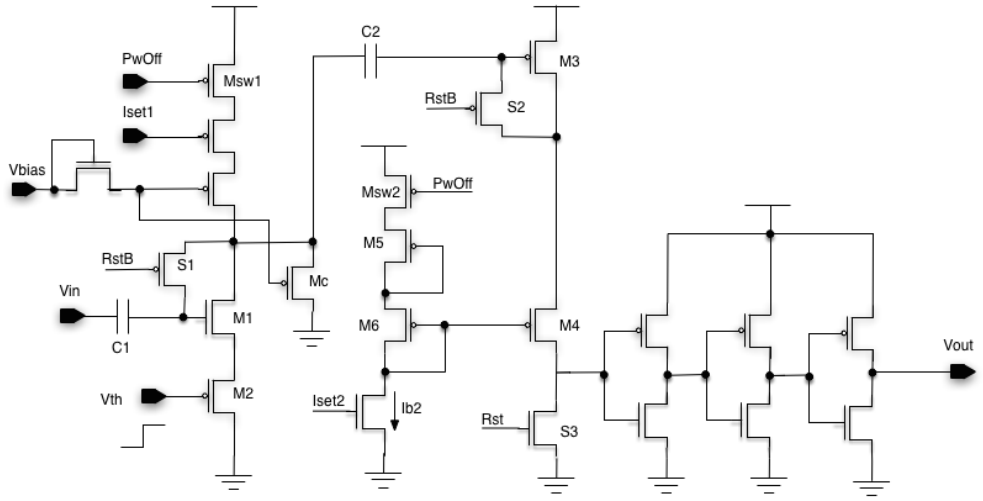



Figure 3.20: Transistor level schematic of the IFCP65 comparator.

M1 is further amplified by the second stage of the comparator, which consist of a cascode gain stage followed by a chain of inverters. Notice that during the "comparison" phase, the switch $S_3$ is open and the leakage current lowing through M3 and M4 charges the parasitic capacitance connected to the inverter input, increasing the voltage at the drain of M4. Fast comparator operation is difficult to achieve in a low power environment. Therefore, the second stage is operated on the verge of "flipping". For small thresholds, M3 does not fully shut off, and even with no signal this small current will eventually turn on the cascode transistor M4, causing the comparator to flip. However, this would only occur after the 12.5 ns period of interest so is not seen. The comparator

switches within the 12.5 ns period when the signal level is equal to or greater than the threshold. Since half of the cycle is spent for comparator reset, and the preamplifier output should move only after reset is complete, this allows 12.5 ns for preamplifier settling and the comparison operation. So it is crucial to carefully size the dimension of the transistors in order to avoid undesirable comparator hits in a given bunch period (i.e. without a charge signal injected into the channel input). Table 3.4 enlists the key design and performance parameters of the comparator. Therefore, it is important that the comparator be as fast as possible. In summary, the first stage performs comparison of the input to a threshold, and the second stage provides gain for fast operation.

| ***Parameters*** | ***Values*** |
|---|---|
| Input transistor dimensions | W/L = 1.4$\mu$m/140nm; |
| Coupling capacitor to CSA output (C1) | 12.14 fF |
| Coupling capacitor between 1 and 2 stage (C2) | 12.14 fF |
| Current in 1 stage | 800 nA |
| Current in 2 stage | 200 nA |
| Power consumption | 1.2 $\mu$W (per comparator) |

Table 3.4: Key design and performance parameters of the comparator.

A peculiar feature of the IFCP65 comparator is its capability to process two consecutive signals coming from the charge sensitive amplifier. As an example, Figure 3.21 shows the simulated comparator output response to two consecutive charge signals injected into the readout channel. In this simulation the comparator clock is set to 40 MHz, and the threshold to 800 electrons. In the first bucket, lasting 25 ns, the comparator responds to a charge signal equal to 40000 electrons injected at the CSA input, whereas in the second one it responds to a charge equal to 800 electrons. This points out that the IFCP65 readout channel is able to successfully process very large signals followed by signals close to the threshold.

A feature of the comparator worth investigating is its response time. The response time is defined here as the difference between the time at which charge injection at the CSA input takes place and the time at which the comparator gets flipped. Figure 3.22 shows the comparator response time as a function

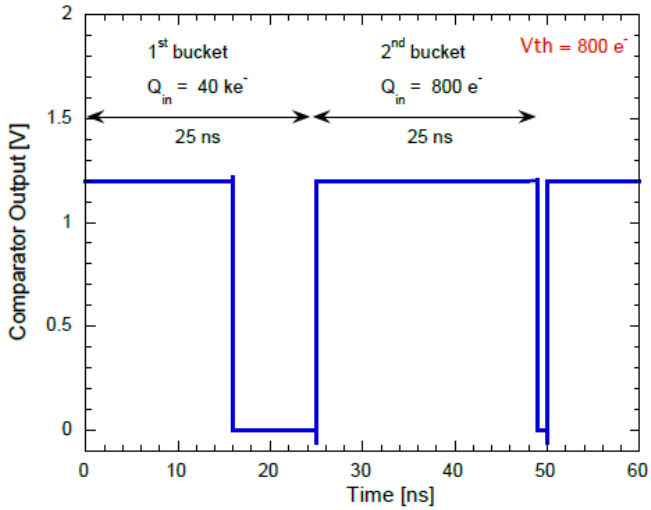



Figure 3.21: Comparator output response to two consecutive event, with a threshold set to 800 electrons.

of the charge injected into the readout channel, with a threshold set to 800 electrons.

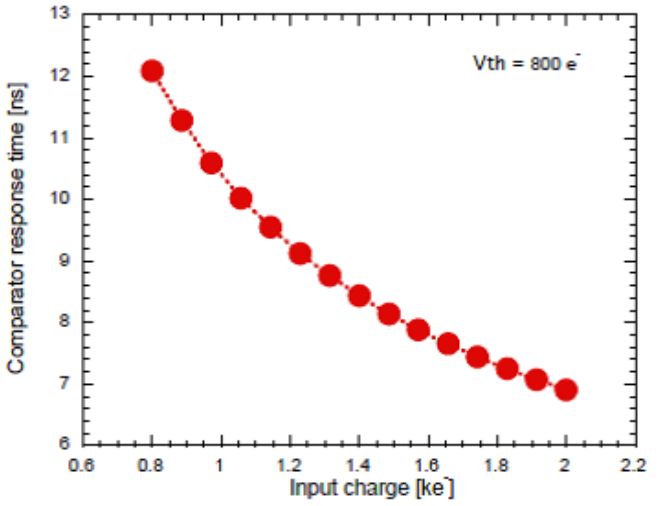



Figure 3.22: Comparator response time as a function of the injected charge. The threshold is equal to 800 electrons.

The response time is equal to 12 ns for a signal close to the threshold, and it decreases down to 7 ns when the input charge signal is equal to 2000 electrons. The average current consumption of the comparator is 1 $\mu$A, including both

static and dynamic contributions. A 2-bit flash ADC based on the proposed comparator thus consumes 3 $\mu$A whereas 8 $\mu$A are needed for the whole channel. For further decreasing power consumption, in order to obtain a front-end channel with specifications in accordance with RD53A (previously enlisted), a low-power mode is introduced as follows. In ADC schematic, PMOS Msw1 and Msw2 works as switches able to power off respectively the first and second stage of the comparators. In this case, only a binary information concerning the presence of hit/no-hit, is provided at the channel output, with a total power consumption equal to 5 $\mu$A.

An optimization process has been carried out during the design phase in order to properly size some critical transistors included in the comparator. Such a process aimed at minimizing the threshold dispersion of the channel, equal to 35 electrons from circuit simulations after optimization. Such a low value for the threshold dispersion allows the readout channel to operate without needing any pixel-level trimming. Figure 3.23 represents the resulting s-curve of Monte Carlo analysis for threshold dispersion. Such a simulation has been achieved considering 800 electrons threshold. Note that an ideal preamplifier is used for this threshold dispersion analysis, as signal input for the comparator and without including the whole ADC. Moreover, such a Monte Carlo result was obtained considering a correlation coefficient between the two MOSFET that perform the current mirror in the second stage.

The simulated comparator turns out to be almost insensitive to corners. As an example, Figure 3.24 shows the amplitude of the threshold voltage step to be provided at the comparator input in order to obtain an equivalent 800 electrons threshold, for the different simulation corners. A value of 11.4 mV has been obtained for the typical corner, with a minimum equal to 11.1 mV in the SS corner and a maximum of 12.5 mV in the FF corner.

### 3.5.4 Simulation performance metrics

The transient simulation in Figure 3.25 shows the response of the analog front-end when a charge of 30000 e- is injected at 12.5 ns, synchronously with the falling edge of the BXClk, just after the comparator has been reset. It shows the Hit comparator, and the three comparators that perform the ADC, firing sequentially as the output of the preamplifier rises. For each ADC comparator was assigned a different threshold.

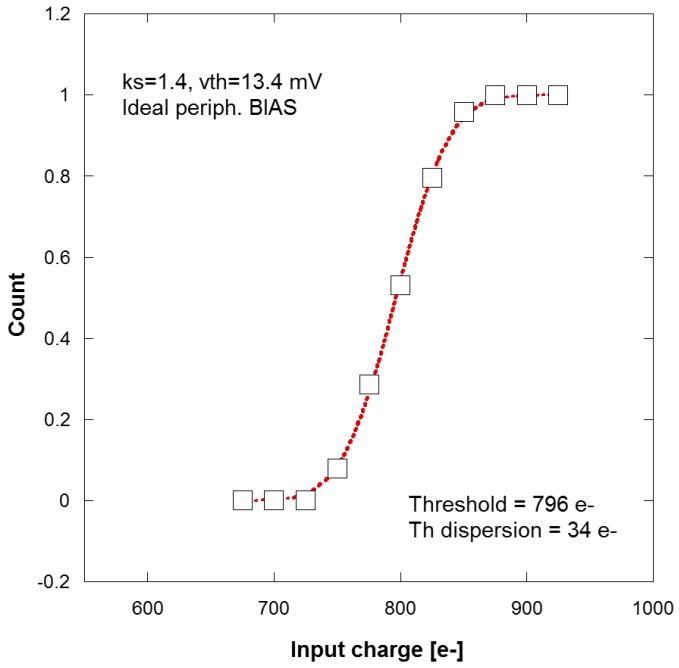



Figure 3.23: Threshold dispersion analysis.

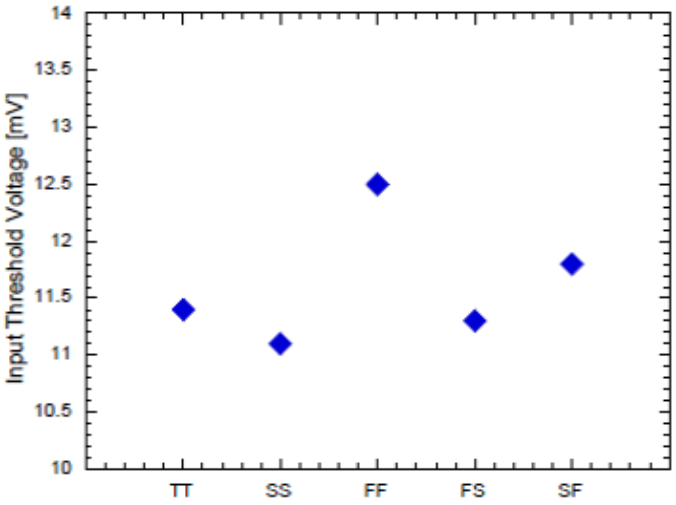



Figure 3.24: Amplitude of the threshold voltage step to be provided at the comparator input equivalent to a 800 electrons threshold, for different simulation corners.

Any charge arriving at the sensor, while the comparator is being reset, is not processed.

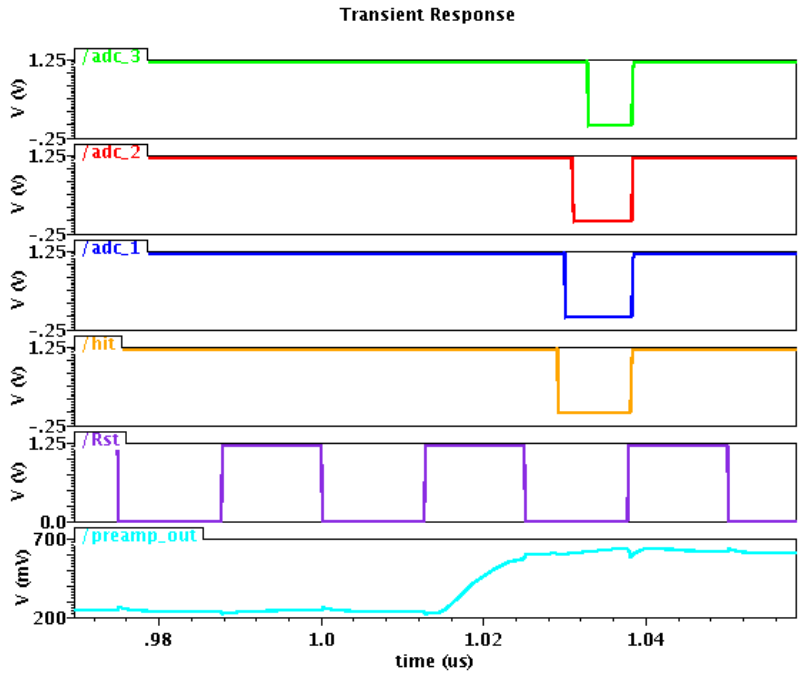



Figure 3.25: Simulation of the analog front-end with charge injected at 12.5 ns.

## 3.6 IFCP65 layout and post-layout simulations

A prototype chip including the IFCP65 readout channel has been submitted in June 2016. The following paragraph describes the layout techniques for circuit design. The front-end chip has been fabricated in the 65 nm low-power CMOS technology by TSMC (www.tsmc.com). Specifications of the IFCP65 ASIC are summarized in Table 3.5. Furthermore, a set of post-layout simulations, compared to pre-layout, are provided here.

### 3.6.1 Pixel layout

According to RD53A requirements, the pixel is 50 $\mu$m x 50 $\mu$m in size, where an area equal to 35 $\mu$m x 35 $\mu$m is allocated for analog part, whereas the remaining area is designated for the digital part. In particular, the area allocated for the digital components of the pixel creates a strip that flows around the square foreseen for the analog area. Such a pixel configuration permits to build, for each pixel that compose the matrix, a so-called "analog island", surrounded by "digital sea". Such design methodology is a new approach used in High

| *Parameter* | *Value* |
|---|---|
| Fabrication process | TSMC 65 nm CMOS |
| Submission | June 2016 |
| ASIC size | 2 mm x 2 mm |
| Number of pixels | 16 x 16 |
| Pixel size | 50 $\mu$m x 50 $\mu$m |
| Analog power consumption | 9.6 $\mu$W |
| ADC resolution | 2-bit |
| ADC conversion time | 1 BXClk cycle (25 ns) |
| Trimming DACs | No |

Table 3.5: Specification of IFCP65 ASIC.

Energy Physics community, which optimize the use of silicon area. In particular, each pixel region is composed by a 4x4 analog pixel cell that share the digital function. For each two columns of pixels, there is a column base block at the end of the column that provides the biasing, reset signal and voltage reference. A Bump-bond pad with an area equal to 16 $\mu$m x 16 $\mu$m is also allocated for interconnection with the sensor.

Figure 3.26 depicts the block diagram of the pixel, which includes the preamplifier (7 $\mu$m x 16 $\mu$m) with MIM feedback capacitance, the Hit comparator (7 $\mu$m x 12 $\mu$m), the 2-bit flash ADC, a Source-follower, digital readout buffers and injection capacitance. In more detail, after the preamplifier, a source-follower that operates as a voltage buffer, has been placed. This stage is used to drive low-impedance load with negligible loss of the signal level. Moreover, the role of injection capacitance Cinj equal to 14.9 fF is to emulate the detector capacitance. The overall layout of the pixel is clearly visible in Figure 3.27. All the devices are placed in the global P-substrate. The preamplifier block is surrounded by NWELL Guard-ring path. In some case in CMOS, the N and P structure used in each process can create a parasitic path between the supply and the ground. By using the Guard-ring, it can reduce these parasitic effects (NPN-PNP parasitic transistors created). As far as the pixel biasing is concerned, the preamplifier and the 4 comparators are biased with vertical power lines on Metal 6 (M6) (see layout 3.28(a)) whereas the power supply and ground are provided with layer 9 (M9) (see layout 3.28(b)).

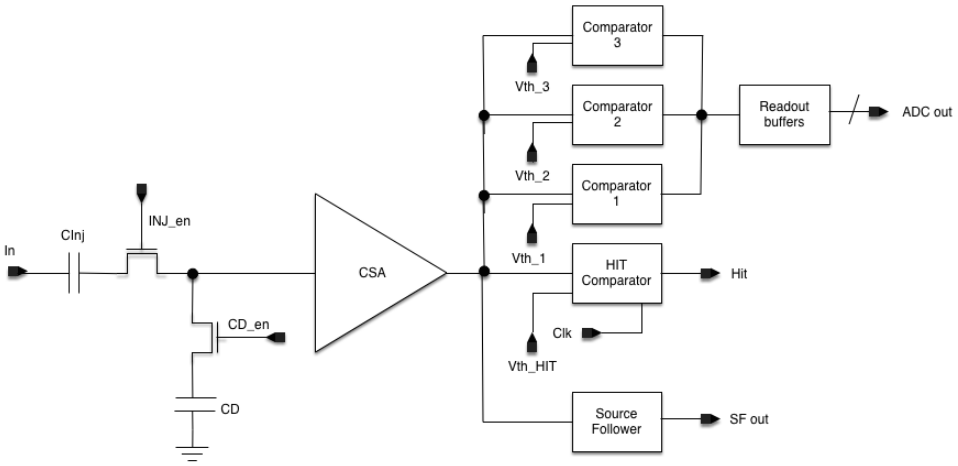



Figure 3.26: Block diagram of the whole pixel.

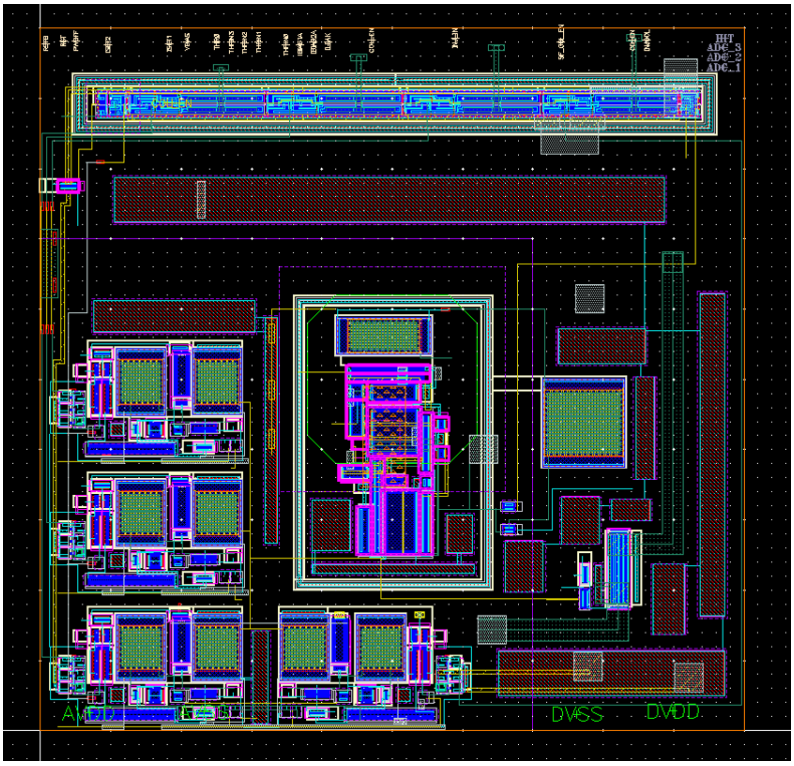
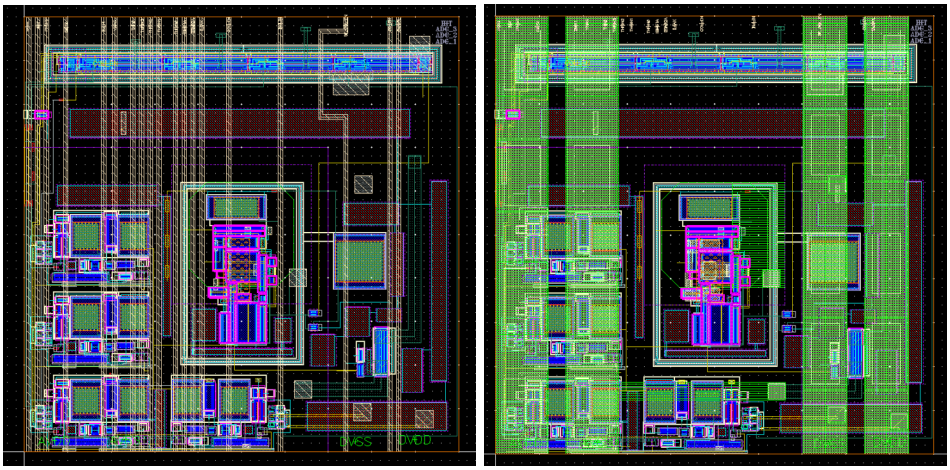



Figure 3.27: Layout level of the pixel readout front-end.

### 3.6.2 Simulations

A proper set of simulations has been carried out in order to evaluate the analog front-end, after pixel layout design. These simulations include parasitic wire

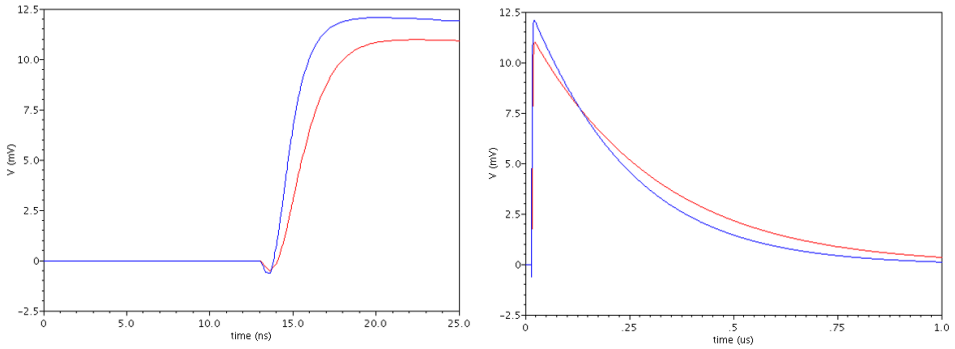


(a) (b)

Figure 3.28: Preamplifier and comparator biasing (a) and power supply and ground (b).

capacitances and resistances. This level of detail is necessary to achieve the highest degree of accuracy. While the parasitic resistances are necessary to accurately understand the delay of the circuit, a degradation in performances can be predicted very well also using parasitic capacitances.

The transient analysis at preamplifier output in Figure 3.29, performed at the schematic and layout level, show no significant variation at the signal. When a charge signal equal to 1200 electrons is injected at the input, the peaking voltage is equal to 12.5 mV (for post-layout) and 11.2 mV (for pre-layout), with negligible difference in rise time. Furthermore, considering parasitic components, the preamplifier output has lower return to the baseline, as shown in Figure 3.29(b). For a complete description of the transient analysis, Figure 3.30 represents the preamplifier output during 4 corner simulations, when a charge signal equal to 1.2, 10, 30 k-electrons is injected at the input. With respect to the Typical corner (TT), the variation in peak amplitude is $\pm$ 14%. This good result is mainly due to the MIM feedback capacitance. The detector Capacitance CD is equal to 50 fF, with 600 electrons threshold. Note that the spikes overlapping the output are due to the 40 MHz reset, but this does not condition good performance of the whole analog channel. As already described in the previous paragraph, the charge sensitivity of the CSA is defined as the slope of the straight line of Figure 3.31, which shows the four corners simulation




(a) (b)

Figure 3.29: Transient analysis at preamplifier output pre-layout (blu line) and post-layout (red line) (a) Preamplifier baseline restore (b).

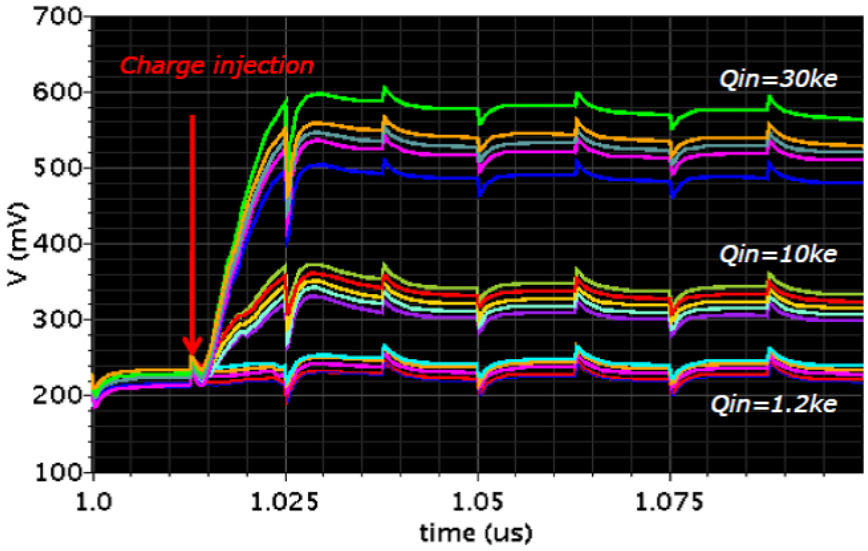



Figure 3.30: Preamplifier output during 4 corner transient simulations.

of the amplifier peak amplitude as a function of the injected charge. The charge sensitivity, calculated in TT corner, is 10.3 mV/ke. Good linearity is confirmed in all the corners.

As far as the comparator output at post-layout level is concerned, Figure 3.32 confirms good results in terms of signal processing. It shows the four corner simulations of hit comparator output when the input signal is equal to 1.2, 10, 30 k-electrons. With respect to TT condition, a change in flipping time is less than ±400 ps. Several additional simulations have been performed in

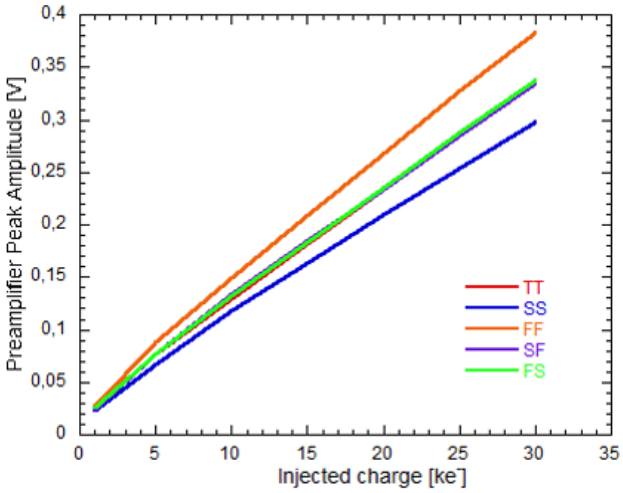



Figure 3.31: Post-layout four corner simulations of the CSA peak amplitude as a function of the input charge.

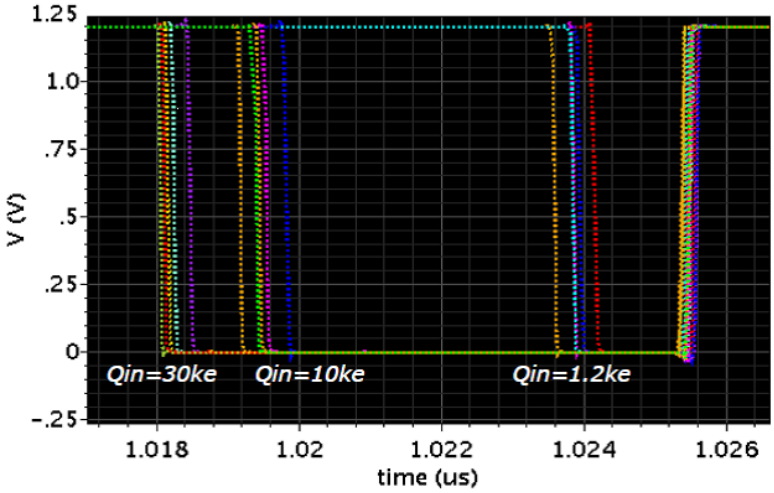



Figure 3.32: Post-layout four corner simulations of the comparator output with different input charge.

various conditions. As an example, the analog front-end output at different temperature (T = -20C) exhibits negligible changes. Only slight variations (about 500 ps) for the comparator flipping time are observed. Moreover, for different detector leakage currents a slight variation in comparator flipping time for smaller signal (around 400 ps) and non-negligible decrease in preamplifier peak amplitude for large signals is detected. The same simulations have been

carried out in 500 MRad radiation corner, showing negligible offset in CSA output response and in comparator flipping time. In order to simulate the front-end behavior after irradiation, a model of 500 MRad corner was provided by RD53 framework.

Figure 3.33 simultaneously depicts the hit and ADC comparator outputs for an input signal equal to 30 k-electrons. The threshold for the different comparators is set up independently by means of bias lines distributed through the matrix columns.

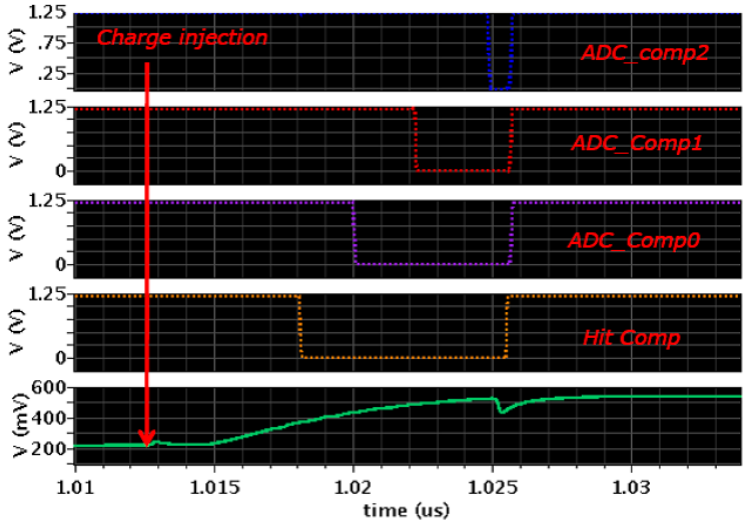



Figure 3.33: Hit comparator and ADC comparator outputs in post-layout simulations.

Simulation setup resulting in an equivalent to CDS filtering is as follows. A voltage controlled voltage source (VCVS) with a unity gain is inserted between the preamplifier output and an ideal transmission line creating a 12.5 ns delay. A second VCVS measures the difference between the preamplifier output and the transmission line output. Transient noise results show that noise after CDS is slightly lower than the preamplifier output noise. Plot in Figure 3.34 depicts the ENC as a function of CD (detector Capacitance) at temperature equal to 27C, evaluated at the preamplifier output with and without CDS simulated effects. Tables 3.6 and 3.7 enlist different front-end parameters evaluated with post-layout simulations in various corners. In table 3.6 the results are obtained considering default configuration, at room temperature and with detector capacitance equal to 50 fF. Note that the detection time is

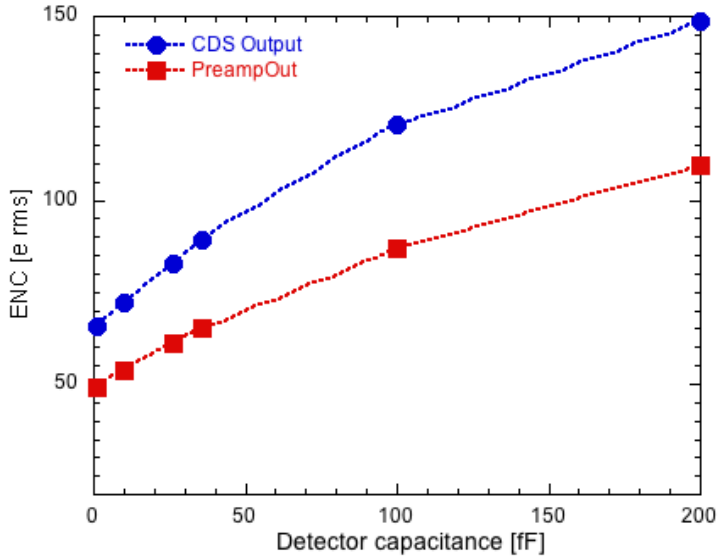



Figure 3.34: Simulation of Equivalent Noise Charge as a function of CD including CDS effects.

defined as the difference between comparator flipping time and charge injection time, when 1200 electrons are injected as charge signal input. In table 3.7, data are obtained by applying a different value of voltage to the pixel. In particular by subtracting a $\Delta$V equal to 10 mV and then to 20 mV at the pixel voltage AVDD (AVDD'=AVDD-$\Delta$V). The same $\Delta$V amount is added to ground (AVSS'=AVSS+$\Delta$V). At the same time, the peripheral biasing blocks are powered by 1.2V voltage (AVDD). The aim is to evaluate possible changes of the channel performances due to bias swings.

### 3.6.3 Digital design for data readout

A mini@asic including a 16 x 16 matrix with a simple readout has been submitted in June 2016. The designed ASIC is 2 x 2 $mm^2$, with 94 wire bond pads at the periphery, and 16 x 16 central pads connected to the pixel inputs. Figures 3.35(a) and 3.35(b) respectively show the layout of the overall matrix with 94 wire bond pads and the physical bump-bonded chip.

Charge injection and readout are controlled via three independent serial-in, parallel-out (SIPO) shift registers (SR):

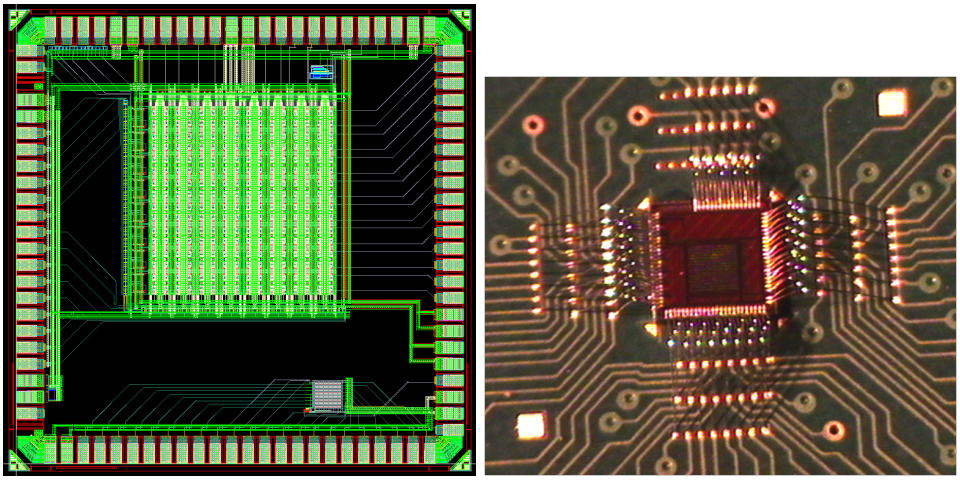
- *analog readout* (SR_preamp): the chip has 16 independent outputs (one

| ***Parameters*** | ***TT*** | ***500 Mrad*** | ***SS*** | ***FF*** | ***FS*** | ***SF*** | ***Spec*** |
|---|---|---|---|---|---|---|---|
| Charge sensitivity [mV/ke] | 13.9 | 13.5 | 12.4 | 16.1 | 14.2 | 14 | - |
| ENC rms [e] | 58 | 59 | 60 | 55 | 58 | 57 | $\ll$126 |
| Threshold dispersion $\sigma(Q_{th})$rms [e] | 35 | - | - | - | - | - | $\ll$126 |
| $(ENC^2+\sigma(\text{Qth})^2)$ [e] | 68 | - | - | - | - | - | $\ll$126 |
| Current consumption [$\mu$A/pixel] | 7.6 | 7.2 | 7.6 | 7.6 | 7.6 | 7.5 | <4 |
| Delay time [ns] | 10.8 | 12.1 | 11.0 | 10.5 | 10.8 | 10.9 | - |
| ADC conversion time [ns] | 12.5 | 12.5 | 12.5 | 12.5 | 12.5 | 12.5 | - |

Table 3.6: Post-layout simulations in different corners.

| ***Parameters*** | ***TT*** | ***Temp -20*** | ***$\Delta V$ 10 mV*** | ***$\Delta V$ 20 mV*** | ***Spec*** |
|---|---|---|---|---|---|
| Charge sensitivity [mV/ke] | 13.9 | 15 | 13.4 | 12.8 | - |
| ENC rms [e] | 58 | 56 | 60 | 62 | $\ll$126 |
| Current consumption [$\mu$A/pixel] | 7.6 | 7.4 | 6.9 | 6.2 | <4 |
| Delay time [ns] | 10.8 | 9.9 | 10.7 | 11.6 | - |
| ADC conversion time [ns] | 12.5 | 12.5 | 12.5 | 12.5 | - |

Table 3.7: Post-layout simulations in different conditions.



(a) (b)

Figure 3.35: Layout of the submitted chip (a) Physical bump-bonded chip (b).

for each row) to read out the pixel preamplifier output via the nMOS source follower (SF). The related SR has therefore 16 cells, and the data pattern should include a single 1 for correct read out. The 16 outputs (SF_OUT<15:0>) also provide the bias current for the source follower.

- *digital readout* (SR_rd): controls which pixel is connected to the pads HIT, ADC<0:3> to readout the discriminator outputs.
- *charge injection* (SR_inj): controls which pixel(s) is connected to the global line for charge injection (INJ_IN).

As described in Figure 3.36, the last two SRs are 32-bit long: the first half addresses the columns, while the second half is connected to the rows. In particular, *SR_preAmp* (top) controls what pixel in each of the 16 rows are output to the SF_OUT<15:0> pads. *SR_inj* and *SR_out* control which pixels are charge-injected and readout respectively. To make sure that only one pixel is selected, there should be a single 1 in each of these two sections. While having more than one pixel selected at the same time would corrupt the digital readout, several pixels can be selected at once for charge injection (with the limitation that shadow pixels will also be selected from the combination of rows and cols selections). For what concerns analog readout, typical operation

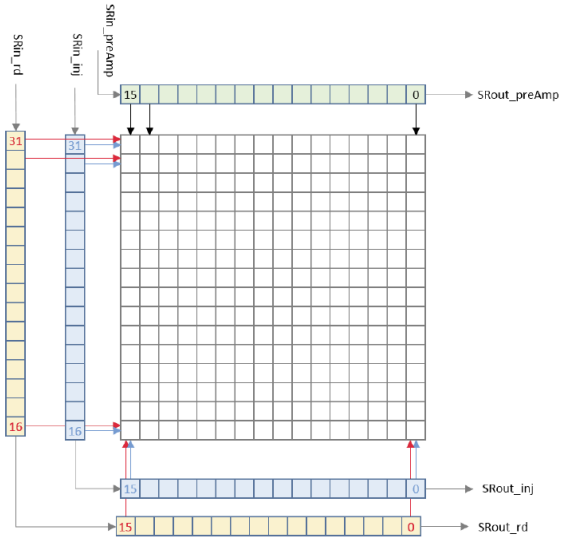



Figure 3.36: Shift register readout of the pixel matrix.

requires injecting a test signal into a selected pixel(s) and readout the data at

the preamplifier output by means of an in-pixel source follower. To perform such an operation, the pixel has to be enabled for charge injection by means of proper setting of the SR_inj, described above.

As an example, injecting charge to the top-left corner pixel, requires to have a logical 1 in SR_inj[31] and SR_inj[15], while keeping all the other SR output cell bits to 0. The charge injection takes place by providing a negative analog pulse signal at the INJ_IN pad. Notice that a 15 fF injection capacitance is connected to the preamplifier input. Thus, a 10.6 mV input pulse corresponds to a 1000 electrons input charge. A 500 ps delay between the edge of the Reset (Reset_B) signal and the input test pulse should be guaranteed for proper operation. The analog front-end includes a 35 fF Metal-Oxide-Metal (MOM) capacitor emulating the detector capacitance. This capacitance can be connected or disconnected to the preamplifier input by means of the CD_EN input pin, common to the whole matrix. If CD_EN is equal to 1.2, all the capacitances are connected to the preamplifier input. The preamplifier outputs are fed to the SF_OUT[15:0] pads. There is one SF_OUT pad per row, and one column at a time can be selected by properly configuring the SR_preAmp. As an example, a logical 1 in SR_preAmp[15] allow to readout the preamplifier outputs for all the pixels of the left-most column. Notice that the preamplifier output is connected to the pad through an in-pixel source follower stage providing a gain G equal to 0.91 V/V. Finally, Table 3.8 enlists the main signal building the analog front-end digital interface and respective properties.

### 3.6.4 New version of pixel layout for RD53A

A new version of the pixel layout has been designed for matching RD53A requirements, with particular emphasis on the analog part of the front-end. For this version the analog front-end is not integrated in the global substrate. Two different Deep-N Well (DNW) are involved in the layout: one for digital and one for analog section. The digital section is placed in DNW to isolate switching activity from coupling to the analog substrate. On a conventional CMOS process, NMOS devices are formed in a P well or substrate connected to ground. PMOS devices are formed in an N well connected to the most positive supply. Substrate noise caused by minority carrier injection into the substrate and well can be collected by the use of well taps and/or guard rings. An additional problem exists in that capacitive coupling of noise from the well

| *PAD name* | *Polarity* | *Default* | *Description* |
|---|---|---|---|
| RESET | Input | - | 40 MHz reset signal for the threshold comp and ADC. Rise and fall time <500 ps. |
| RESETB | Input | - | 40 MHz reset_bar signal for the threshold comp and ADC. Rise and fall time <500 ps. |
| ADC_OFF | Input | 0 | ADC power down bit:<br>• 0: ADC powered normally<br>• 1: ADC in shut-down mode (binary readout) |
| ADC_AND | Input | - | Logical AND between ADC_OFF & RESET |
| ADC_OUT<2:0> | Output | - | Output of the 3 comparators making up the in-pixel Flash ADC |
| HIT | Output | - | Hit comparator output |

Table 3.8: List of main PAD.

to the substrate means more noise reaches the supply. Furthermore relatively noisy digital logic cannot be isolated completely from more sensitive analog areas, since is not possible to isolate NMOS devices. A solution is to isolate the NMOS devices by using a deep N well. In summary, the use of deep N well devices can significantly reduce noise coupling between sensitive analog areas and more noisy digital regions in mixed-signal designs.

With respect to the pixel layout version previously described, the new one includes only 3 comparators, since the binary information of hit/non-hit is directly provided by the ADC. Furthermore, the digital DNW encloses the series of inverters for each comparator, as shown in Figure 3.37. A Guardring path surrounding the preamplifier is still present. Such a solution is on-going work, a possibly mini@Asic including the pixel layout just shown will be submitted in early 2017.

## 3.7 Preliminary ASIC test results

After chip submission a test board has been assembled in September 2017 and characterization activity started in October 2017. In the following paragraph very first preliminary measurement results are shown.

As far as the preamplifier is concerned, very good measurement results are obtained. As confirmed in Figure 3.38, the preamplifier output reacts very

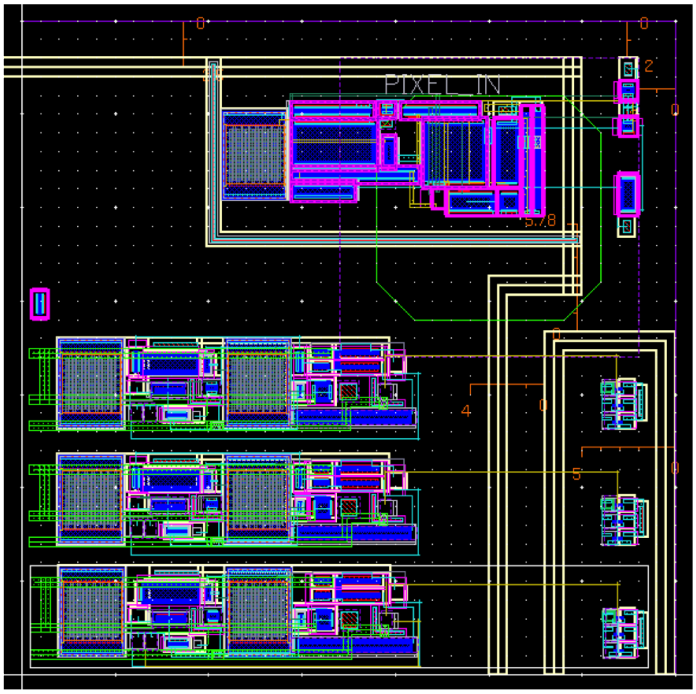



Figure 3.37: New version of pixel layout for RD53A project.

well to a voltage step at the input. With a voltage step equal to 90 mV the time constant, calculated when the signal reaches 63% of the peak, ranges from 3.1 ns to 5.7 ns. Referring to the block diagram 3.39, Table 3.9 gathers the time constant values in different configuration of injection and detector capacitances. When the injection capacitance Cinj is off, charge can still be

| ***Time constant [ns]*** | ***Cinj*** | ***Cd*** | ***Line in plot 3.38*** |
|---|---|---|---|
| 3.1 | Off | Off | Blue |
| 4.8 | Off | On | Purple |
| 4.1 | On | Off | Red |
| 5.7 | On | On | Green |

Table 3.9: Integrator time response parameters.

injected through a small parasitic from a voltage step Vinj to the integrator input. With Cinj off, the amplitude of Vinj is significantly increased to yield the same amplitude signal as obtained when Cinj is activated. Furthermore, pixel-to-pixel gain variation across the array is less than 2%.

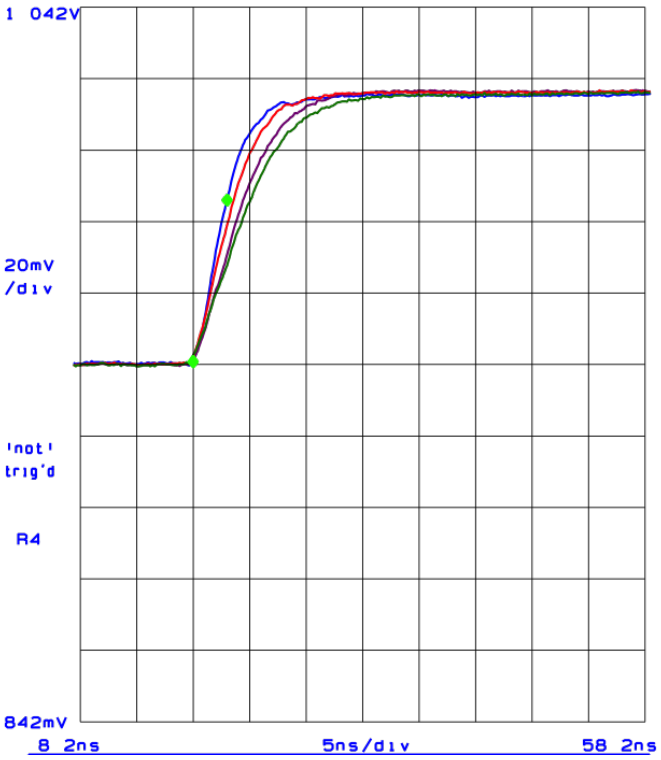



Figure 3.38: Integrator time response.

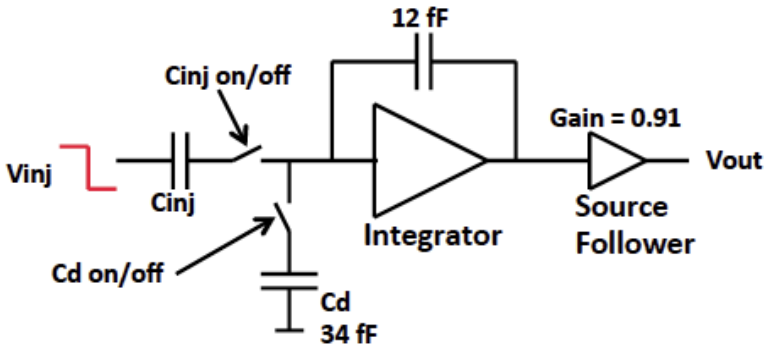
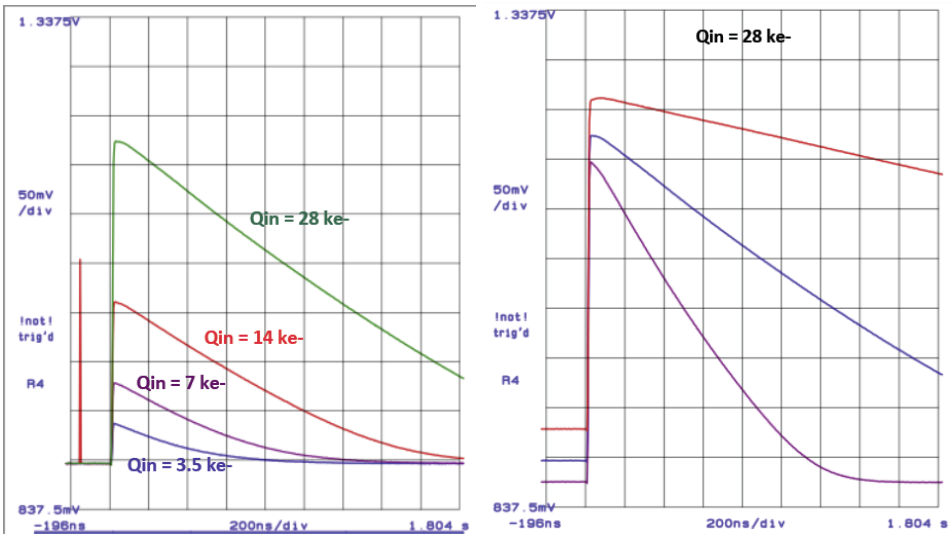



Figure 3.39: CSA block diagram.

Moreover, Figure 3.40 depict good results also in CSA return to baseline for different input charges. A constant current discharge for large signals is also detected. As already demonstrated by preamplifier simulations, the detector leakage does not affect the rise time of the CSA output response (see 3.40(b)).

Concerning the noise analysis, Figure 3.41 shows the results related to ENC




(a) (b)

Figure 3.40: CSA return to baseline for different input charges (a) CSA response for different values of detector leakage current (b).

as a function of CD, evaluated at the preamplifier output with and without CDS effects. For this measurement 15 ns sample time was used. Based on such results, CDS should be efficient for reducing low-frequency components that don't depend on detector capacitance. For a complete set of noise analysis results, Figure 3.42 represents the low frequency noise spectrum of preamplifier and CDS output, with particular emphasis on 1/f noise at the preamplifier output. However, as far as the comparator performances are concerned, a threshold dispersion significantly higher than what expected from simulations, has been detected. Considering the measurements illustrated in Figure 3.43, a voltage step equal to 16 mV (corresponding to 1100 electrons) is injected at the input. Moreover, by applying 800 electrons threshold to the four comparators in one pixel, the comparators should flip 13 ns after charge injection. All discriminators should trigger at the same time. However, a significant time dispersion in the pixel is observed. In the example of Figure 3.43 is about 5 ns from peak-to-peak.

The origin of such a threshold dispersion could be ascribed to the second stage of the comparator. In fact, it behaves as a current source that is almost switch off. After the "reset" phase, and when the first stage amplifies the

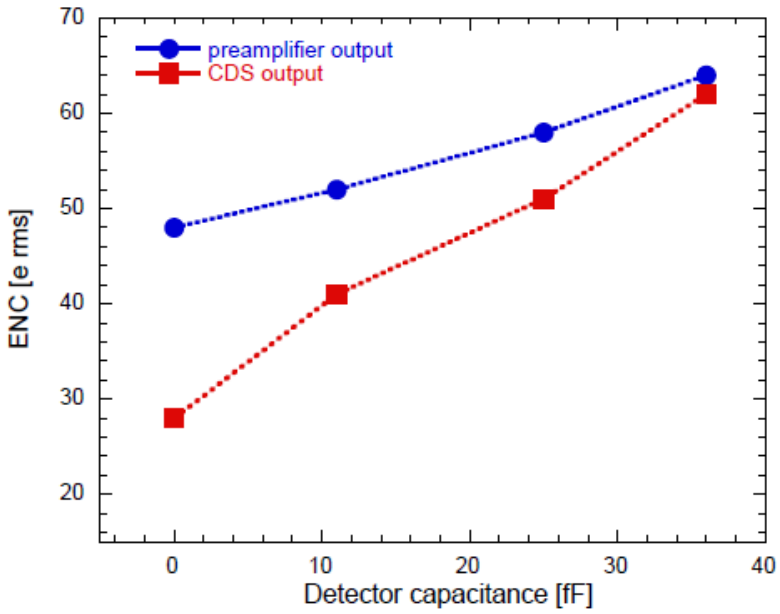



Figure 3.41: Equivalent Noise Charge as a function of CD including CDS effects.

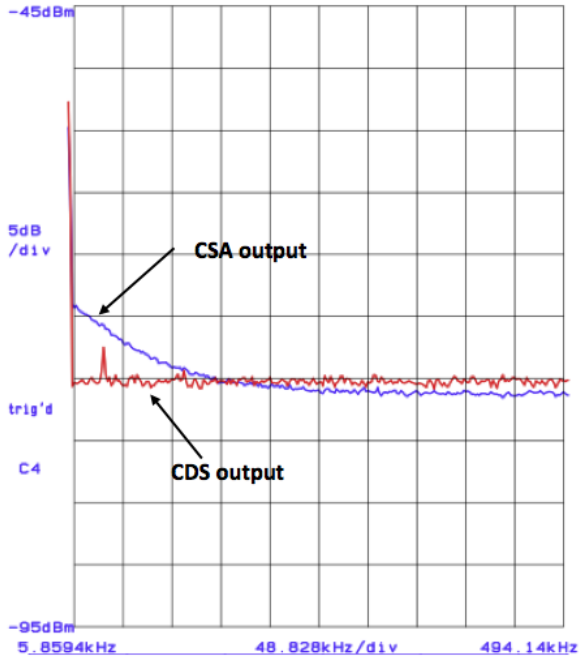



Figure 3.42: Low frequency noise spectrum.

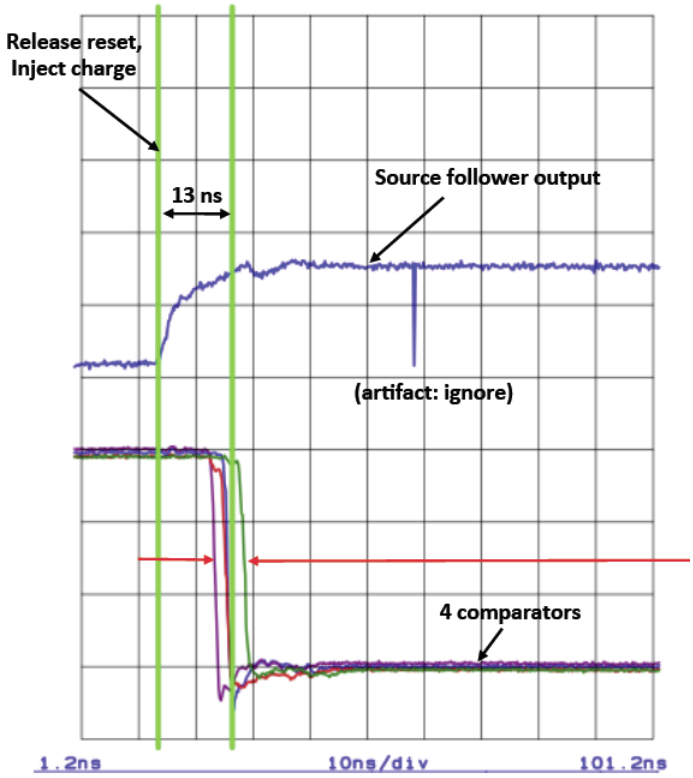



Figure 3.43: Test of 4 comparators output in the pixel.

difference signal, it switches on the current source that acts as a current-to-voltage converter and starts charging a parasitic capacitor. A higher value of threshold dispersion (146 electrons) is also confirmed by the resulting s-curve of Monte Carlo analysis in Figure 3.44. Such a simulation has been carried out considering 760 electrons threshold and without any correlation coefficient applied at the two MOSFET perform in current mirror in the second stage of the comparator. This is related to the optimistic consideration done at the simulation level (see simulation 3.23).

## 3.8 New ideas for intelligent digital readout architecture

### 3.8.1 Level-1 pixel trigger study for CMS

The front-end presented beforehand during this chapter is involved in the so-called *Level-1 pixel based track trigger for CMS* studies. Such studies engage the

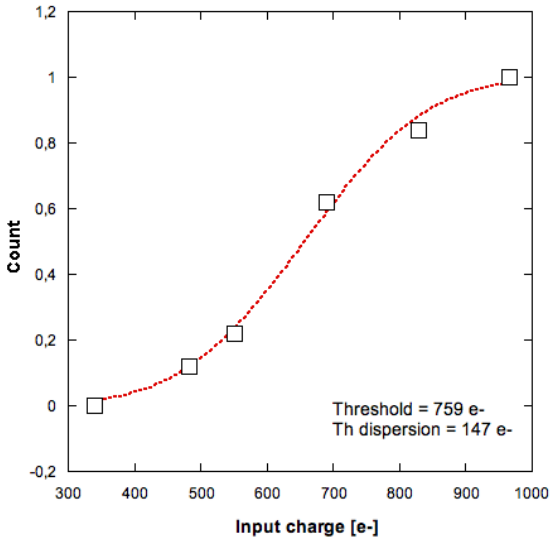



Figure 3.44: S-curve of Monte Carlo analysis for threshold dispersion.

feasibility analysis of the requirements to implement a Level-1-pixel-based track trigger to the CMS detector and they have been conducted over these past four years. This work involves different research groups: CNRS/IN2P3 (France), Cornell (Ithaca, USA), FNAL (Batavia, USA), INFN (Pisa, Italy), LIP (Lisbon, Portugal), Seoul National University (S. Korea), SPRACE-UNESP (Sao Paulo, Brazil). In this subsection the impact of such an alternative on the Front-End, and thus here the IFCP65 layout, is discussed.

As already described at the beginning of this chapter, after the first long shutdown (LS1), the current planning for the LHC and injector chain foresees two more long-shutdowns, namely the LS2 scheduled in mid 2018-2019 and the LS3 scheduled in 2023-mid 2025. During the LS2 long shutdown, the CMS vertex detector will undergo an important upgrade, in particular including the complete redesign of the ROC and the overall readout chain [60]. The pixel vertex detector will then be rebuilt for the HL-LHC starting around 2025. A series of feasibility studies have been conducted in order to investigate the performances and motivations for a Level-1 trigger based on pixels [61]. The Level-1 (L1) trigger based on the use of the pixel information can serve as one of the powerful triggers, part of the overall CMS L1 trigger architecture. First of all, the physics motivations are briefly listed in this subsection, before tackling

the main advanced possible hardware solutions currently under study, in order to implement the Level-1-pixel-based track trigger in the CMS detector.

At the HL-LHC, the proton-proton collision rate will be increased by almost a factor of five with respect to the current operation. In order to search for new physics at the electroweak scale, the use of powerful hardware and firmware tools calling for advanced technologies are essential. On one hand the L1 trigger using the pixel detector (so-called *L1 pixel trigger*) can provide the ability to efficiently select leptons and to achieve a high rejection factor in a high-rate collision environment [61]. On the other hand, pixel tracking information provides precise primary vertex determination especially along the beam axis. This is crucial for the tagging of b-quarks i.e. the secondary vertex determination. The physics motivations of the L1 pixel trigger cover several physics cases, such as: electroweak standard physics, new physics phenomena with leptons, and a large variety of interesting cases. The achieved feasibility studies [61] do show how the electron identification is improved by using the L1 pixel trigger. This is especially true in the larger pseudorapidity $\eta$ regions (endcaps and very forward). It also helps getting rid from electron-bremsstrahlung at this early stage of the selection [61]. Some important physics cases are chosen for illustrating in a bit more details, the motivation for a L1 pixel trigger. These are three physics cases considered as priority for the HL-LHC upgrade, namely: the Double Higgs production, top-antitop Higgs (ttbarH) associated production and rare decays which cover various appealing beyond standard model scenarios. Additional details can be found at [61] and references therein.

The main concept of the L1 pixel trigger is that unlike the L1 outer tracker track trigger, this is a *seeded* trigger. The seed is provided either by the electro-magnetic calorimeter L1 cluster (for electron) or by the L1 track from the L1 outer tracker track trigger (giving primary and secondary vertex precise determination as well as impact parameter which is used for b-tagging). In summary, L1 Pixel trigger is based on the pull strategy which defines the Region of Interest (ROI) where to look in the pixel device. Two cases are considered:

- Use L1 Track Trigger from the outer tracker: in this case L1 Track is the seed;

- Use the L1 tower from electromagnetic calorimeter trigger as seed.

Figure 3.45 shows the case where the L1 pixel trigger is seeded by the outer tracker L1 track. As shown the track reconstructed in the outer tracker allows defining a signal window in the pixel tracker for matching the L1 track with the relevant pixel clusters in such a window. A precise primary vertex determination is especially important when very large pile-ups occur. The combined usage of the pixel and the outer tracker information allows a very precise estimate of the longitudinal component (i.e. along the beam axis) of the primary vertex, namely 40 $\mu$m resolution instead of 600 $\mu$m (with the outer tracker only). Concerning the electron identification, a new Level-1 algorithm

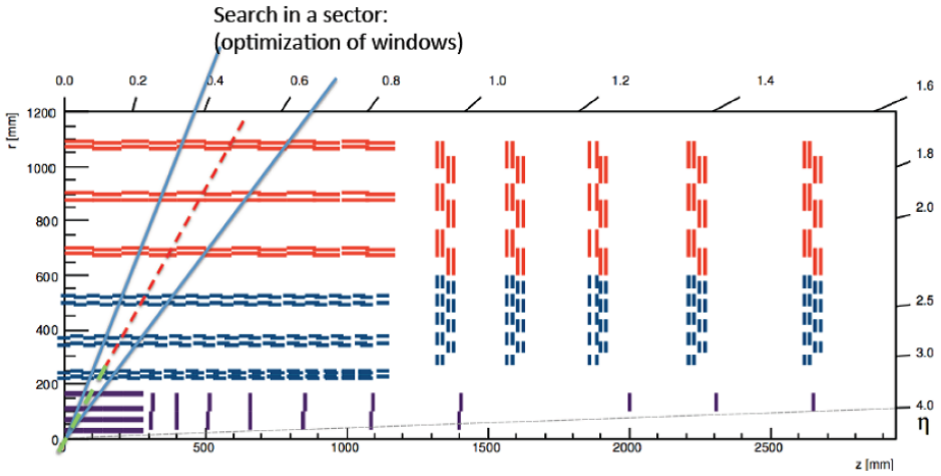
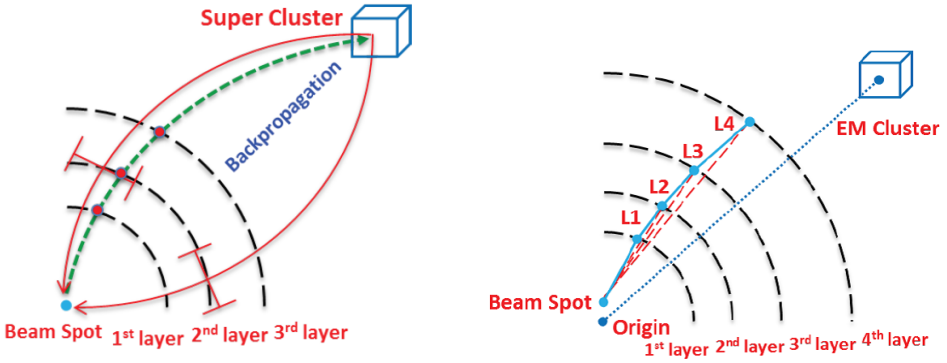



Figure 3.45: Matching of the track as defined by the L1 outer tracker trigger with the pixel track segment.

called PiXTRK [69], has been implemented by the collaboration, in order to combine pixel clusters with level-1 Electro Magnetic (EM) calorimeter tower. As an example, Figure 3.46 represents the schema describing the Pixel matching with the em-cluster in the calorimeter. In particular, the region of interest (ROI) is defined, in the transverse R-$\phi$ plane, by the L1 EM cluster linked to the beam spot (BS). R is defined as follows, where $\varphi$ is the azimuthal angle in the transverse plan to the beam axis and $\eta$ the pseudorapidity:

$$\Delta R = \sqrt{(\Delta\eta^2 + \Delta\varphi^2)} \tag{3.8}$$

The selected pixel clusters in each layer are those which are in the $\Delta\phi$




(a) (b)

Figure 3.46: Schema describing the Pixel matching with the em-cluster.

window (figure 3.46(b)) defined by the following equation:

$$\Delta\phi = \phi(BS, L_i) - \phi(BS, EM) < 0.1 \tag{3.9}$$

Where (BS, Li) is the pixel segment joining the beam spot with the relevant pixel cluster in the corresponding $L_i$ layer. The segment of (BS, EM) joins the beam spot with the L1 EM cluster. In this region pixel clusters are selected which, in each layer ($L_i$, i=1,...,4) are included in a $\Delta\phi$ window defined here by $\Delta\phi < 0.1$, and considering both the cases of electrons and positrons. In the case of more than one cluster satisfying the equation 1, all the combinations corresponding to all the possible clusters in this region of interest are considered. The pattern recognition procedure is further refined [69].

The main technical challenges for the Phase-2 Pixel Read-Out-Chip (ROC) associated with a pixel-based Level-1 trigger are the *data bandwidth* and the *L1 trigger latency*.

The overall trigger system must have sufficient bandwidth to allow selected pixel information to be kept within the limits of the overall L1 bandwidth. The hit storage at the periphery of the front-end pixel ASIC must have sufficient buffer capability until the pixel-based trigger decision is being made. As mentioned in the L1 track trigger workshop at LPC-FNAL in September 2014 [62], a preliminary estimate of the bandwidth allocated to the electron L1 trigger stated that it should not exceed more than 10% of the L1 trigger readout bandwidth. If the seed is provided by the L1 outer tracker track (or by

the muon tracks), the corresponding ROI will be extremely small and thus the bandwidth negligible. The estimated value of L1 bandwidth for the electron study, following the corresponding feasibility, is equal to 2.5% if the total L1 trigger bandwidth is 750 kHz; thus is much below the 10% limit value. As overall conclusion, because of the seeded trigger strategy for L1 pixel, the bandwidth is not a concern.

On the other hand, the baseline design for the CMS Phase-2 upgrade calls for a total L1 front-end latency of 12.5 $\mu$sec. An estimate of the time required to find stand-alone pixel tracks from the ROI readout seeded by the EM calorimeter information in the proposed electron-trigger is not yet evaluated. However it is likely that this process would be no slower than the process of finding high PT tracks in the outer trackers. The currently envisioned 10 $\mu$sec buffers would be sufficient to support the pixel-based trigger [63]. If the Phase-2 pixel ROC uses an architecture similar to the current CMS pixel ROC, it would be straightforward to implement a 20 $\mu$sec latency buffer. This is because the latency buffer is located in the chip periphery and digital logic in the new chip will take much less space than in the Phase-1 ROC, which is implemented in 0.25 $\mu$m CMOS technology using enclosed layout transistors. The new chip will be implemented in 65 nm CMOS technology. The Phase-1 ROC contains a 4 $\mu$sec latency buffer. A Phase-2 ROC with a similar architecture could include up to 20 $\mu$sec latency buffer in an area no larger than the required for the Phase-1 latency buffer. Currently the Phase-2 ROC developed within RD53 collaboration, is foreseen to use a digital layout a-la-FEI4b [64]. In this architecture, the latency buffer is distributed throughout the pixel array. The architecture has the advantage that data are moved to the chip periphery only if they are going to be read out. The largest fraction of data is not moved out of the pixel. If we assume a pixel hit rate of 2 GHz/cm$^2$ and a pixel size of 50 $\mu$m x 50 $\mu$m (or 25 $\mu$m x 100 $\mu$m), this implies a rate of 0.05 hits/pixel/bunch crossing. Together with a specification of no more than 0.1% data loss in the pixel ROC, this implies a buffer size of five hits for a latency time of 10 $\mu$s and six hits for a latency time of 20 $\mu$s [63].

In order to keep the latency and further reduce the bandwidth, three main features are essential:

- Data sparsification (zero-suppression);

- Hit pixel clusterization;
- Including a fast ROI trigger.

All these three features must first be designed within the front-end ASIC architecture. The next step will be mainly outside of the front-end ASIC, i.e. at the data transfer and upper stage in the readout chain. This means that is necessary to organize the readout chain as efficiently as possible and accordingly to the data flow for the overall DAQ system.

### 3.8.2 New ideas for including the Pixels in L1-trigger

The hybrid pixel detectors are composed by Sensor and Read Out Chip (ROC). The ROC basically contains: the Pixel Unit Cell (PUC) and the Peripheral Logic. In particular, the PUCs are organized in columns (or double columns) where each cell is bump bonded to a sensor pixel. The peripheral logic includes the end-of-column logic, the chip-level logic and the wire bond pads for power supply, I/O to DAQ system, etc. When particles are detected by the PUC, the hit informations are stored in the ROC. Only a small fraction of stored data is read out to the Data Acquisition system (DAQ) in response to a trigger; most of that are discarded. The process of hit storage can be based on the following two approaches:

- "Column drain": it sends all hits to periphery as they occur;
- Store hits in Pixel array until trigger comes. In this case only transfer hits to periphery if they will be read out.

The second approach allows smaller pixels and lower power consumption. Indeed it maximizes the rate capability. Trigger occurs either after a fixed latency (that it corresponds to a number of BX clock cycles) or as a request to read out a specific BX. Each event is time-stamped using the Beam Crossing number (BCO or BX).

In this subsection, two ongoing studies approaches are presented, both using the digital FEI4 architecture design for implementing sparsification, clusterization and ROI fast trigger features in the front-end ASIC. The reason why we chose FEI4 architecture it is because is favoured for the time being by RD53 [65]. Moreover, unlike in the ROC-Phase1 it is favoured, in the FEI4b

architecture developed by ATLAS the latency buffer is distributed throughout the pixel array. In such an architecture, the data are moved to the chip periphery for further digital processing only and only if these data are going to be read out, therefore providing sparsification by design.

We use as case study the case where the ROI is defined by the L1-EM cluster. The first approach foresees the use of a Content Addressable Memory (CAM). A CAM is a particular memory that compares input search data against a table of stored data, and returns the address of the matching data. Unlike the standard memory, CAM is particularly used in applications requiring very-high-speed searches [67]. Considering a trigger latency lasting 10 $\mu$s and BXClk equal to 40 MHz, 400 is the number of BX cycles to be taken into account. The CAM is key solution for quickly finding the match between the L1 trigger and the BX. For each end of columns a 8-bit CAM memory is allocated for the storage of 400 BX number. A schema of the architecture is shown in Figure 3.47.

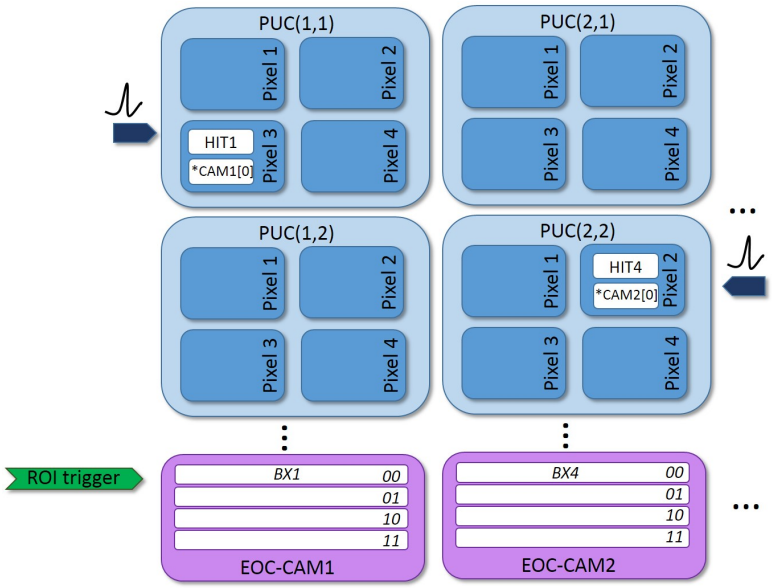



Figure 3.47: Schema of the proposed readout architecture including EOC CAMs.

The following steps describe the operating principle of the proposed architecture:

- When hit occurs in the pixel or group of pixels (cluster), the corresponding

BX number is stored at the end of column (EOC) CAM. At the same time a pointer to the EOC BX in the hit pixel is allocated.

- Hits are stored locally in the pixel array, each one with the address of an EOC CAM holding the corresponding BX.
- Hits are read out from the pixel array to the EOC in response to a match between a CAM-stored BX and the requested BX.
- When ROI triggers occur, only data with (column,row) in requested range is read out; full chip data is retained in EOC for possible later read out by general trigger.
- Data held for possible later read out (in the pixel array or in the EOC) is dropped after it reaches a specified age (number of BX cycles).

In the architecture, the hit storage is performed in each column of the matrix pixel and data are passed to the periphery only if there is a trigger. This proposal is based on an architecture presented in [68]. IFCP65 will be used for developing and testing this readout architecture. The aim is to verify the feasibility and efficiency of this fast way to extrapolate data from pixel array after ROI trigger coming. In particular, it means to studying the CAM requested size in order to include it in the overall front-end ASIC design, as well as the added power dissipation and possible complication requested in the layout.

A second approach foresees to include a second L1 trigger, in the FEI4 digital design. The inclusion of a ROI-based fast L1 trigger should provide in the overall architecture a fast extraction of the relevant hit-cluster in the ROI, to be sent to the L1 trigger correlator. According to FEI4 experts (Thomasz Hemperek, private communication), this is easy to implement. The main issue here is to study how it impacts on the data transmission and upper stage design. The ongoing work focuses on the Verilog simulation of a ROI fast L1 trigger strategy, similar to the one of FEI4-b.

## 3.9 Conclusions

A synchronous analog processor for future pixel detectors was being designed in a 65 nm CMOS technology in the framework of the CERN RD53 Collaboration.

The analog front-end includes a fast, low-noise charge sensitive amplifier with detector leakage compensation. It also includes a compact, single-ended hit comparator, able to provide a binary information at the channel output and a flash ADC. At the simulations level, the charge sensitive amplifier features a fast output response, with a 3 ns rising edge for an input charge close to 1000 electrons, and a current consumption equal to 4 $\mu$A. Non-negligible changes in charge sensitivity, designed to be close to 12.6 mV, have been detected in the four corners simulation. Such changes have to be ascribed to the use of a metal-insulator-metal capacitance as the feedback element of the charge amplifier. The comparator, operated in two different phases, is able to successfully process two consecutive events, even in the presence of a very large signal followed by a signal close to the threshold. The ADC architecture is based on the same circuit used for the hit comparator, whose average current consumption is close to 1 $\mu$A. Thanks to the very good performance in terms of threshold dispersion, the front-end channel does not require any in-pixel fine threshold tuning system. A prototype chip including the IFCP65 readout channel has been submitted in June 2016. The ASIC is 2 mm x 2 mm in size. Preliminary measurements results on the preamplifier pointed out good performances in terms of time response, return to baseline for different input charges and noise. However, a significant dispersion in flipping time has been identified for the comparator. A first analysis on dispersion effect in the comparator has been achieved, but further studies are necessary in order to better fix the problem. Moreover, systematic measurements on CSA, comparator and ADC in the whole matrix are foreseen as next steps of the work. Finally, an application of IFCP65 front-end ASIC, but still not implemented, is shown within the L1-pixel trigger studies for CMS. The aim is to verify the feasibility and efficiency of a novel fast way to extrapolate data from pixel array after ROI trigger coming, including CAM memory in the pixel or a new ROI Fast L1 trigger.

# Conclusions

In this thesis work, two different novel and intelligent microelectronics systems have been discussed and presented, focusing on their feasibility to meet advanced requirements. The goal was to study and test novel ideas for new generation of readout systems for particle detectors.

The first application concerned the development of a compact and potentially portable Radon detector for environmental applications, showing how the state-of-art can be advanced thanks to the availability of SiPMs and the new circuits. The preliminary test results demonstrated the development of a promising device for Radon detection. A general preliminary design and set of measurements was discussed, however further steps need to be accomplished. Future planes include optimization of SiPM segmentation (i.e. how many more channels of readout can the power budget afford in relation to what detection efficiency improvement can be obtained), some further noise analysis and measurements with known sources to verify the expected vs. measured detection efficiency, with consequent determination of calibration curves.

The second part of this thesis work dealt with the ASIC design of a prototype front-end for HL-LHC pixel readout system. In the framework of RD53 collaboration, the aim was to demonstrate the feasibility of the third generation of pixel front-end ASICs using for the first time the 65 nm CMOS technology. This front-end includes signal processing and synchronous analog-to-digital conversion within one Bunch Crossing, lasting 40 MHz. Furthermore,

in the context of the pixel detectors at extreme data rates, the proposal of the new digital readout architecture has been a key point in order to verify the feasibility of novel Particle Physics studies. Very preliminary tests on chip confirmed good performances for the preamplifier stage. The main issue arisen from the characterization activity are related to the threshold dispersion, which is higher than expected. Ongoing activities are focusing on the optimization of the second stage of the comparator, which is the main responsible of the high threshold dispersion, and on possible solutions to improve the signal processing, toward a new prototype chip submission foreseen by middle 2017. Future steps are devoted to systematic measurements on preamplifier, comparator and ADC in the whole chip and characterization after an irradiation campaign.

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