Transmission lines implementation on HDI flex circuits for the CMS tracker upgrade

You may also be interested in:

Transmission lines implementation on HDI flex circuits for the CMS tracker upgrade

G. Blanchot,[a] **F. De Canio,**[c,d] **T. Gadek,**[a] **A. Honma,**[a] **M. Kovacs,**[a,1] **P. Rose**[a] **and G. Traversi**[b]

[a] *CERN, European Organization for Nuclear Research,*
Route de Meyrin, CH-1211 Geneva 23, Switzerland

[b] *Università degli Studi di Bergamo,*
via Salvecchio 19, 24129 Bergamo, Italy

[c] *Università degli Studi di Pavia,*
Via Adolfo Ferrata 3, 27100 Pavia PV, Italy

[d] *Istituto Nazionale di Fisica Nucleare,*
Via Bassi 6, 27100 Pavia PV, Italy

E-mail: mark.istvan.kovacs@cern.ch

ABSTRACT: The upgrade of the CMS tracker at the HL-LHC relies on hybrid modules built on high density interconnecting flexible circuits. They contain several flip chip readout ASICs having high speed digital ports required for configuration and data readout, implemented as customized Scalable Low-Voltage Signalling (SLVS) differential pairs. This paper presents the connectivity requirements on the CMS tracker hybrids; it compares several transmission line implementations in terms of board area, achievable impedances and expected crosstalk. The properties obtained by means of simulations are compared with measurements made on a dedicated test circuit. The different transmission line implementations are also tested using a custom 65nm SLVS driver and receiver prototype ASIC.

---

[1]Corresponding author.

Contents

1 Introduction to the CMS tracker upgrade for the HL-LHC

The planned luminosity of the High Luminosity LHC (HL-LHC) requires a major upgrade of the CMS detector in order to meet the new requirements [1]. The development of the modules featuring higher granularity, lower mass and capability for the high data rate is in progress. The new electronics introduces the ability to correlate the signals locally from a pair of silicon sensors in order to enable the rejection of low momentum tracks. At the same time, a new level 1 (L1) track triggering functionality is implemented to reduce the L1 trigger rate [2]. The electronics, sensors, mechanical support and other components are designed to form an individual module that can be built, handled and installed separately.

The upgraded tracker is made of a barrel and endcap geometry with two different module types, with a sensor separation ranging from 1 mm to 4 mm depending on the radial position of the module. One module type consists of two silicon strip sensors (2S module). The other module type consists of a silicon strip sensor and a pixelated strip sensor (PS module) providing additional Z axis information for the track triggering functionality.

The 2S module front-end hybrids will use the CBC3 [3] flip chip ASICs and the Concentrator [3] ASICs that are currently under development. Using a flip chip die allows for a significant size
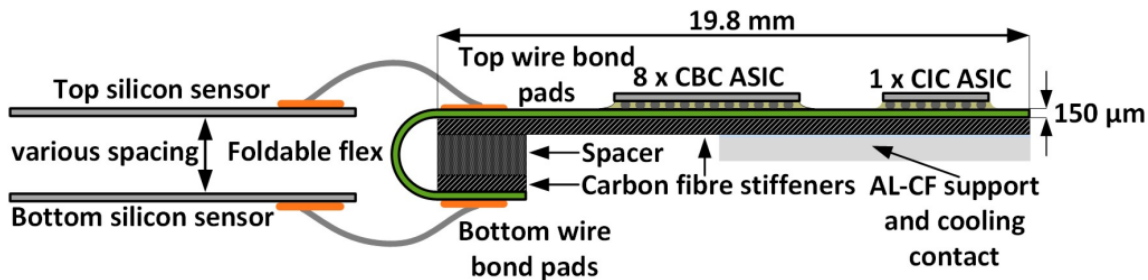
Figure 1. 2S module cross section view at the front-end hybrid fold over.
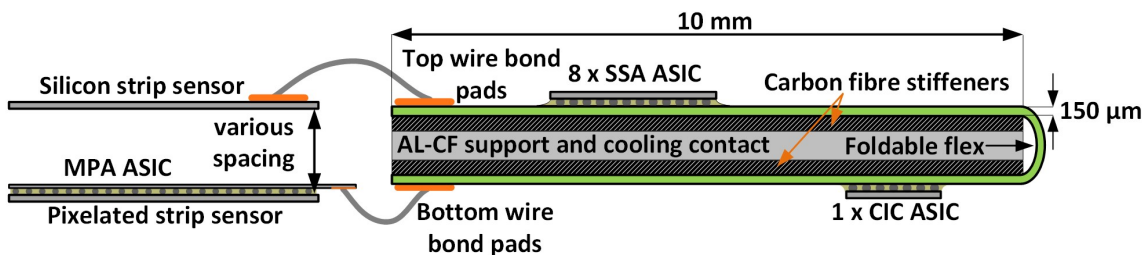

Figure 2. PS module cross section view at the front-end hybrid fold over.

reduction compared to wire bonded dies. In addition, the bump bonds have less parasitic inductance compared to the wire bonds. The usage of flip chips also reduces the complexity and time of the module assembly by eliminating a large number of wire bonds. However the 250 μm pitch of the flip chip bumps and the 180 μm pitch of the wire bond pads imposes the use of High Density Interconnection (HDI) technology in the front-end hybrids.

1.1 Modules, front-end hybrids

The Strip-Strip (2S) (figure 3) and Pixel-Strip (PS) (figure 4) modules are the two main building blocks of the upgraded CMS tracker. Each module type contains two front-end hybrids interconnecting the silicon sensors with the read out ASICs [4]. The hybrids are folded, so that the wire bonding level is set to obtain the shortest wire bond length (figure 1, figure 2). To keep the circuits sufficiently flexible at the fold-over areas and to achieve the lightest circuit, the dielectric is made of polyimide and its thickness is reduced as much as possible. The input-output signalling of the front-end ASICs is implemented with custom SLVS differential drivers and receivers [6]. In the majority of the modules, the data rate of the drivers is 320 Mbps or 640 Mbps in a few modules, where a higher speed is required. The characteristic impedance requirement of the drivers sets the target impedance of the differential pairs to 100 Ω. It is difficult to obtain this desired impedance. The thin layers of dielectric and the minimum 50 μm linewidth restriction of the circuit manufacturer results in a strong capacitive coupling between the traces and the planes, which decreases the characteristic impedance.

1.2 Input-Output requirements

The 2S hybrid has to host 62 differential pairs (max. 640 Mbps speed) and 5 single-ended traces. The front-end ASICs use six differential pairs per chip to send trigger and L1 data [3, 5] to
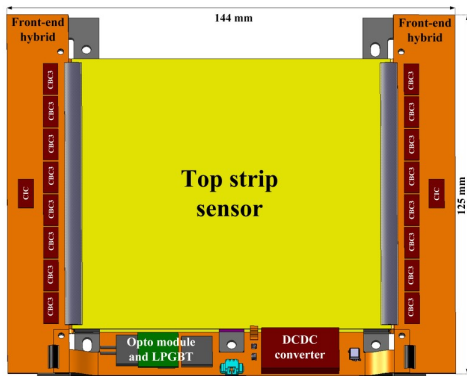
Figure 3. Top view of the 2S module design.
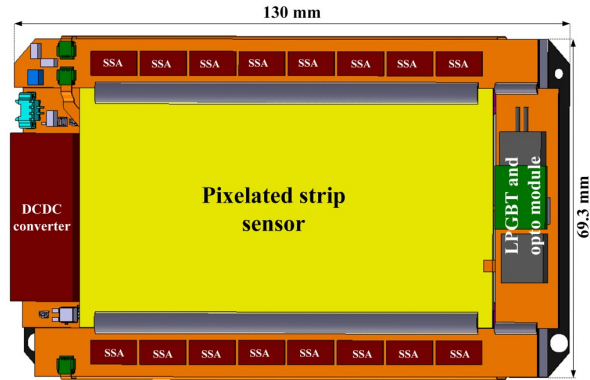
Figure 4. Top view of the PS module design.

the Concentrator ASIC (CIC). The CIC sends and receives data through the Low Power Gigabit Transceiver (LPGBT) [6] on all modules, using 11 differential pairs (figure 5 left). On every module type, 3 differential pairs are used for clocking and configuration.

The PS hybrid has to host 78 differential pairs and 3 single-ended traces. The Short Strips ASIC (SSA) is designed to read, serialize and send the uncorrelated data from the silicon strip sensors to the Macro Pixel ASIC (MPA) chip using two differential pairs. The MPA ASIC correlates the SSA data with the pixelated silicon strip sensor signals and forwards it to the CIC ASIC using 6 differential pairs (figure 5 right).
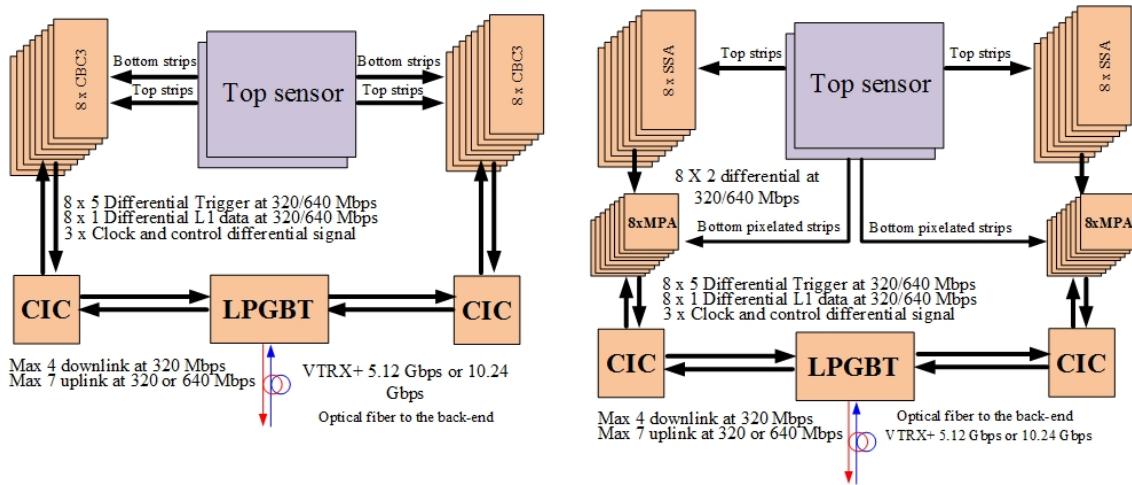
Figure 5. 2S (left) and PS (right) data flow architecture

2 Possible build-up topologies in a four layer flexible circuit

The need for low material budget and the number of interconnections in the hybrids set a four layers build-up arrangement. A ground plane and a power plane are essential and the copper area of the build-up has to stay symmetric. Because of these conditions, only a few types of differential pairs can be implemented (figure 6).

Figure 6. Possible differential pair geometries using four layers build-up.

2.1 Edge coupled microstrip

- Higher impedance compared to the other geometries on figure 6.

- Coupling with only one plane, therefore more sensitive to common mode noise.

2.2 Edge coupled stripline

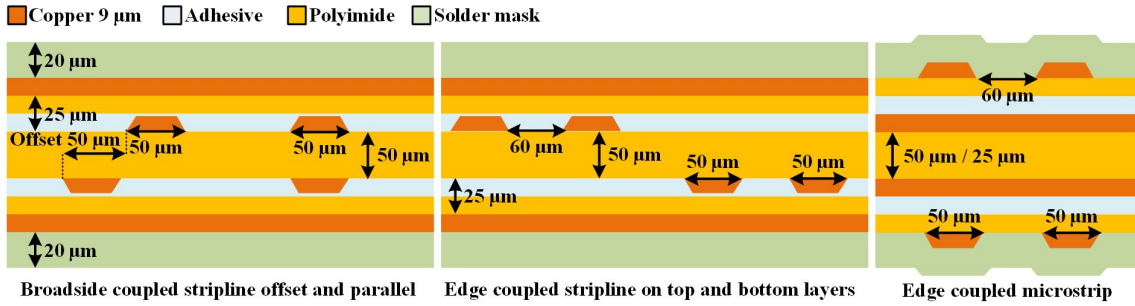- Lower impedance compared to the edge coupled microstrip geometry.

- Coupling with two planes, therefore it has better noise rejection.

- Large routing area required to avoid crosstalk.

2.3 Broadside coupled stripline

- The traces are vertically placed and they are coupling to two plane layers.

- The strong coupling between the nodes of the pair results in low impedance.

- Symmetric build up and excellent routing area usage.

- Impedance can be increased by applying an offset between the nodes.

2.4 Impedance calculations

The dimensions of the geometries, which are used in the front-end hybrids are beyond the validity range of the equations defined in IPC-2221 standard [7], therefore the equation based calculators do not provide reliable results. To estimate precisely the impedance values a 3D field solver is required. The Ansys Siwave field solver and the Polar Instruments 9000E field solver based calculator were used for the calculations. The 3D solver calculations were done at 1 GHz frequency. The two simulators show different results for the same geometry (table 1).

3 Impedance and SLVS driver test board

An impedance test board (figure 8) was designed to measure the electrical properties of the simulated differential pair geometries and to test a custom SLVS driver. The testboard consists of four

Table 1. Impedance simulation results.

Simulator	Edge coupled microstrip	Edge coupled stripline	Broadside coupled stripline	Broadside coupled stripline offset
IPC Equations	83 Ω	100 Ω	27 Ω	Not applicable
Polar SI 9000	92 Ω	71 Ω	58 Ω	62 Ω
Ansys SiWave	88 Ω	80 Ω	69 Ω	76 Ω

differential pair geometries (figure 6) implemented in two different lengths (6.7 cm and 12.7 cm). These lengths are corresponding to the shortest and longest foreseen interconnections in the hybrids. Each pair of traces is driven by one SLVS driver ASIC and received by another ASIC on the opposite side of the test board (figure 7).
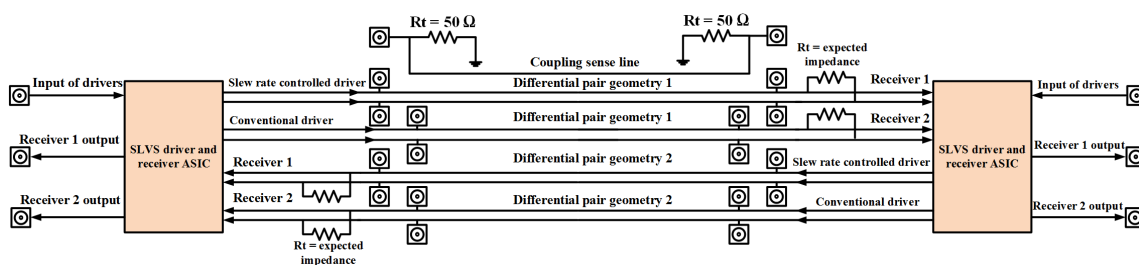
Figure 7. Schematic diagram of one test block of the impedance and SLVS test board.

Micro coaxial connectors are connected to each transmission line close to the driver and receiver side. By using these connectors, each transmission line's scattering parameters (S parameters) can be measured. The S parameters are useful to carry out simulations using the measured characteristics. Despite the very small size of the micro coaxial connectors, the stray capacitance of the surface mounting pad distorts the measurements (figure 10). Other connectors and jumpers are used to configure and power the SLVS driver ASICs. Crosstalk pickup lines are also placed at 150 μm distance from the 12.7 cm long differential pairs.
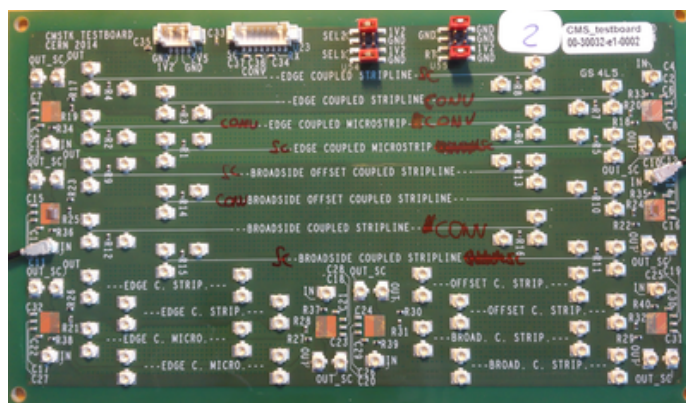
Figure 8. An assembled impedance and SLVS test board.

3.1 The SLVS driver ASIC prototype

The SLVS driver prototype chip is designed and manufactured using the 65 nm fabrication process, as well as the MPA, SSA and CIC ASICs. The ASIC consists of a slew rate controlled SLVS driver and a conventional SLVS driver [8] (figure 9). Each ASIC contains two receivers with an integrated $80\,\Omega$ termination resistor. The internal termination can be enabled or disabled. The chip size is $1.7 \times 1.5\,\text{mm}^2$ and 24 wire bond pads connect it to the test circuit.
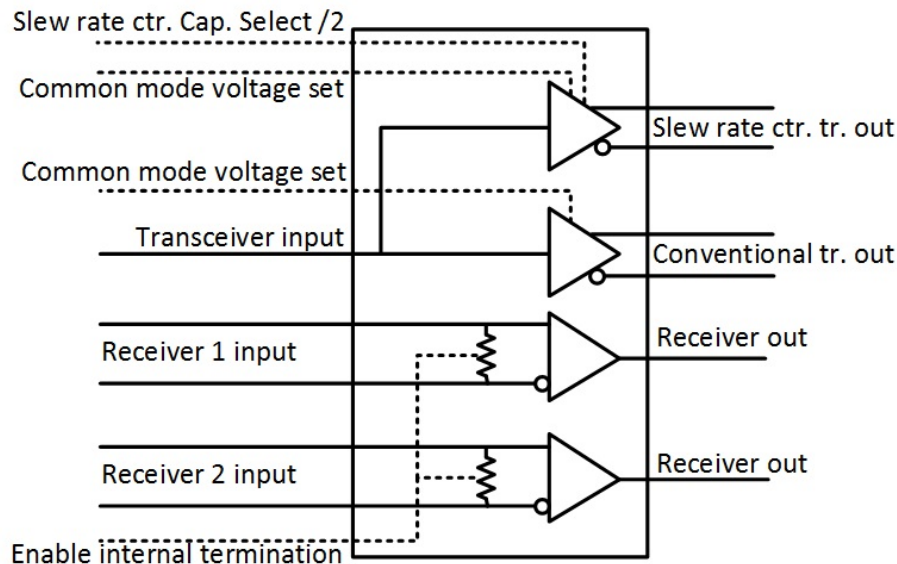

Figure 9. Schematic diagram of the SLVS diver ASIC.

4 Measurements

4.1 Impedance measurement

The impedance of the different transmission line geometries was measured by a Vector Network Analyzer (VNA). The VNA can measure the scattering parameters of the transmission media precisely in a frequency range; from few kilohertz to tens of gigahertz. The obtained S parameters have to be transformed to the time domain in order to obtain the impedance plots. To improve the results, the resistance of each transmission line is measured and the impedance plots are compensated for the DC resistance distortion. The large stray capacitance of the micro coaxial SMD pads are also distorting the measurements (figure 10).

In case of the edge coupled microstrip and the edge coupled stripline geometries, the average values obtained by the measurements are well in line with the expected impedance from the SiWave 3D field solver simulator (table 2). The measured impedance of the broadside coupled geometries is lower than the expected value from SiWave. The values calculated with Polar 9000E are showing slightly larger difference between simulation and measurement values. The mismatch of the broadside coupled geometry is probably due to some build-up thickness variation in the

Table 2. Average impedance values calculated from the measurements, compared to simulation results.

	Edge coupled microstrip	Edge coupled stripline	Broadside coupled stripline	Broadside coupled stripline offset
Polar 9000E	92 Ω	71 Ω	58 Ω	62 Ω
Ansys SiWave	88 Ω	80 Ω	69 Ω	76 Ω
Measurement	86.9 Ω	79.4 Ω	64.2 Ω	68.6 Ω

Figure 10. Impedance of different trace geometries.

manufacturing process. It is necessary to inspect the cross section grindings of the real circuit in order to validate the measurements.

4.2 Cross section grindings

Due to the manufacturing process variations, the real geometry of the circuit can differ from the design. By the cross sectional grindings, the real dimensions can be measured and the quality of the build-up can be evaluated. The precision of this inspection method is ranging between 1 μm and 3 μm. The deviations of the track width and the differential pair gap are within 10% (table 3). Due to the lamination process the thickness of the dielectric layers shows larger variations. In order to compare the results of the simulators and the measurements, the simulations were recalculated by using the real dimensions of the differential pairs (table 4).
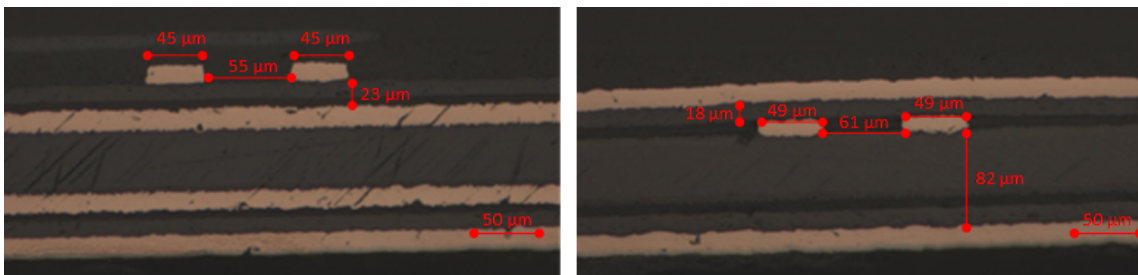
Figure 11. Cross sectional grinding of the edge coupled microstrip and stripline geometries.
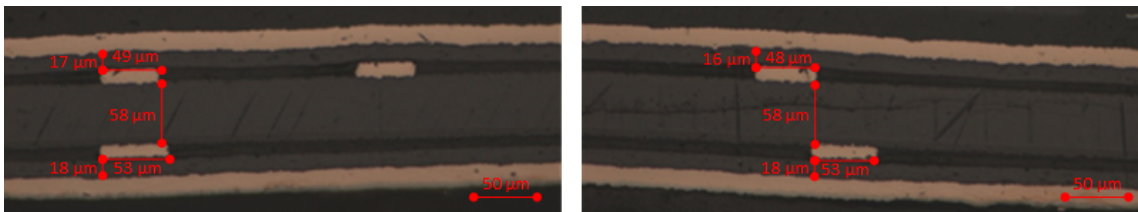

Figure 12. Cross sectional grinding of the broadside coupled stripline geometries.

Table 3. Deviation of the measured differential pair geometries from design.

	Edge coupled microstrip		Edge coupled stripline		Broadside coupled stripline		Broadside coupled stripline offset	
	Design	**Actual**	**Design**	**Actual**	**Design**	**Actual**	**Design**	**Actual**
Track width	50 μm	45 μm	50 μm	49 μm	50 μm	53 μm	50 μm	53 μm
Diff. pair gap	60 μm	55 μm	60 μm	61 μm	-	-	-	-
Dielectric 1	25 μm	23 μm	25 μm	18 μm	25 μm	17 μm	25 μm	17 μm
Dielectric 2	-	-	75 μm	82 μm	50 μm	58 μm	50 μm	58 μm

The difference between the impedance values obtained by the simulations and measurements is probably due to the build-up variations, except the Polar 9000E result of the broadside coupled stripline which is inaccurate for an unknown reason.

Table 4. Measured impedance comp. to simulation results using the real dimensions of the circuit.

	Edge coupled microstrip	Edge coupled stripline	Broadside coupled stripline	Broadside coupled stripline offset
Polar 9000E	86.9 Ω	78 Ω	47.6 Ω	69.1 Ω
Ansys SiWave	85 Ω	80 Ω	67.8 Ω	72.3 Ω
Measurement	86.9 Ω	79.4 Ω	64.2 Ω	68.6 Ω

4.3 SLVS driver measurements

The performance of the SLVS driver prototype ASICs was evaluated at 320 Mbps by measuring eye diagrams. The eye diagrams were measured close to the receiver pads of the ASICs. The proper termination was mounted on the test board, therefore the internal termination of the driver was disabled. Significant ringing and degraded eye crossing percentage are visible in the eye diagrams of all geometries (figure 13). Despite these problems, the signal quality is still acceptable in all differential pair geometries. Simulations show that the ringing is probably due to the impedance mismatch caused by the stray capacitance of the micro coax connectors. This connector will not appear in the final circuit, therefore the ringing can be eliminated.
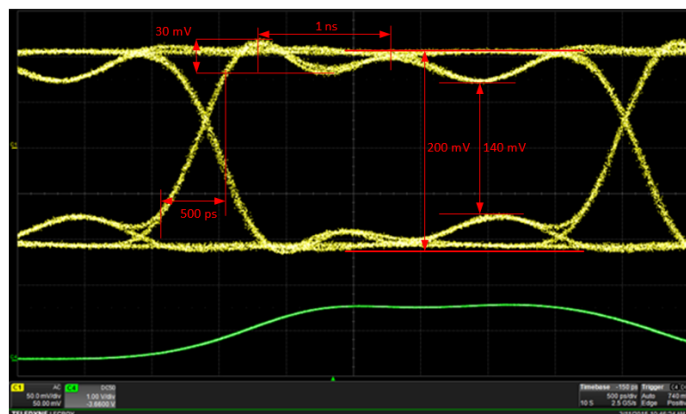

Figure 13. Eye diagram measured on the term. resistor of a conventionally driven edge coupled stripline.

4.4 Crosstalk measurement

Crosstalk pickup lines are implemented in the test board in order to prove that the planned 150 μm pair to pair spacing is large enough to keep the crosstalk sufficiently low. The measurement was carried out using a four port VNA instrument, measuring the energy coupled from the source trace to the pickup trace.

Table 5. Crosstalk measured in the frequency domain at 1 GHz and 3 GHz

Crosstalk	Edge coupled microstrip	Edge coupled stripline	Broadside coupled stripline	Broadside coupled stripline offset
Near-end 1 GHz	−47 db	−75 db	−70 db	−68 db
Far-end 1 GHz	−50 db	−75 db	−69 db	−69 db
Near-end 3 GHz	−45 db	−65 db	−62 db	−60 db
Far-end 3 GHz	−44 db	−66 db	−68 db	−64 db

The geometries coupling to two reference planes are expected to have less cross talk coupled to the pickup lines as most of the fringe fields are closed at the reference planes. The table 5 shows the near-end and far-end crosstalk at 1 GHz (500 ps rise time) and 3 GHz (100 ps rise time)

bandwidth. The crosstalk is negligible for all geometries and it proves that 150 μm pair spacing is sufficient. The edge coupled microstrip geometry has significantly higher crosstalk compared to the other geometries, but it still provides a good signal integrity.

5 Conclusions

The planned upgrade of the CMS detector requires the development of new hybrid circuits with less mass and higher data rates. Hybrid circuit prototypes were manufactured using the latest circuit manufacturing processes. Therefore limited amount of information was available about the electrical properties of these circuits. An impedance test board was designed and manufactured to measure the properties of differential transmission lines and a custom SLVS driver, using the planned build-up of the front-end hybrid circuits. The impedance of each geometry was simulated and measured. The measured impedance values were in line with the simulations carried out using 3D field solver tools. Cross section grindings show that the circuit quality is good and most of the geometries are within 10% divergence from the design target value. New simulations, which use the real circuit dimensions, show that the applied tools can precisely estimate the transmission line impedance. Although some problems were discovered during the tests, the performance of the custom SLVS drivers was still sufficient. All the tested differential pairs were able to provide sufficient signal quality at 320 Mbps with the SLVS drivers. The crosstalk between each differential pair is negligible, if the spacing is larger than 150 μm and the signal rise time is not shorter than 100 ps. The achievable impedance is the highest in case of the edge coupled microstrip geometry. Furthermore, the circuit core thickness can be reduced to obtain a lighter circuit with better power integrity. Despite the microstrip geometry is more sensitive for common mode noise, the high common mode noise rejection of the receiver stage allows for its usage. Therefore, the edge coupled microstrip is the preferred geometry to route the next hybrid prototypes.

References

[1] CMS collaboration, D. Abbaneo, *Upgrade of the CMS tracker with tracking trigger*, 2011 *JINST* **6** C12065.

[2] CMS collaboration, N. Pozzobon, *Development of a Level 1 Track Trigger for the CMS experiment at the high-luminosity LHC*, *Nucl. Instrum. Meth.* **A 732** (2013) 151.

[3] J. Butler, D. Contardo, M. Klute, J. Mans and L. Silvestris, *Technical Proposal for the Phase-II Upgrade of the CMS Detector*, CERN-LHCC-2015-010.

[4] M. Kovacs, G. Blanchot, A. Honma, A. Kokabi and M. Raymond, *Flexible front-end hybrids for the CMS outer tracker upgrade*, 2015 *JINST* **10** C01046.

[5] CMS collaboration, M. Jeitler, *The upgrade of the CMS trigger system*, 2014 *JINST* **9** C08002.

[6] D. Felici, S. Bertazzoni, S. Bonacini, A. Marchioro, P. Moreira and M. Ottavi, *A 20 mW, 4.8 Gbit/sec, SEU robust serializer in 65nm for read-out of data from LHC experiments*, 2014 *JINST* **9** C01004.

[7] *IPC-2221 Generic Standard on Printed Board Design*, http://www.ipc.org/TOC/IPC-2221.pdf.

[8] G. Traversi, S. Bonacini, F. De Canio, L. Gaioni, K. Kloukinas, M. Manghisoni et al., *Design of low-power, low-voltage, differential I/O links for High Energy Physics applications*, 2015 *JINST* **10** C01055.