an area smaller than 183 mm²

2. The central process unit is a 32 bit, ultra low power microcontroller with a floating point unit, running up to 80 MHz

3. Has geomagnetic and inertial sensor, needed to achieve a IMU (Inertial Measurement Unit) or an AHRS (Attitude and Heading Reference System). The platform embeds two accelerometers, one magnetometer and one gyroscope. The presence of two accelerometers allows the platform to implement HDR (High Dynamic Range) algorithms on linear accelerations.

4. Has environmental sensor, further expanded with sensors on the programming cradle. The I2C, UART, SPI, I2S allows the platform to connect a wider number of sensors.

5. Has acoustic sensor or rather, a digital microphone. It has also a digital audio output (I2S) to connect a DAC (digital to analog converter) and reproduce audio.

During the development of the *SensorTile*, lot of use case have been developed and three of them has been shown in Section 2.4. Its usefulness in the internet of things context has been successfully proven.

Chapter 3

Wireless Power Charger Design

This chapter describes the development of a Qi-ready wireless power charger suitable for recharging a wide-power range of wearable devices, from few milliwatts up to 5 watts. I decided to adopt the Qi specification from Wireless Power Consortium [Con] because it is the leading group in wireless power chargers and several embedded systems are available nowadays implementing Qi specifications. For example, mobile devices from Nokia, Samsung, Microsoft, Panasonic and Google embeds the wireless charging capability in their smartphones. It is clear that adopting an existing standard is the right choice rather than inventing a new one. The goal of this chapter is to develop a charging system implementing the Qi specification. Moreover, due to simplicity in algorithms implementation, the system is microcontroller based. The system must keep the efficiency as higher as possible, according to other power chargers that can reach efficiency up to 70% at maximum output power, and must implement safety features such as voltage, current and temperature monitoring.

Figure 3.1 depicts the system architecture described by the wireless power consortium [Con]. In order to achieve a system that respects the Qi specifications both power receiver and transmitter must implement the blocks shown in the figure. The power transmitter, also known as base station, is based on a power conversion unit which generates the alternating electromagnetic field transmitted between two, magnetically aligned, planar coils. The power receiver has a pick up unit that is an active rectifier used to convert the alternating electromagnetic field into a constant voltage and current. Both power transmitter and power receiver have a communication and control unit, but the communication link is unidirectional and it is implemented in order to close the loop between receiver and

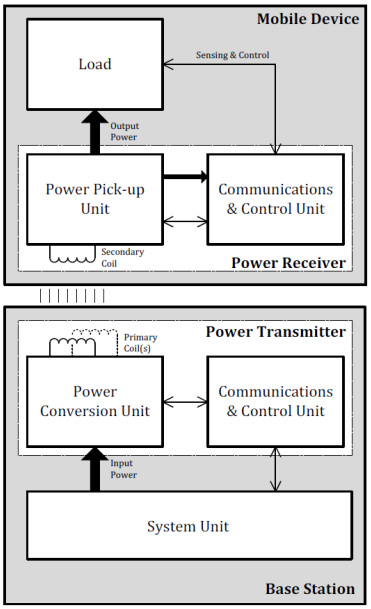


Figure 3.1: Qi standard block scheme of power receiver and power transmitter as reported in [Con]

transmitter. The communication occur using the power transmitter's carrier, by means of load modulation technique by the receiver. The communication and control unit of power transmitter decode the information and manages the power charging cycle.

In the chapter, the overall system architecture of the developed platforms for wirelessly recharge wearable devices is illustrated and a brief description of tests performed with the system for validation purpose and compatibility demonstration of the whole system is shown.

3.1 Wireless Power Transmitter Module

The aim of this section is to demonstrate that is possible to achieve a fully working, Qi-compatible wireless power transmitter based on a standard microcontroller. Up to now, technology companies that design and manufacture semiconductors offer Application Specific Integrated Circuit (ASIC) dedicated to Wireless Power Transmitter. Such ASICs usually include all that is necessary to achieve a Qi-compliant system such as the control unit (a CPU), power management, power converter, analog front-end and a precompiled library

for the firmware. It is not possible to customize the firmware, because the availability of the source code is not available.

The goal of this design is to develop a wireless power charger based on a standard microcontroller, providing:

- Schematics as reference design, easy to modify and adapt to customer specifications
- ANSI C library with source code, for a wide range of STMicroelectronics STM32 microcontrollers, implementing Qi-specifications
- Compatibility with the CubeMX HAL libraries in order to allow users to customize the source code or add features using the available microcontroller's resources

Manufacturer	Part #	HW	FW
ST	STWBC	Flexible	API, configurable
TI	bq500511A	Fixed	Integrated
IDT	P9030	Fixed	Integrated
NXP	NXQ1TXL5	Fixed	Integrated
ROHM	BD57020MWV	Flexible	Configurable
Toshiba	TB6865AFG	Flexible	Configurable
This project		Flexible	Open, with source code

Table 3.1: Commercial devices hardware and firmware customization availability

Most of the devices available up to now have source code stored into a ROM memory and it is not possible to make any customization on it, as listed in Table 3.1. Some of the device available on the market have the possibility to configure some parameters through I2C or UART bus, but there is still lot of limitations in customization. The STMicroelectronics STWBC on the contrary has an upgradeable Flash memory and the CPU is available to the users, but the developed Qi-standard code is available as a precompiled library and the customer firmware has to share the CPU load with the Qi-standard APIs. The goal is to develop an open Qi-standard library from the scratch, for any STM32 microcontrollers.

3.1.1 Block Scheme

The proposed system has been designed with an ultra low power microcontroller, provided by STMicroelectronics. The STM32L151R6H6 has a ARM® Cortex®-M3 CPU and a very rich peripheral portfolio. The power inverter section consists of two n-channel Power MOSFET, in half bridge configuration, as depicted in schematics of Figure 3.4. The high current n-channel MOSFET half-bridge inverter is driven by a high-frequency bridge controller (L6747A) and ensures an extremely fast turn-on of power MOSFETs, avoiding cross-conduction effect thus maximizing the overall efficiency [AV15]. The n-channel half-bridge inverter switch at a frequency in the 110 kHz - 205 kHz range accordingly with the required output power. Whereas the power inverter drives a LC resonant tank made of a transmitting coil and a resonance capacitor, working close to the resonance allows the inverter to increase or decrease the output power by varying the output frequency. A lower switching frequency corresponds to a higher transmitted power, accordingly to the Qi standard specification [Con].

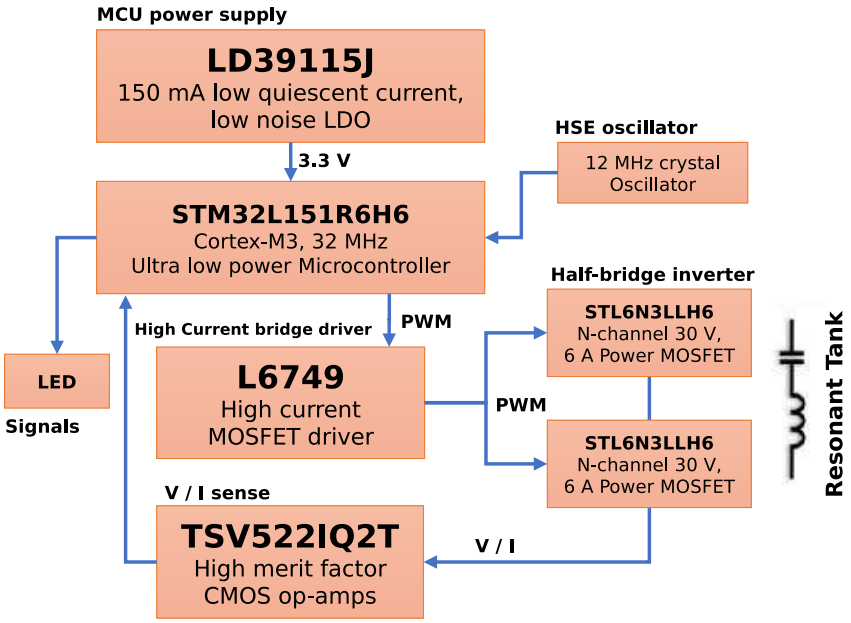


Figure 3.2: Block scheme of the STM32L1-based Wireless Power Transmitter board

3.1.2 Schematics

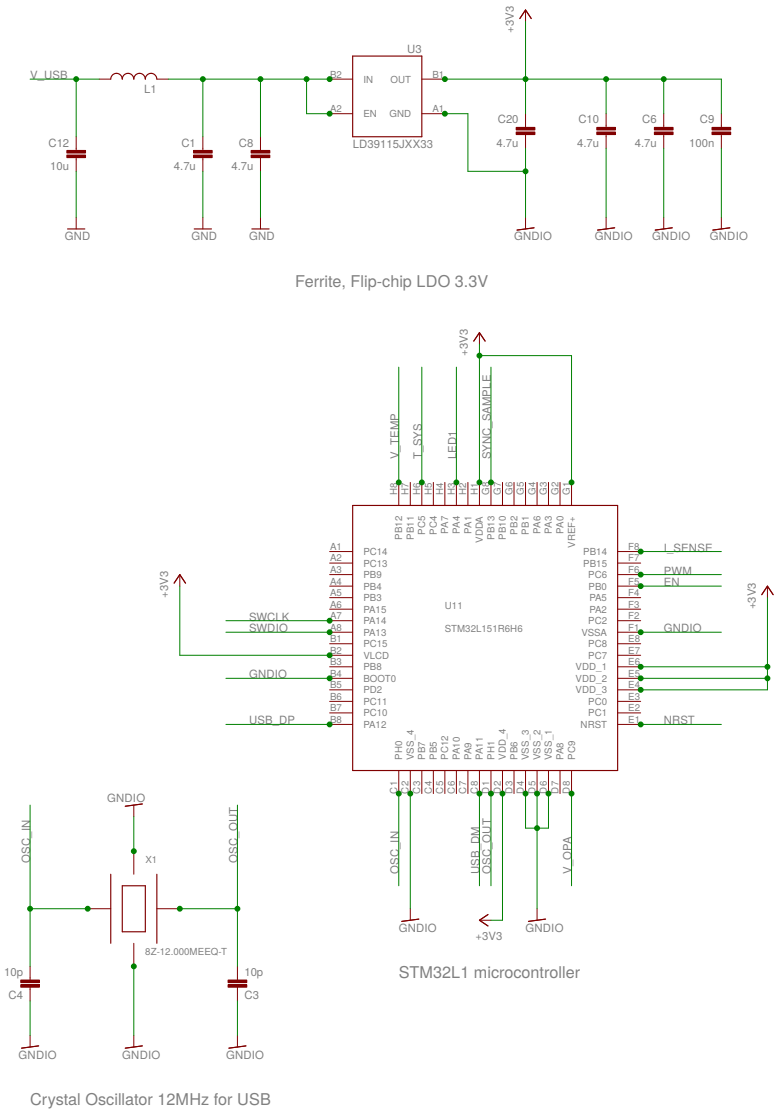


Figure 3.3: Microcontroller and power regulation section schematic

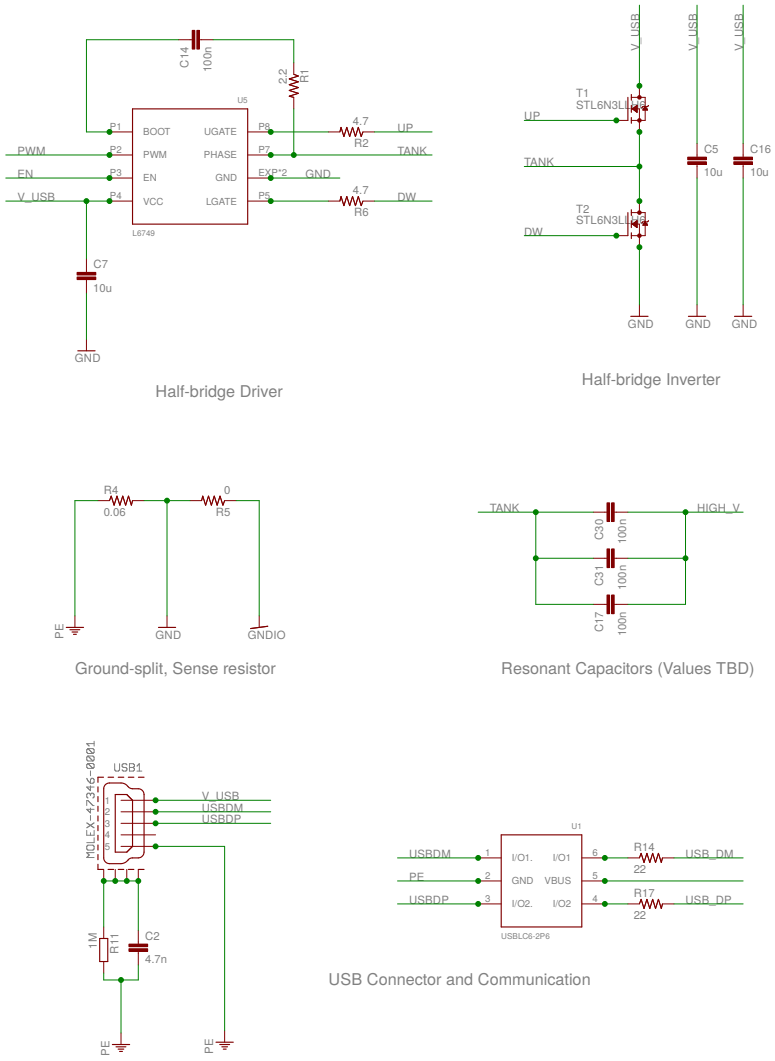


Figure 3.4: High current bridge driver, power MOSFETs and tank resonator schematic

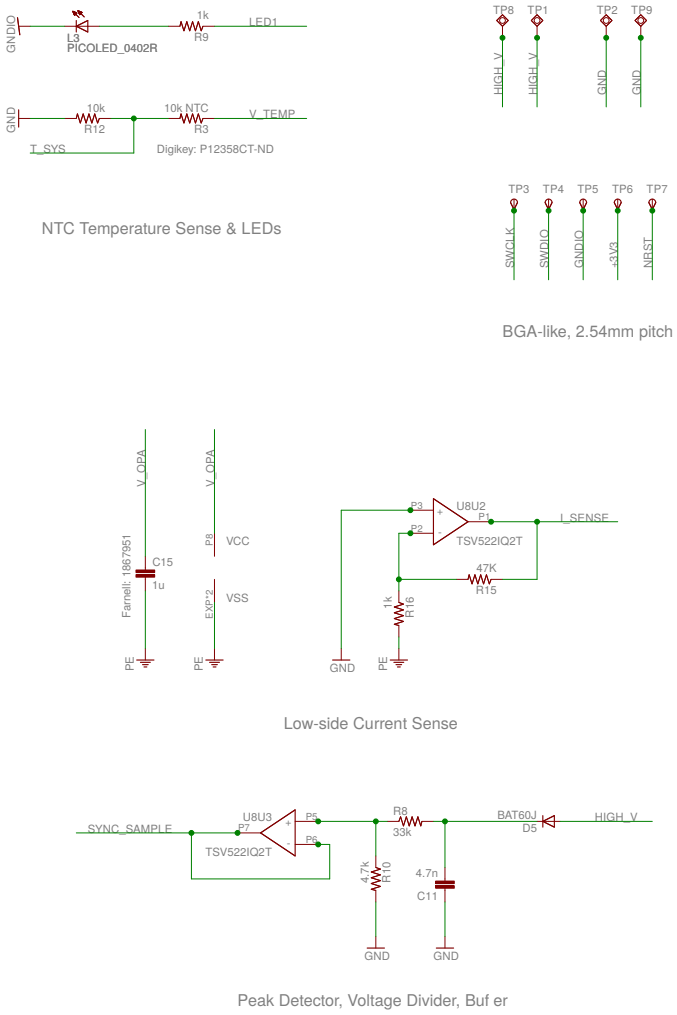


Figure 3.5: Current, voltage and temperature sense with one LED schematic

3.1.3 Layout

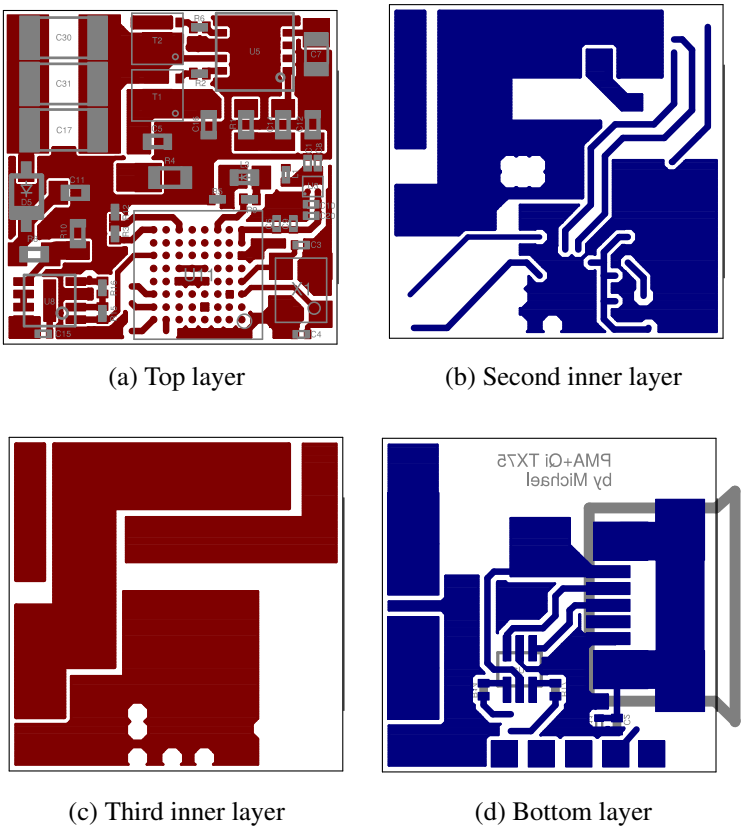
Layout of the system has been designed to fit the components in the minimum area considering, however, the thermal dissipation of the Power MOSFETs. As depicted in Figure 3.7 the layout has been designed with all the components on the topOP side of the PCB, and only the USB connector and USB protection chip on the bottom since they are optionals and can be left unpopulated. The Figure 3.7a depicts the position that has been adopted, realized in this way:

- The resonant capacitors C30, C31 and C17 are in the top left side, with a wide trace connected to the power MOSFETs T1 and T2 routed to the bottom side where there are the coil solder pads
- The bridge driver U5 is close to the MOSFETs and the driver output pins have the same length for both high and low side gate transistor
- The analog front-end (the envelope detector) and the operational amplifiers for both decode the envelope and current sense purpose are placed in the bottom left section, as much as possible away from the power MOSFETs, to keep the switching noise as low as possible
- The microcontroller U11 is place in the bottom center in order to reduce the trace length of the connections to the externals components and it has a high speed 12 MHz crystal oscillator to use the micro USB connector for communication purpose with a PC

(a) Top view 3D rendering (b) Bottom view 3D rendering

Figure 3.6: 3D rendering of the miniaturized Wireless Power Transmitter. The PCB form factor is only 13 mm X 13 mm size

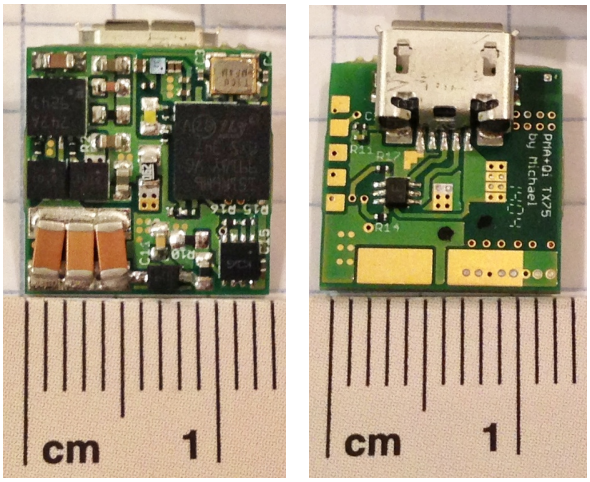
Figure 3.7b and 3.7c show the two inner layer layout. This two layer has been used to route the high-current power supply which drive the power inverter and the main ground plane. The final platform is a PCB whose size is only 13 mm X 13 mm side and all the active components have been placed on the top side, as depicted in Figure 3.8a. On the bottom side of the PCB have been placed a micro USB connector, solder pads to connect the debugger and two wider solder pads to connect the transmitter coil, as shown in Figure 3.8b.



(a) Top layer (b) Second inner layer

(c) Third inner layer (d) Bottom layer

Figure 3.7: Four layer layout, top view, of the miniaturized wireless power transmitter



(a) Top view (b) Bottom view

Figure 3.8: Photos of the miniaturized wireless power transmitter

3.1.4 Communication Unit

In this section, the schematic of Figure 3.4 is redrawn for the sake of better understanding of the power carrier generation and data demodulation. The schematic in Figure 3.9 summarized the overall high voltage power carrier generator and data demodulation block.

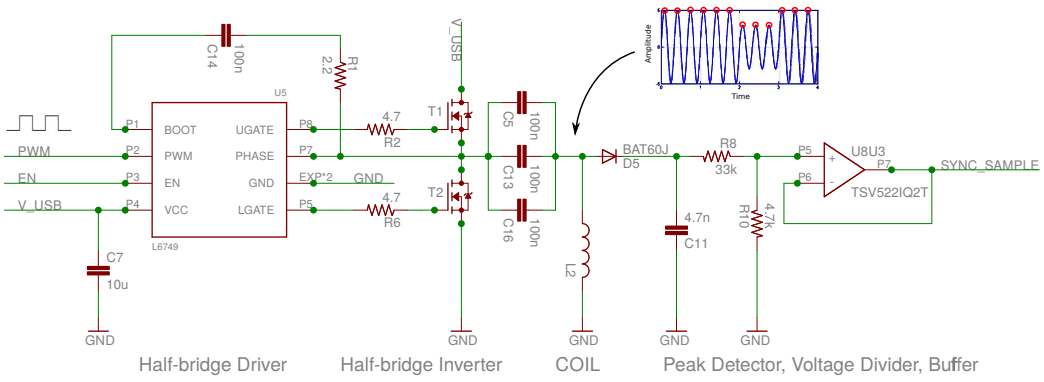


Figure 3.9: Power inverter and carrier demodulation section

As described by the Qi-specification [Con], a power receiver communicates informa-

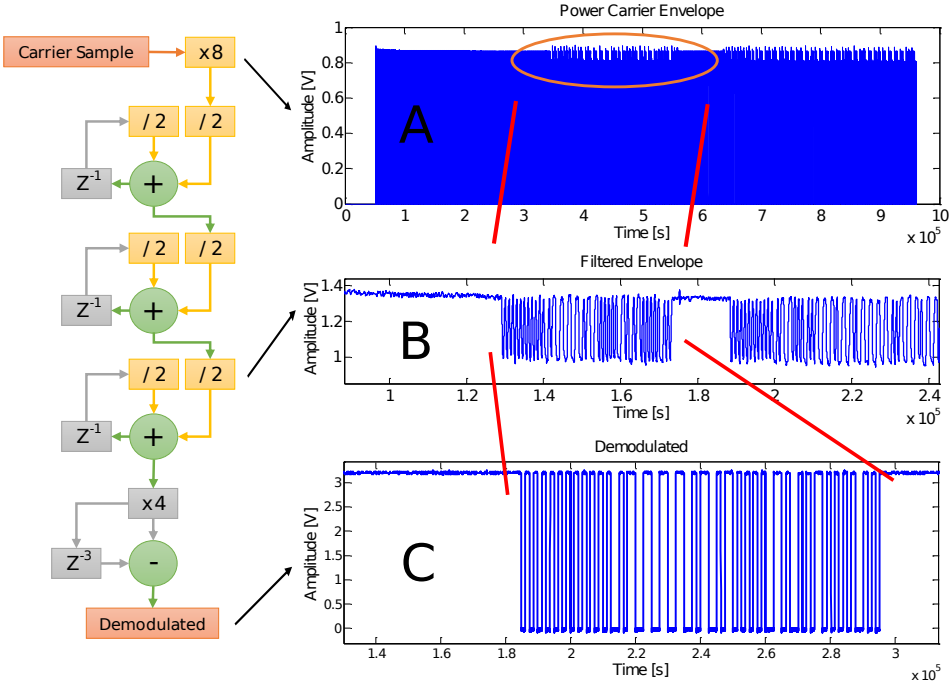


Figure 3.10: Block scheme of the digital demodulator block

tion of required power, modulating the transmitter power carrier with the load modulation technique, thus affecting the system in terms of voltage and current variation into the transmitter coil, as depicted in Figure 3.9. The developed power transmitter is able to demodulate the stream of bits sent back by the power receiver by means of a fully-digital synchronous peak envelope detector, which operates by sampling the power carrier's peaks synchronously with the inverter switching frequency. As illustrated in the schematics, only a simple protection operational amplifier is placed between the power carrier section and the microcontroller analog to digital converter. The synchronous sampling can be performed by means of the PWM timer that can also trigger the analog to digital conversion. However, sampling the power carrier synchronously with the switching frequency of the inverter implies a huge amount of samples generated by the analog to digital converter, more than 25 kS/s when switching ad 205 kHz. So a very light and real-time responsive algorithm has to be designed in order to manage such data.

The diagram in Figure 3.10 shows the structure of the implemented algorithm that, basically is a third order moving average filter. Figure 3.10 A depict the power carrier while the system is in active mode and a power receiver is modulating some information on it, by

means of a variation of amplitude in the power carrier envelope. Figure 3.10 A is the power carrier in the range of 110 kHz up to 205 kHz and the digital information is modulated at 2 kbit per second in differential bi-phase encoding of each individual bit. Figure 3.10 B reports the result of the moving average filter and shows that the implemented filter is able to extract the very small envelope from the power transmitter carrier. Moreover, Figure 3.10 C depict the output of the demodulator in which it is clearly visible that the stream of bits modulated on the carrier by the receiver are demodulated and decoded successfully. This kind of filter is very simple to implement and is very fast runtime because uses only power of 2 coefficients in the filter, thus only shifts operation and sums are coded into the microcontroller.

3.1.5 Firmware Architecture

The designed wireless power transmitter firmware is compatible with the Wireless Power Consortium 1.1 standard definitions [Con] allowing the recharge of several wearable devices up to 5 W of output power. The firmware structure combines high performance in code execution and deep sleep functions of the ARM® Cortex®-M3 Core, allowing the system to be permanently plugged maintaining power consumption as low as possible.

As depicted in Figure 3.9 the high voltage power carrier is followed by a simple envelope detector with 10:1 voltage scaling and then buffered by an operational amplifier. The power carrier is sampled by the microcontroller ADC at a sampling rate synchronous with the bridge driver PWM divided by 4. The sampled envelope is processed in software differential mode, with a predefined threshold that is able to detect when a rising or falling edge (as shown in Figure 3.10B) occurs on the power carrier, due to modulation acted by a power receiver. When an edge is detected the *WPC_Receive_Next(...)* function is called as shown in Figure 3.11 to detect if the received bit is a good candidate to be a "ONE" or a "ZERO". The *WPC_Decode_Next_Bit(...)* is triggered when a correct timing of a bit is detected.

When a preamble of at least 5 correct "ONES" is detected, after 1 ms it is assumed that the communication is completed (as per standard [Con] the stream of bits lasts always less then 1 ms after the preamble) and the received stream of bits is then parsed and decoded:

- The stream of bits is fist of all, splitted in "*preamble*", "*header*", "*message(s)*" and "*checksum*". The number of messages contained in the full stream of bits is defined

by the header and it is taken into account during the bit parsing

- Header, message(s) and checksum are checked to verify if the parity bit is consistent. If one of the parity bit is wrong, the entire sequence is rejected because no error correction code in the protocol is implemented (only a mild error detection technique is defined by the standard [Con])

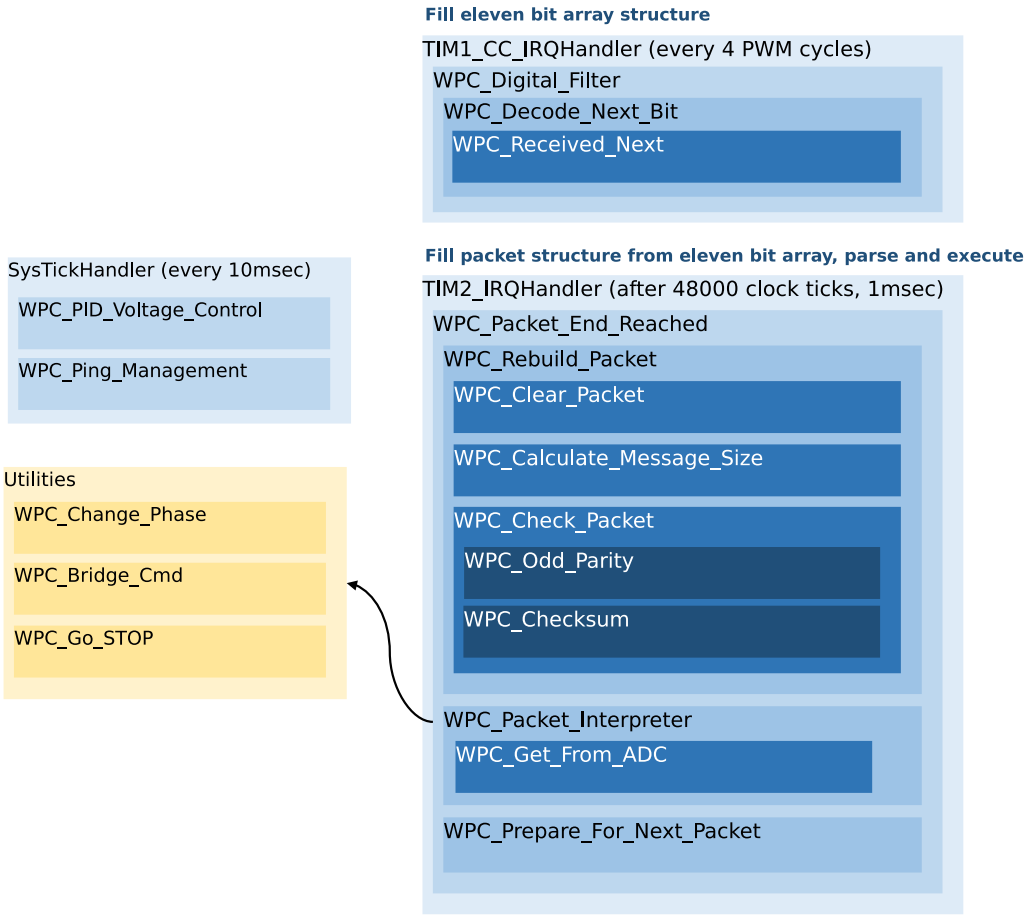


Figure 3.11: Firmware structure for discrete wireless power transmitter. The figure depicts the function call structure

- The received checksum is compared by recalculating the *checksum*(*header*, *message(s)*) and if the match is positive, both the header and message(s) are processed by the *WPC_Packet_Interpreter(...)* function that contains the state machine of the Qi specification

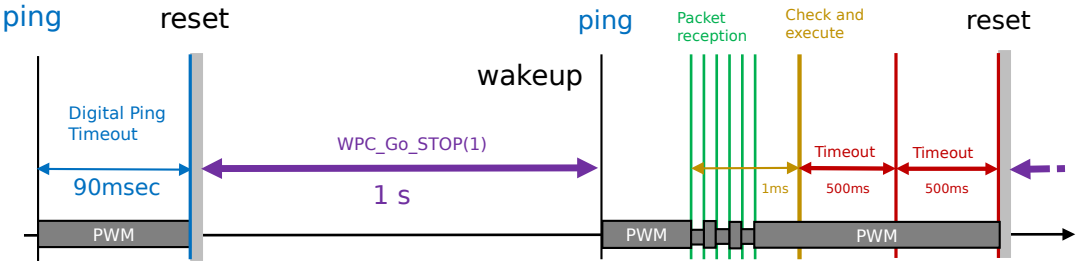


Figure 3.12: PWM power carrier during ping and transmission phase. The timing diagram shows that the Ping lasts for 90 ms and if no packet is modulated on that period, timeout occurs and the transmitter turns off the power carrier and return in stop mode for one second. If a packet is detected (modulation is present) during the ping phase, the power carrier is kept on, and a new timeout value is set to 500 ms in order to wait for the next packet.

3.1.6 Characterization

One of the major problem of systems with power MOSFETs with very low $R_{DS(ON)}$, driven by a high current bridge driver such as the STMicroelectronics L6749 is that the switching activity generates significant spikes on the power supply and this effect is unwanted in USB powered devices, because it can affect very sensitive equipments.

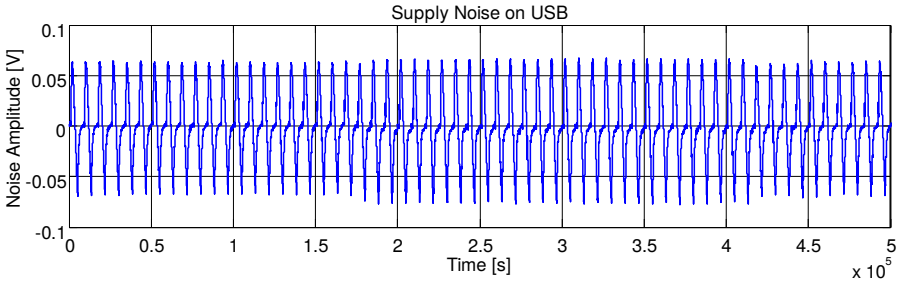


Figure 3.13: Measured noise on USB power supply, AC coupled, due to switching activity of power MOSFETs. Spikes on 5 V USB power supply are in the range of 120 mV as reported in [AV15]

In order to reduce spikes effect on power supply a Tantalum and a ceramic capacitor with very low serie resistance and very low self discharge current has been placed as close as possible to the bridge driver.

The overall system efficiency has been measured with a commercial power receiver, connected to a resistive, variable load. As depicted in Figure 3.14 the maximum efficiency can be as high as 70% at medium load and an average distance between coils of 2 mm.

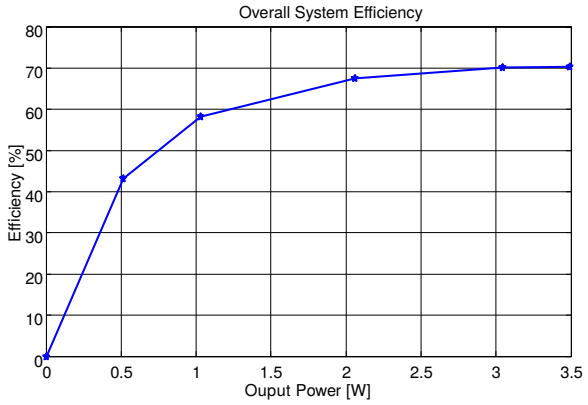


Figure 3.14: Efficiency test performed from 0.5 W up to 3.5 W. The distance between the receiver and transmitter coils is within 2 mm

3.2 Wireless Power Transmitter Evaluation kit

The developed wireless power transmitter module described on Section 3.1, is very optimized in terms of size and integration and it is one of the smallest 5 W wireless power transmitter available up to now. It can be used as a reference design platform but could be difficult to develop and modify the assembled board, if needed, due to components size.

This section will describe the redesign of a wireless power transmitter evaluation kit, with the same feature of the transmitter described in Section 3.1 but the goal to achieve a low-cost, easy to debug and modify platform.

A Wireless Power Transmitter evaluation kit based on entry-level microcontroller has been designed to focus requests from customers want to start design and working on wireless power charger devices using standard STMicroelectronics microcontroller. For the sake of development time, the firmware running on the evaluation kit of the wireless power transmitter is the same of the wireless power transmitter module, with an additional layer of abstraction to be compatible with the CubeMX HAL libraries which ensure compatibility on a wide set of microcontroller as shown in Figure 3.15.

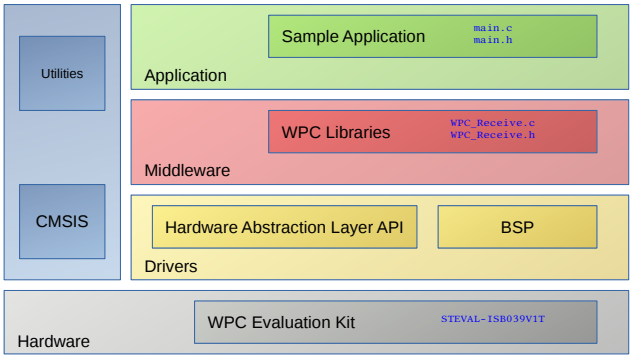


Figure 3.15: Firmware architecture. The Wireless Power Transmitter library works using the Hardware Abstraction Layer libraries by ST and allows the library to be reused on a wide set of platform.

3.2.1 Block Scheme

Few components modification of schematics of Figures 3.3, 3.4 and 3.5 has been performed in order to fulfill customer requests, and are summarized in Table 3.2.

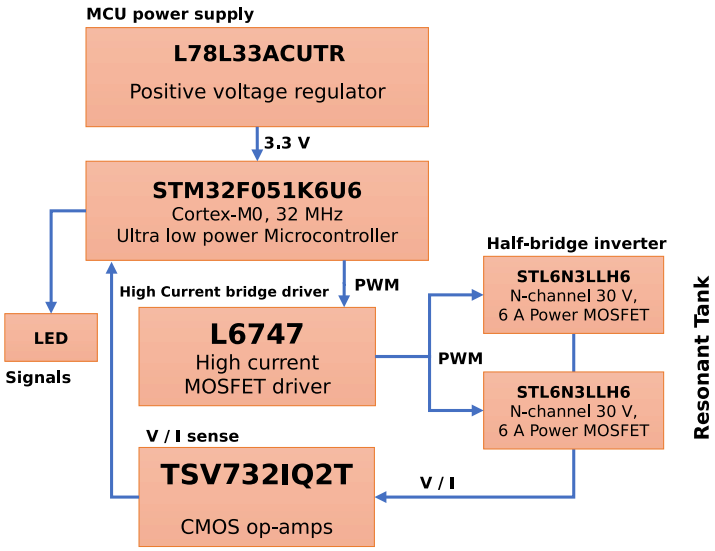


Figure 3.16: Block scheme of the STM32F0-based Wireless Power Transmitter evaluation platform

The result of this design is the official evaluation board called STEVAL-ISB039V1T and up to now, it is the only Qi-standard compatible wireless power transmitter realized with a STM32 microcontroller.

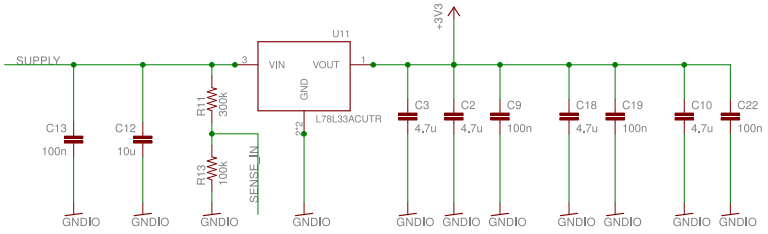
Component	Module	Eval-kit	Reason for modification
MCU	STM32L151R6H6	STM32F051K6U6	Cheaper, entry-level
Op-Amp	TSV522	TSV732	Cheaper, good bandwidth
LDO	LD39115J	L78L33ACU	Cheaper, standard
Driver	L6749	L6747	Higher availability

Table 3.2: Modifications between the wireless power charger module and evaluation kit.

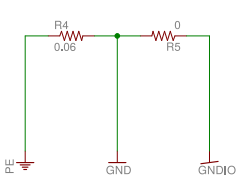
As depicted in Figure 3.2, the main reason to change some components is the price. Cheaper components are usually well appreciated by designers when mass production is involved. The differences, reported in Table 3.2, are related to:

- The microcontroller: switching to a entry-level ARM Cortex-M0 microcontroller ensures a cheaper system design, moreover computational performance and embedded peripherals match the requirements of the wireless power transmitter
- The operational amplifier has been modified with a cheaper TSV732. Despite it has a lower bandwidth compared to he TSV522, it is sufficient for this purpose
- The L6747 is almost the same high current bridge driver and differs from the L6749 only in the integrated bootstrap diode
- The LDO is switched to a standard L78x serie with the same output voltage of 3.3 V, which is very cheap and widely available from distributors

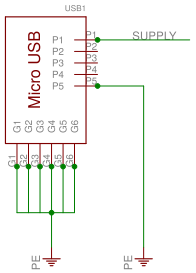
3.2.2 Schematics



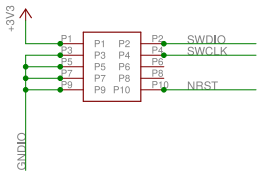
Linear regulator 3.3V



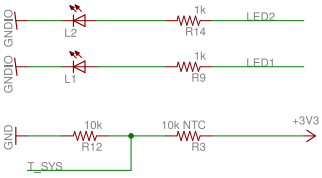
Ground-split, Sense resistor



Micro-USB connector

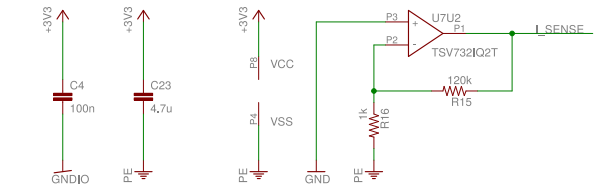


SWD debugger connector

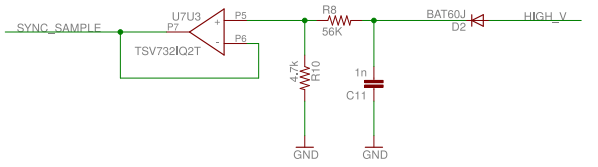


NTC Temperature Sense & LED

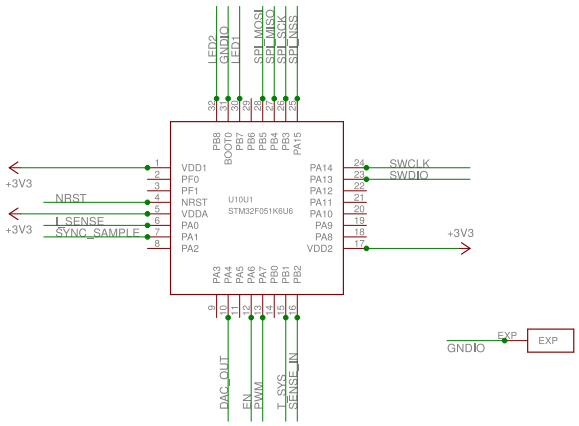
Figure 3.17: Power regulation ad connectors section schematic of Evaluation board of power transmitter



Low-side Current Sense



Peak Detector, Voltage Divider, Buffer



STM32F0 Value-Line microcontroller

Figure 3.18: Microcontroller and analog front-end for current sense and voltage envelop detection

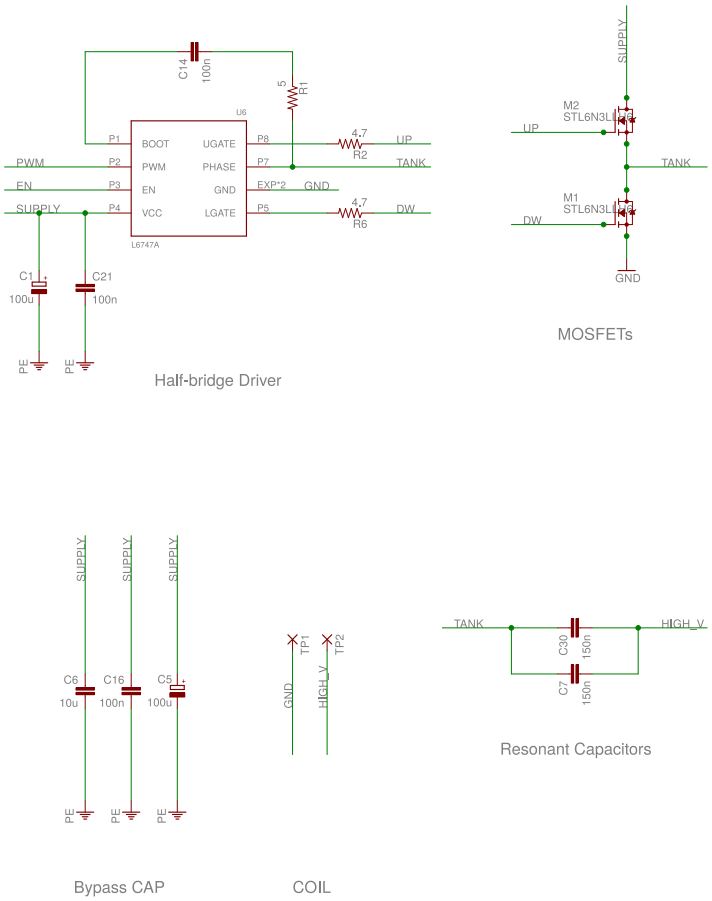
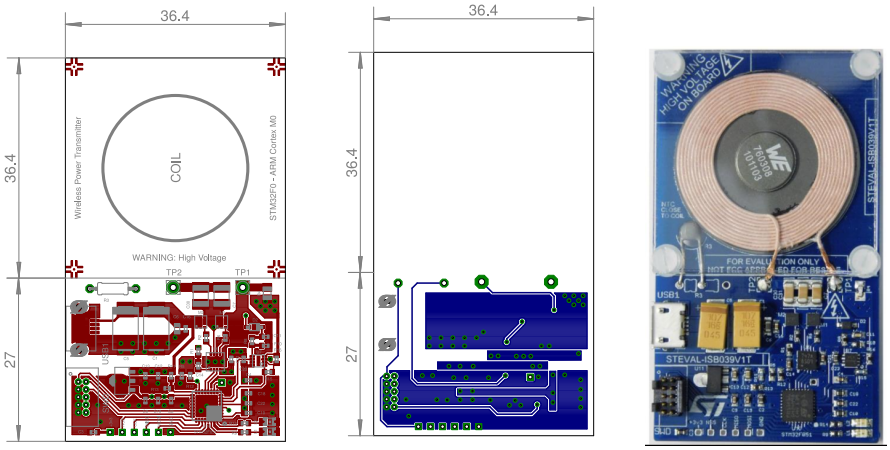


Figure 3.19: High current bridge driver, power MOSFETs and tank resonator schematic

3.2.3 Layout

The evaluation kit has been designed to keep the cost of manufacturing as low as possible, and the components have been chosen in order to be easily replaced if needed.

Compared to the wireless power transmitter module, this wireless power transmitter evaluation kit has been designed on two layers, as depicted in Figures 3.20a and 3.20b. Surface mount technology passive components with size higher than 0402 (1005 metric) have been used.



(a) Top layout (b) Bottom layout (c) Top photo

Figure 3.20: Two layers layout and photography of the evaluation kit. As depicted in this images, the platform has been designed to easily modify the PCB and probe signals available on the board

The result of this design is a 1 W wireless power transmitter (depicted in the photo of Figure 3.20c) supplied by a micro USB connector and it is suitable for recharge wearable devices.

3.3 Wireless Power Receiver Module

3.3.1 Block Scheme

Based on a cheap and very low power microcontroller, the power receiver module has been designed with a STM8L151G6U6 with a Harvard CPU architecture running up to 16 MHz.

The 8 bit architecture microcontroller has enough computational power to run a firmware that has to monitor the received power, temperature and manage the communication loop on the received power carrier.

Designed with discrete components available on the market, the power receiver has a partial-active full-wave rectifier made of two n-channel power MOSFET for the low-side (M3 and M4 in Figure 3.24) and two fast switching Schottky diodes for the high-side (D6 and D7 in Figure 3.24). The partial-active rectifier ensure high efficiency in AC/DC conversion thanks to the very low $R_{DS(ON)}$ of power MOSFETs, moreover avoids reverse currents due to the presence of the two Schottky diodes on the high side. The configuration with two power MOSFETs and two diodes allows the rectifier to be self driven when a power carrier is available on the coil, hence the rectification does not need any driver or controller to work.

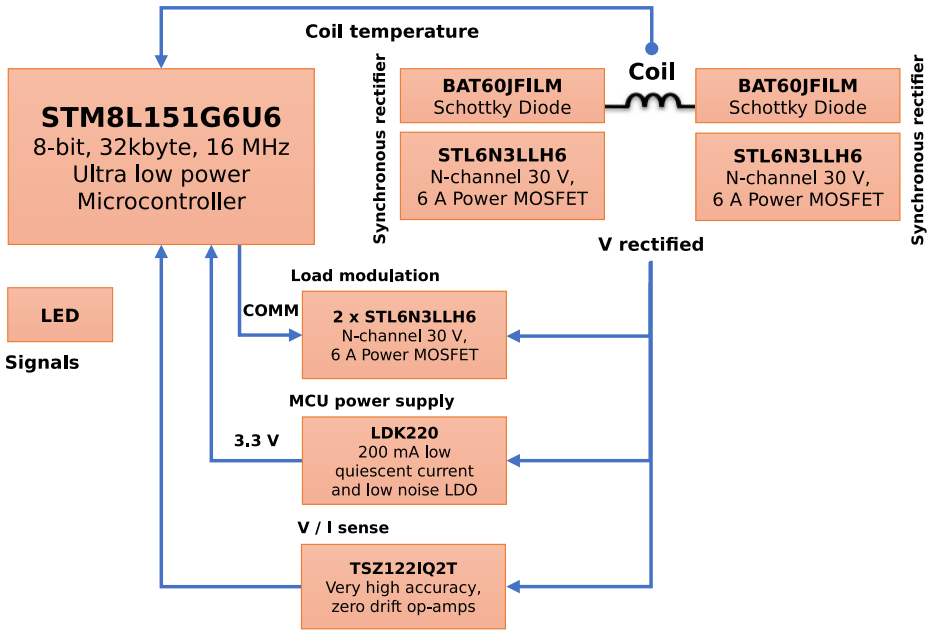


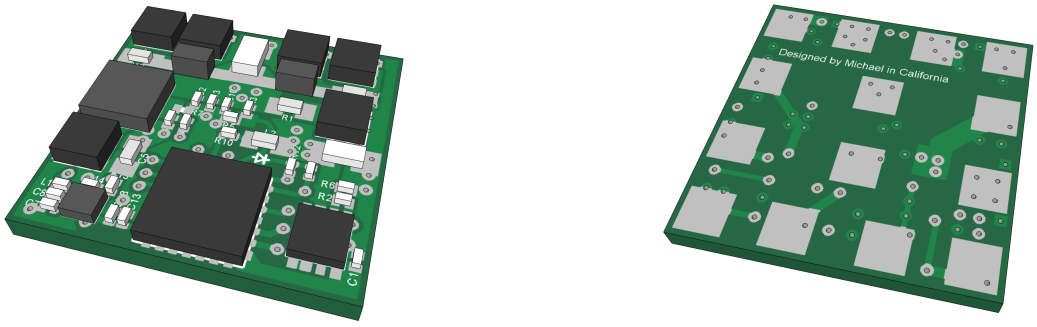
Figure 3.21: Block scheme of the STM8L-based Wireless Power Receiver board

As previously illustrated in block scheme 3.1 the power receiver has to implement a communication and control unit. The communication is mandatory in order to transmit basic information to the power transmitter on its power carrier. The communication is

performed by means of two capacitive loads (capacitors C6 and C12) activated by two MOSFETs M1 and M2 that are switched ON or OFF by the microcontroller with a stream of bits, bi-phase coded. The modulation of the two capacitive loads reflects on the power transmitter's power carrier in terms of current consumption and voltage amplitude which can be easily decoded by the transmitter's envelope detector.

For the sake of ruggedness and compatibility with all the power transmitter available on the market, also a resistive load activated by M5 power MOSFET has been placed on the schematic and it can be activated by the firmware upon request. The resistive load is placed directly on the rectified DC voltage whilst capacitive loads are placed on the received AC power carrier as depicted in Figure 3.24.

The result of this design is a compact PCB in a 13 mm X 13 mm size form factor. The bottom side of the PCB does not contain any components and has BGA-like solder pads in order to be easily used as a solderable module. Next sections will describe the design of the module, showing schematics, layouts and the firmware structure of the embedded microcontroller.



(a) Top view 3D rendering

(b) Bottom view 3D rendering

Figure 3.22: Top and bottom 3D rendering of the miniaturized Wireless Power Receiver

3.3.2 Schematics

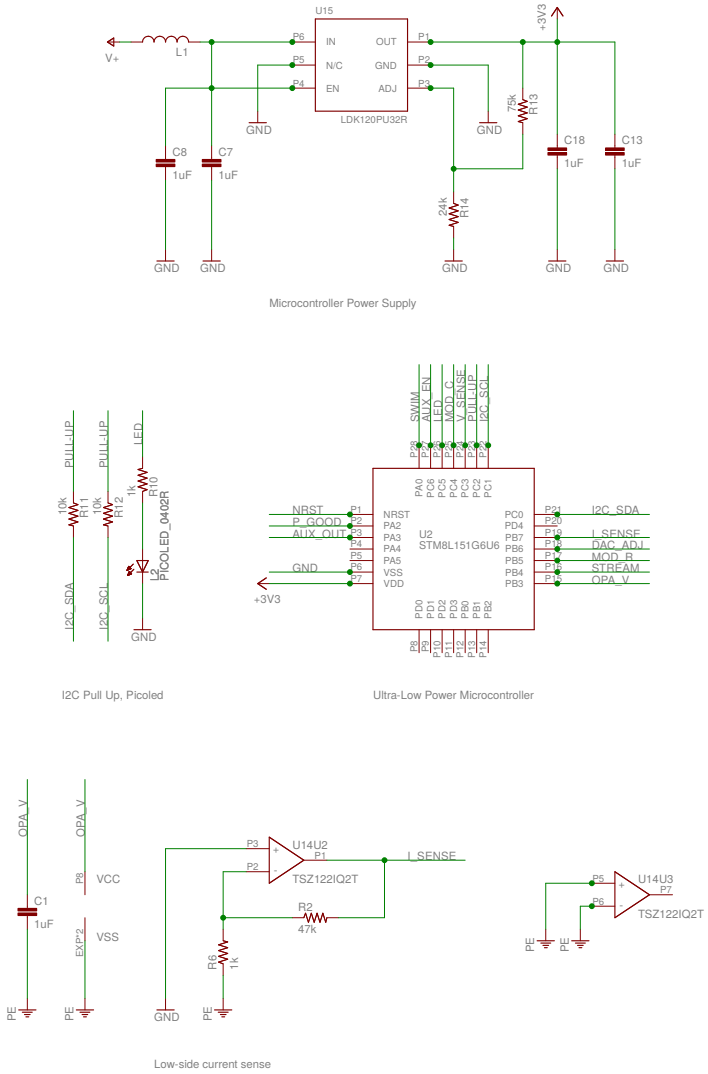


Figure 3.23: Microcontroller and power regulation section schematic

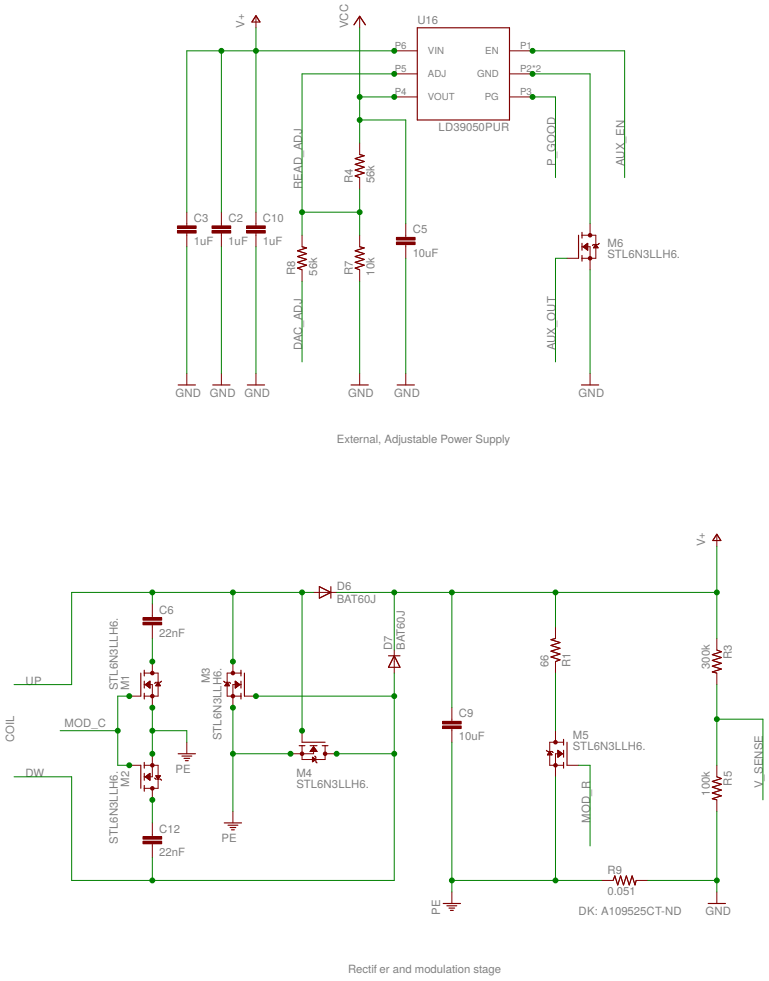


Figure 3.24: High current bridge driver, power MOSFETs and tank resonator schematic

3.3.3 Layout

The layout of the PCB takes into account the presence of both very high voltage on power rectification stage and high sensitivity requirements on voltage and current sensing section. The limited size of the PCB, which measures only 13 mm X 13 mm, makes the placement to be carefully performed. The coexistence of some high voltage and current components with some low voltage, small signal circuits is not trivial. To reduce interference on signal sensing and voltage regulation caused by the switching activity of rectifier bridge, the power section as been designed to reduce the track impedance on the high voltage side, where the AC power signal is present. The power path of the rectified signal is routed in layer 2 and layer 3 of the PCB and the tracks width has been cautiously dimensioned in order to carry such amount of voltage and current without any issue. Figures 3.25 depict the final layout of each layers.

The Figure 3.25a depicts the positioning of the components on the PCB:

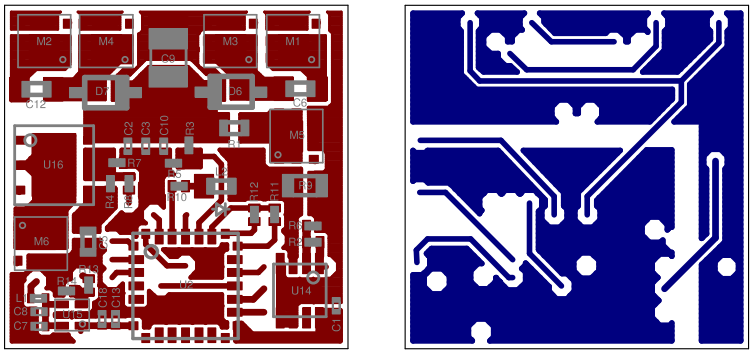
- On the top have been placed the power MOSFETs (M4 and M3) of the rectifier bridge and the power MOSFETs (M2 and M1) of the modulation stage. Very close to the rectifier diodes have been placed a 10 μF ceramic capacitor which store the rectified power.

- The microcontroller (U2) has been positioned away from the high voltage section, on the opposite side of the PCB, in the center.

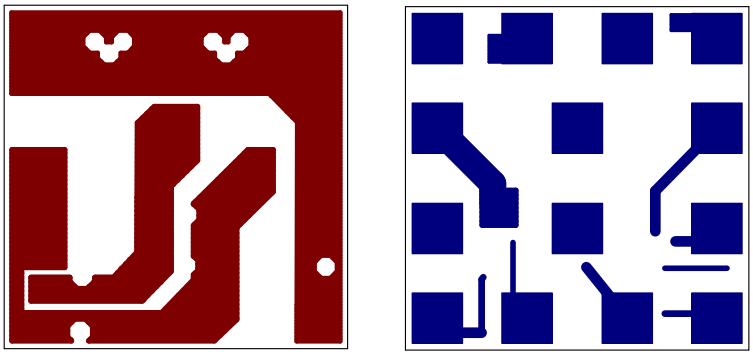
- On the left side of the microcontroller (U2) has been placed the voltage regulator (U15) which provides the 3.3 V for the system. On the close proximity of the rectifier bridge has been placed the high current voltage regulator (U16) which provides a stable voltage withdrawable by the user.

- On the right side of the microcontroller, the voltage and current sensing section has been placed. The current sense is performed using a low-side resistor (R9), and a simple operational amplifier convert the voltage drop across it into a measurable signal routed to the microcontroller's ADC.

- The bottom layer, shown in Figure 3.25d, does not have any soldered components. The layout expose 14 pins in a BGA-like style. This bottom layer allows the PCB to be used as a solderable surface mount module.



(a) Top layer (b) Second inner layer



(c) Third inner layer (d) Bottom layer

Figure 3.25: Four layer layout, top view, of the miniaturized wireless power receiver

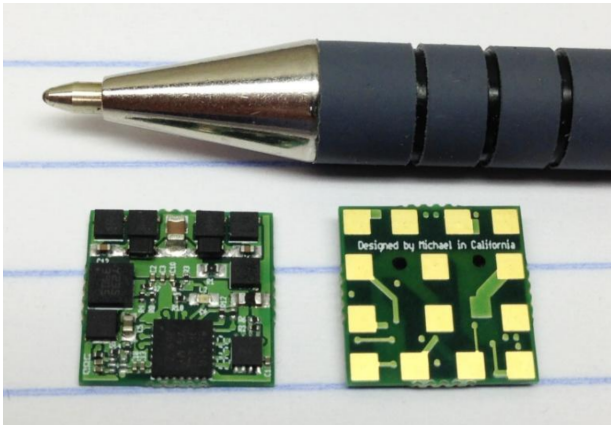


Figure 3.26: Photo of the miniaturized wireless power receiver

3.3.4 Firmware structure

From the wireless power receiver perspective, when the receiver coil is wrapped with an alternated electromagnetic field withing 110 kHz : 205 kHz range, the power rectifier starts to rectify the signal generating a direct current (DC) power supply. The DC power supply turns on the U15 low-drop linear voltage regulator which in turn supplies the microcontroller at 3.3 V.

The microcontroller tasks is to control and manage the received power, by means of current, voltage and temperature monitoring.

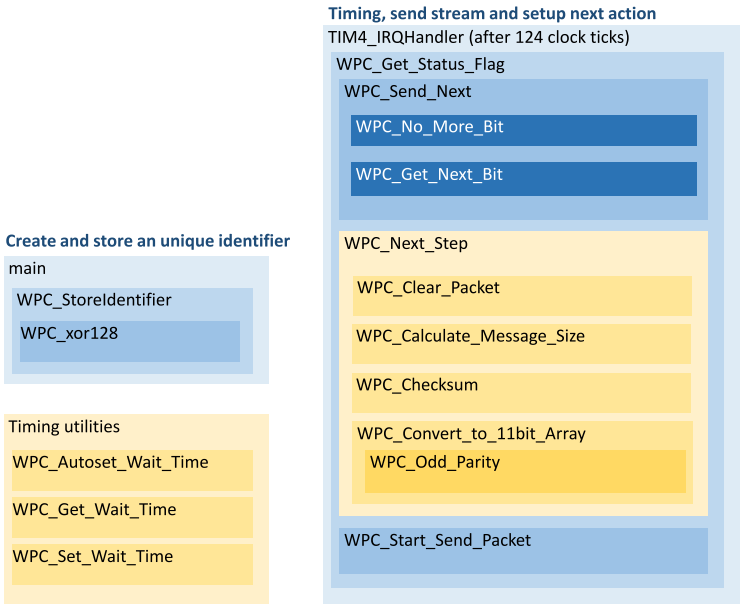


Figure 3.27: Firmware structure for discrete wireless power receiver. The figure depicts the function call structure

3.4 Wireless Power Tx / Rx ASIC development

This section describes an evolution in wireless power chargers (also known as wireless battery chargers), based on a patent-pending application by Andrea Lorenzo Vitali and Michael Galizzi named *PowerShare*. The name *PowerShare* comes from the idea of sharing wirelessly the electrical power stored everywhere (mostly accumulated in a battery pack or taken directly from the power grid) by means of a power share controller mod-

ule being operable to both transmit and receive wireless power without any change in the hardware.

Based on the same principle of the *PowerShare* idea, during the 2015 STMicroelectronics has been design a dedicated silicon chip with the same hardware capability. The silicon is the STWLC53 and it will be described in details in the next sections.

The developed wireless battery charger Application Specific Integrated Circuit (ASIC), designed by STMicroelectronics is the results of a strong collaboration between teams in:

- Catania (Italy), for ASIC hardware design
- Prague (Czech Republic), for development of the wireless power receiver firmware
- Santa Clara (California), for wireless power transmitter firmware development and external analog front-end designed and characterization

As reported on a patent-pending application titled "Wireless Power Transmitting/Receiving Devices And Methods" by M. Galizzi and A. Vitali a wireless power transmitting/receiving device includes a power transmitting/receiving element (a coil with resonant capacitors), power MOSFET switches, current/voltage sensors and a controller. Each of the plurality of power MOSFET switches has a control terminal and a conduction terminal, with the conduction terminal being coupled to the power transmitting/receiving element. The current sensor senses a current through the power transmitting/receiving element, and the controller is configured accordingly to control the plurality of switches based on the sensed current.

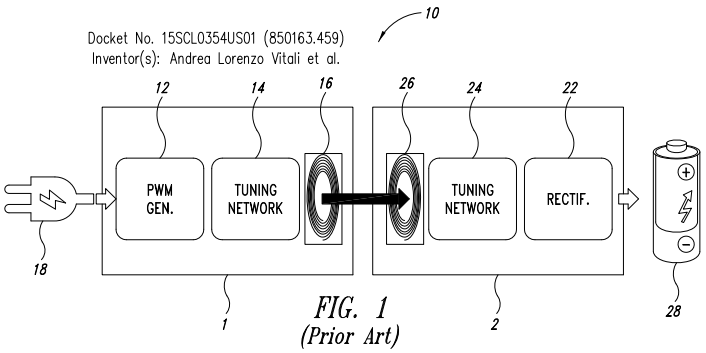


Figure 3.28: Prior Art block diagram of wireless battery chargers. As specified by the

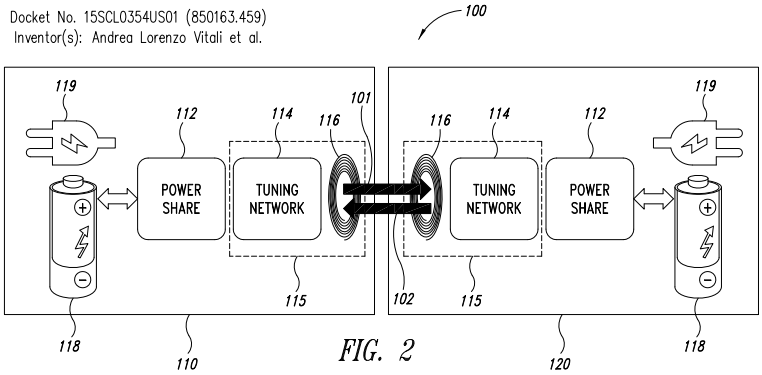


Figure 3.29: *PowerShare* patent pending application block diagram

3.4.1 PowerShare development

3.4.2 Development on FPGA board

The first step carried out in silicon chip development was to simulate and validate the digital section (such as CPU, memory, timers, watchdogs and interfaces) on a field-programmable gate array (FPGA) board, properly programmed. The FPGA board is a very versatile device containing a huge number of programmable logic blocks that can be configured to simulate an application specific integrated circuit (ASIC). The FPGA board used to simulate the PowerShare architecture is the Xilinx Virtex®-6 evaluation kit, as depicted in Figure 3.30, which provides a high performance environment for system design.

The FPGA code can be loaded on Xilinx Virtex®-6 chip via an external CompactFlash memory that automatically load the code at the power up. The code which emulates the ASIC has been developed by the hardware design team in STMicroelectronics and it can emulates:

- ARM® Cortex®-M4, 32 bit central processing unit running up to 32 MHz with 32 kB of ROM memory, 8 kB RAM and 4kbit of non-volatile memory (NVM)
- Full speed (32 MHz) TIM0 with advance PWM control. The advance TIM0 timer can generate 4 PWM signals with an accurate dead-time control. The dead-time control is useful to avoid the short circuits on the same side of the bridge. TIM0 output can be also routed to the ADC trigger input in order to sample the envelope synchronously with the power carrier

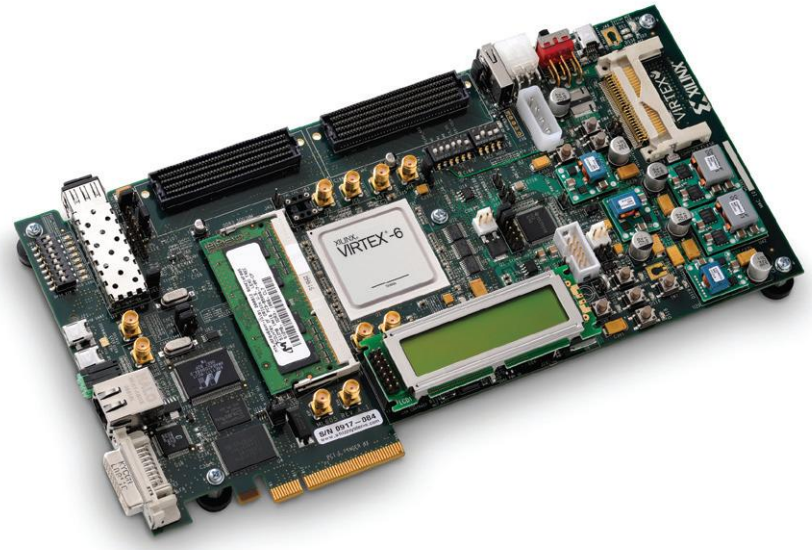
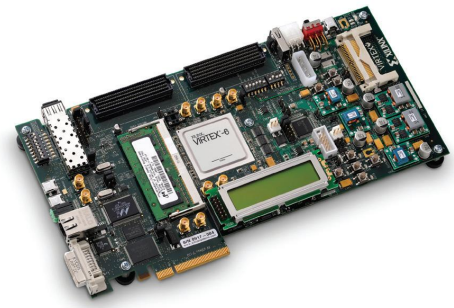


Figure 3.30: Xilinx Virtex®-6 FPGA Evaluation Kit

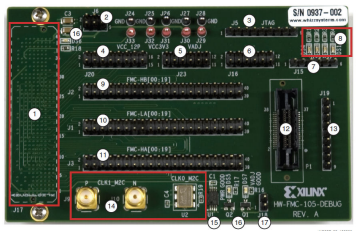
- Two or more general purpose timers TIMl_1 TIMl_2 ... TIMl_x for timing intent. The general purpose timers can be used to trigger peripherals such as the analog to digital converter trigger

- ASK demodulator, implemented as an analog watchdog with rising and falling edge detection. The ASK demodulator implemented in hardware allows the system to detect edges on the power carrier and trigger the demodulation of the stream when needed

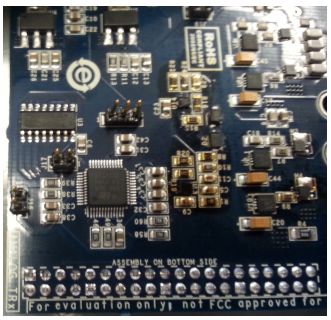
One important peripherals that is missed on the FPGA evaluation kit is the analog to digital converter as the Virtex®-6 FPGA can only work with signals in the digital domain. Moreover, the power section containing the required power MOSFETs used as inverter (in transmitter mode) and rectifier (in receiver mode) has to be placed externally. That said, an external board containing both the analog to digital converter and the power section block has been developed in order to add this feature to the FPGA platform.



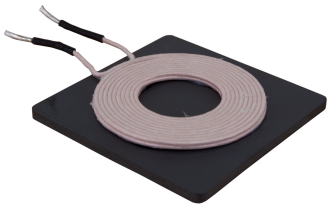
(a) Xilinx Virtex®-6 FPGA Evaluation Kit



(b) Port expansion for Xilinx Virtex®-6 evaluation kit



(c) Analog board with ADC (left half of PCB) and power inverter (right half of PCB)



(d) Wurth Electronics760308111 transmitter coil

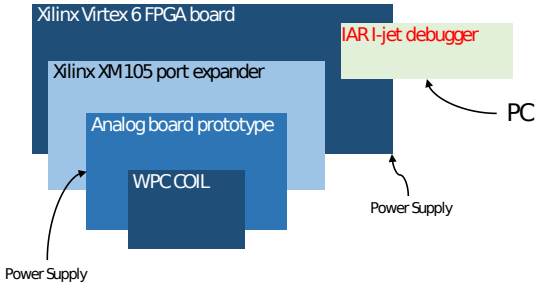
Figure 3.31: Boards used to emulate a ASIC system before starting with the silicon production. The setup is composed by a FPGA evaluation kit, a port expander to increase the number of FPGA I/O, an analog board with analog and power front-end and a power transmitter coil.

The emulation of the ASIC has been done with the following boards:

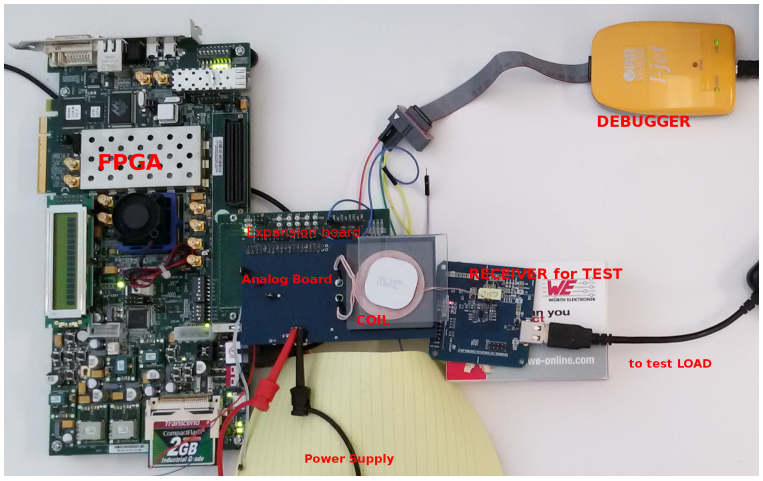
- The Xilinx Virtex®-6 evaluation kit, depicted in Figure 3.31a. The evaluation kit has also two expansion ports which allows the possibility to increase the number of digital I/O
- The Xilinx FMC XM105 Debug Card as in Figure 3.31b. Since at least 10 ports are dedicated to route the parallel signals of the external analog-to-digital converter, 4 ports are related to bridge driver control, one to enable the inverter, and other ports are used to control the analog-to-digital conversion phases, this port expander becomes mandatory to route all the digital signals to the FPGA

- The analog board of Figure 3.31c is in turn connected to the expansion board and exhibits only digital signals routed to the FPGA. This analog board has been designed and prototype in STMicroelectronics and contains the analog and power front-end of the FPGA.
- Wurth Electronics 760308111, Qi-certified wireless power transmitter coil, as depicted in Figure 3.31d

The electronics boards described above are connected one on top of each other, as illustrated in Figures 3.32a and 3.32b. The FPGA board, that is the Xilinx Virtex®-6 evaluation kit, is also connected to a IAR I-jet serial wire debugger.



(a) Board connection simplified blocks



(b) Photo of the connected boards, with a power receiver used for tests

Figure 3.32: Board connection structure. The WPC Coil is connected to the analog board (that contains the power inverter section), in turn connected to the Xilinx XM105 that expands the FPGA Virtex 6 board. The FPGA emulates an ARM® Cortex®-M4 CPU whose code can be debugged with a standard serial wire debugger (SWD) interface

3.4.2.1 Analog board development

As mentioned above, the analog front-end and the inverter/rectifier power section have been placed on a ad-hoc board, connected to the FPGA port extension board.

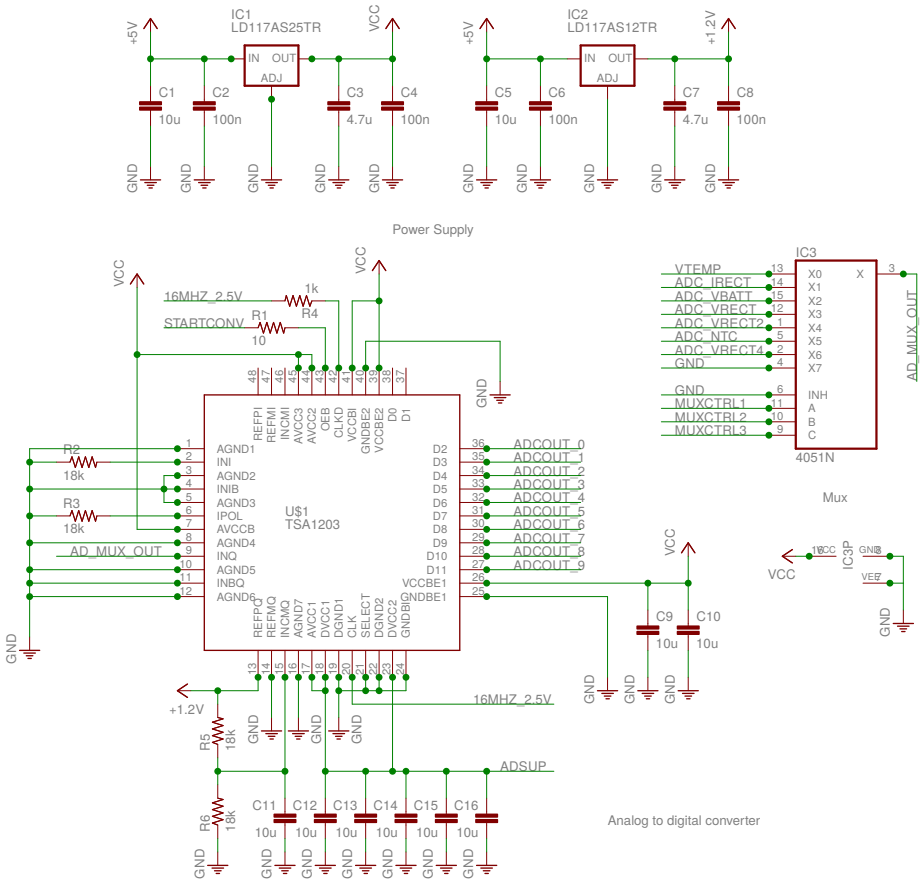


Figure 3.33: FPGA's analog to digital external front end with dedicated analog power supply

Depicted in Figure 3.33 is the schematics related to the analog front-end, made of:

- Two low drop fixed positive voltage regulator. The IC1 voltage regulator generate the 2.5 V voltage used to supply the analog to digital converter, the multiplexer IC3, the operational amplifier U13 and the bridge drivers of Figure 3.34. The IC2 regulator generated the 1.2 V reference voltage for the analog to digital converter.

- Analog to digital converter TSA1203. The TSA1203 emulated the silicon ADC, but only 10 of the 12 available bits are used, since the final chip will have a 10 bit ADC only.

- An 8 input multiplexer 4051N, to emulate multiple channel ADC

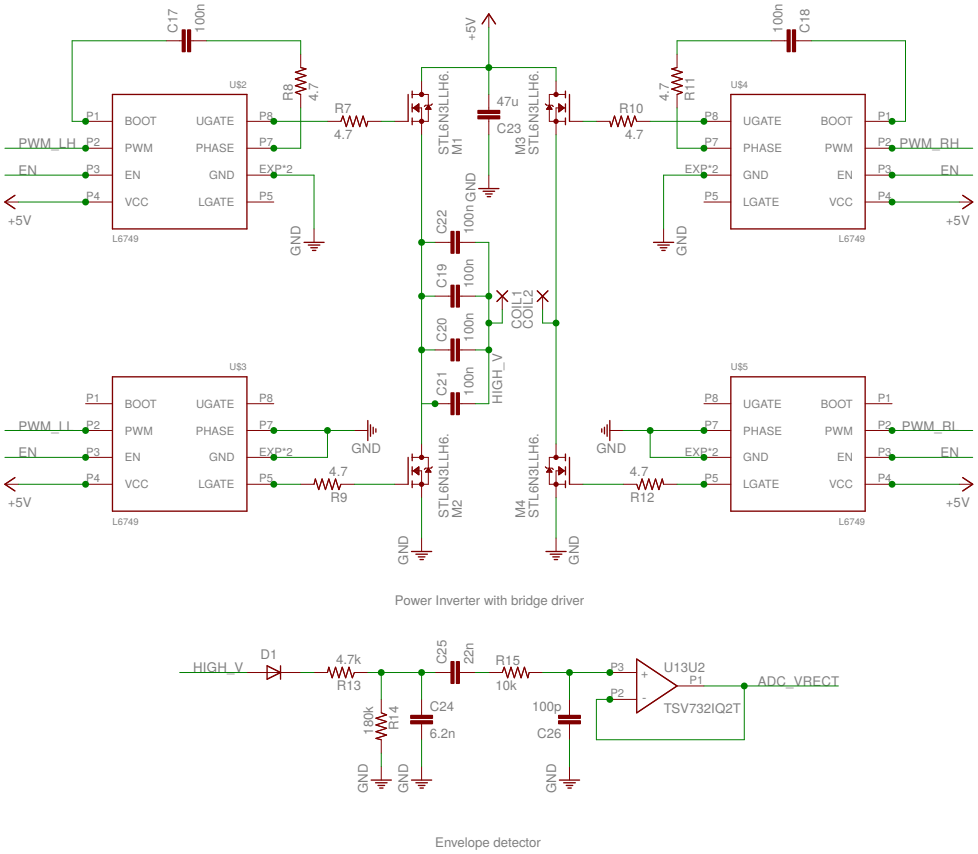


Figure 3.34: Power inverter / Active rectifier with high current bridge driver and envelope peak detector with voltage buffer

The power inverter section is instead depicted in Figure 3.34. It includes:

- Four high current bridge drivers, each of them controlled by an independent PWM clock. The PWM clocks are provided independently, so is possible to adjust frequency, duty cycle and dead-time in real time.

- Four 6 A drain current, n-channel power MOSFETs with low on-resistance $R_{DS(ON)}$ (typical 21 mΩ as reported on the datasheet of STL6N3LLH6 [STM12]) in full-H bridge topology.

- Envelope detector with low-pass filters and a high-pass filter. Low-pass filters are tuned to have frequency response as depicted in Figure 3.40.

3.4.2.2 FPGA firmware development

The firmware that runs on the FPGA evaluation kit is an adapted revision of the STM32L1 wireless power transmitter described on Section 3.1 where only the low-level library interfacing with the peripherals has been modified. The Qi-Standard state machine is exactly the same. The working frequency is different because the inverter topology is full-H instead of the half-H of the STM32L1 wireless power transmitter.

To develop the firmware on the FPGA, the IAR Embedded Workbench Integrated Development Environment (IDE) has been used. The compiler and the debugger of the IAR Embedded Workbench interface with the FPGA through a serial wire debugger (SWD) connector and, from the debugger point of view, the FPGA is seen as a standard Cortex®-M4 microcontroller.

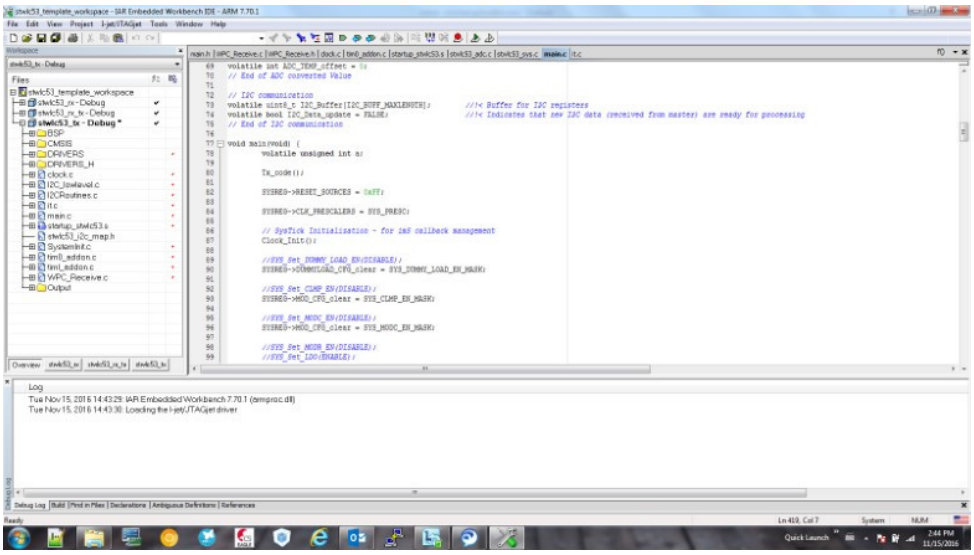


Figure 3.35: IAR Embedded Workbench IDE. The IAR is the IDE used to develop the firmware for both the FPGA system and the ASIC

From the hardware point of view the difference between the standard microcontroller based wireless power transmitter and the FPGA/ASIC version is the embedded ASK demodulator block, obtained by means of an analog watchdog. The analog watchdog connected after the ADC allows the envelope on power carrier to trigger a rising/falling edge so, the digital filter used in the STM32L1 version is no longer needed.

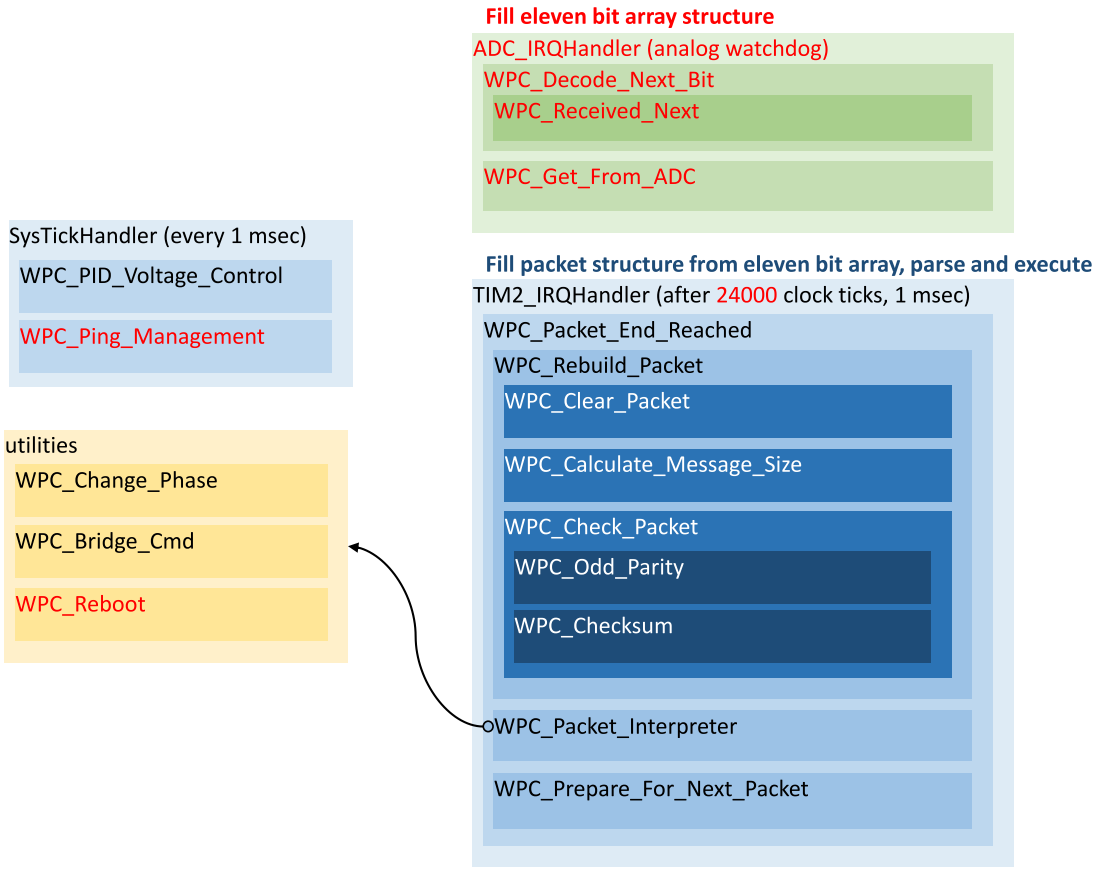


Figure 3.36: Modified firmware structure. The figure depicts the function call structure as in Figure 3.11. The difference between the STM32L1 wireless power transmitter and the FPGA/ASIC version are highlighted in red.

The analog watchdog on the FPGA/ASIC is a hardware peripheral which does not need the CPU to work properly. It can be configured on one ADC channel and it can automatically decode messages modulated on the power carrier, releasing the CPU load significantly.

3.4.3 STWLC53 wireless power transmitter / receiver

In this section the ASIC derived from the FPGA system development will be illustrated. The ASIC, named STWLC53, embed both wireless power receiver and transmitter functionality. The wireless power receiver functionality is available out-of-the-box since the receiver code is programmed on the internal ROM memory, while the transmitter functionality can be enabled by loading, through I2C bus, a specific firmware into the RAM memory and rebooting the device to run the code from RAM. The simplified block diagram of the STWLC53 chip acting as a wireless power transmitter or receiver is depicted in Figure 3.37.

The STWLC53 embeds hardware blocks for both acting as a power transmitter and power receiver. It is possible to enable or disable specific blocks accordingly to the need.

Figure 3.45b depicts the simplified block diagram while acting as a transmitter on the contrary Figure 3.45a depicts the system while acting as a receiver. In both Figure 3.45b and 3.45a the used blocks have been highlighted in red, whereas the unused one are in black. In block diagram of the system while acting both as a power transmitter and power receiver, the energy path has been depicted with green arrows.

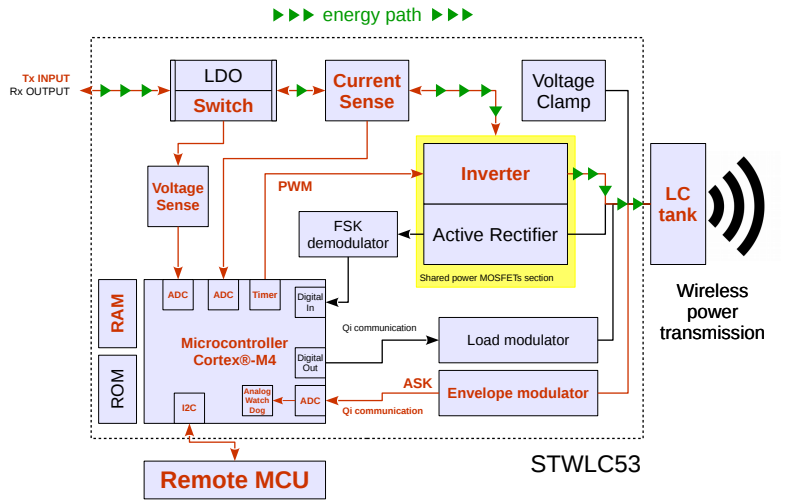
3.4.3.1 Transmitter mode

The STWLC53 chip while acting as a transmitter mode takes the DC power supply from the LDO/Switch pin. In this state, the LDO is switched off and the blocks act as a short-circuit with a low impedance switch. The DC current pass through the current sense and supply directly the MOSFET full-H bridge that, in this case is acting as an inverter controlled by a PWM provided by the microcontroller's timer. As long as the chip is in power transmitter mode, both the current and voltage sense circuits are enabled in order to monitor the input power supply thus imposing a limit in the overall input wattage.

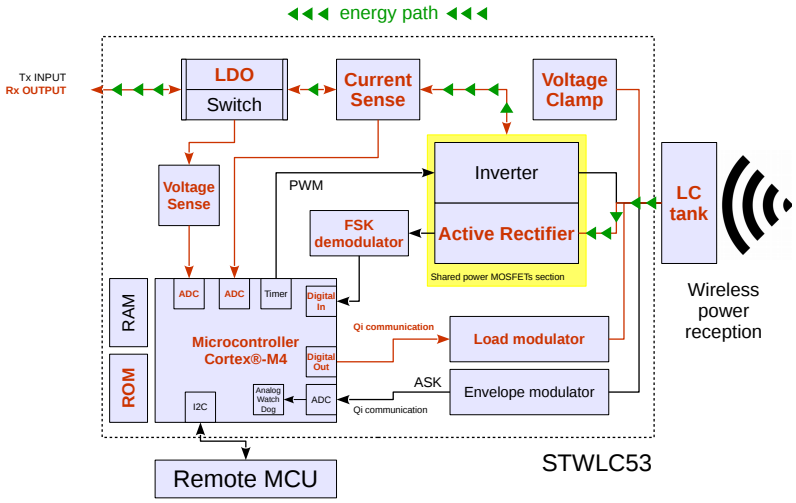
As stated by the Qi-specification [Con], it is mandatory to implement, in a wireless power transmitter, the communication unit. The communication units implemented into the STWLC53 chip is an envelope detector able to decode the information modulated on the power carrier by power receivers. The envelope detector works in combination with the microcontroller's ADC and the analog watchdog peripheral.

As per today, the firmware for the STWLC53 in transmitter mode is an on-going development and the code has to be uploaded on RAM to be executed. The upload of the

firmware can be performed through the I2C BUS or the SWD debugger interface.



(a) STWLC53 acting as a transmitter



(b) STWLC53 acting as a receiver

Figure 3.37: STWLC53 working modes. In red are depicted the enabled blocks. The green arrows show the energy path from/to the coil to/from the DC supply

3.4.3.2 Receiver mode

To act as a Qi-compliant wireless power receiver, the STWLC53 chip rectify the alternating electromagnetic field by means of the full-H bridge working as an active rectifier. The rectified current pass through a current sense and reach a low-drop out (LDO) voltage

regulator. The voltage regulator is used to provide a stable DC power supply on the output. As shown in Figure 3.45a both current and voltage sensor blocks are active exactly as the transmitter mode. The voltage clamp block is switched on for safety reason in order to protect the active rectifier in case of overvoltage during the disconnection of heavy loads.

The communication unit in power receiver mode is enabled and is is controlled by means of a digital output from the microcontroller.

Lastly, as shown in Figure 3.45a, the firmware running while in receiver mode is stored into the ROM and it is permanently stored on embedded memory.

Blocks	Used in TX	Used in Rx	Note
LDO/Switch	Yes (Switch)	Yes (LDO)	
Current sense	Yes	Yes	
Voltage sense	Yes	Yes	
FSK demod	No	Yes	
Envelop demod	Yes	No	
Load mod	No	Yes	
Inverter/Rectifier	Yes (Inverter)	Yes (Rectifier)	Shared full bridge
Voltage Clamp	No	Yes	
ROM	No	Yes	
RAM	Yes	Yes	
LC tank	Yes (to transmit)	Yes (to receive)	

Table 3.3: Blocks in the STWLC53 chip

3.4.4 Schematics of the STWLC53 evaluation board

To test the STWLC53 sample engineering chip, an evaluation board with a minimum set of passives components has been designed and prototyped in STMicroelectronics, as shown in Figure 3.38. In this section only the power transmitter functionality of the STWLC53 chip will be illustrated and explained since only the transmitter firmware was developed for this thesis.

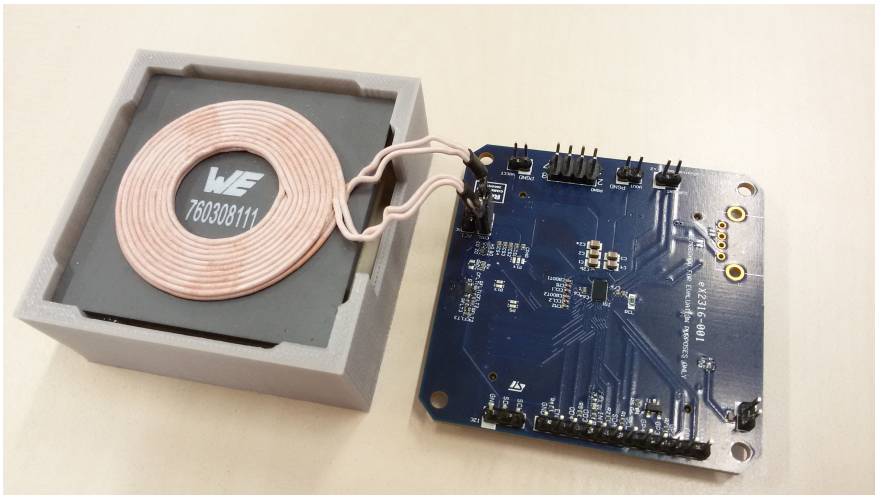


Figure 3.38: STWLC53 evaluation board with a power transmitter coil (Wurth Electronics 760308111)

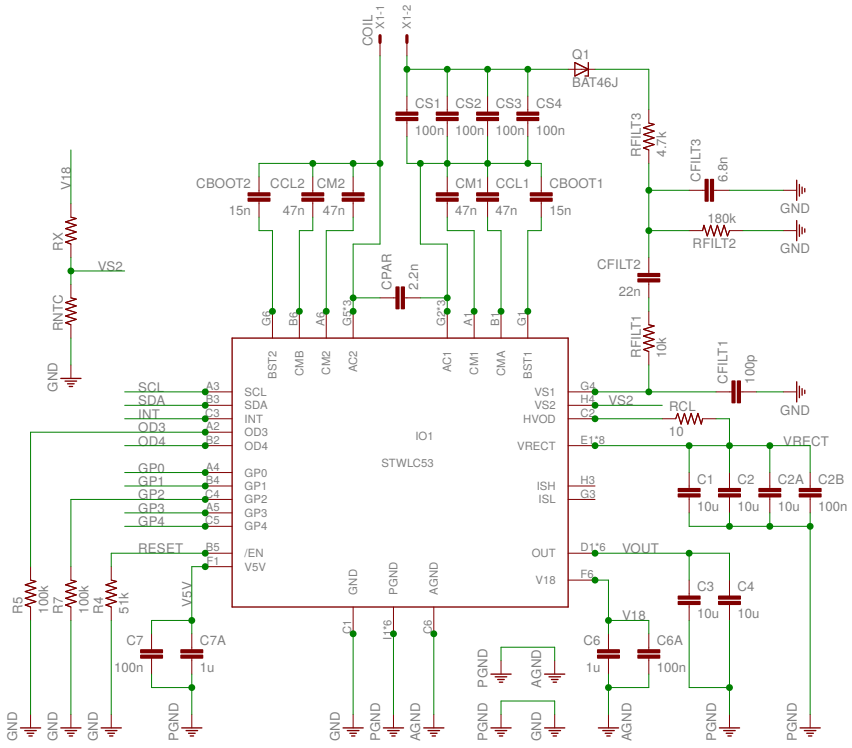


Figure 3.39: Schematics of the STWLC53 evaluation board

3.4.5 Communication Unit

The power carrier envelope detector implemented in the STWLC53 chip has an internal dedicated ASK demodulator, and the operating principle will be illustrated below.

The STWLC53 chip has been designed to minimize external active components thus a simple envelope detector with only passives is required to robustly extract the modulated signal of a power receiver. Figure 3.40 depicts the simple schematics of the external signal conditioning filter that is a two-poles low-pass filter with DC decoupling.

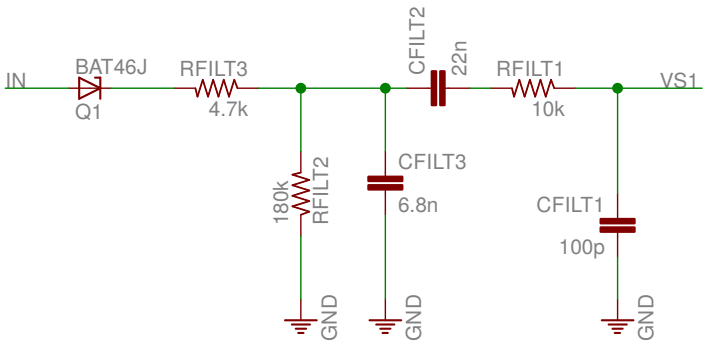


Figure 3.40: External envelope detector

The frequency response of the filter depicted in Figure 3.39 and Figure 3.40 is shown in the Bode diagram of Figure 3.41. The envelope detector is made by:

1. A high voltage, fast recovery Schottky diode Q1, used to remove the negative AC signal

2. A RC low-pass filter made by RFILT3 and CFILT3 tuned at 73 kHz

3. A decoupling capacitor CFILT2 to remove the DC voltage

4. A RC low-pass filter tuned at 2.3 kHz made with RFILT1 and CFILT1

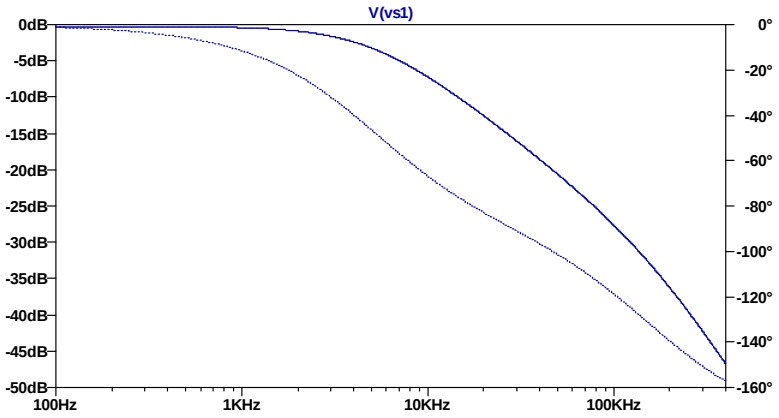


Figure 3.41: Frequency response of the envelope filter on VS1 input pin of the STWLC53 chip. In solid blue line the magnitude while dotted line is the phase response of the demodulator filter

Inside the STWLC53 chip, connected to the VS1 pin, the filtered signal is further conditioned, as depicted in the block diagram of Figure 3.42:

- A DC voltage of 0.72 V is added on the signal, in order to have a fixed, known, steady state
- The signal is clamped between 0 V and 1.8 V to protect the Analog to Digital converter input
- The signal is amplified by a factor of *0.5, 1, 2 or 3* and than it is sampled by a 10 bit ADC

3.4.5.1 Analog watchdog

The analog watchdog is a peripheral which has been embedded into the ASIC in order to significantly reduce the computational load caused by the presence of digital filter used in the wireless power transmitter module of Section 3.1 and in the evaluation kit described in Section 3.2. In the power transmitters previously designed, the digital filter takes as input the ADC converted value of the power carrier, with a sampling rate equivalent to one quarter of the switching frequency. This means, every four PWM cycles the digital filter has to be executed by the CPU.

In the STWLC53 chip an analog watchdog has been embedded in order to reduce the computational effort of the CPU and at the same time, to increase the noise suppression by means of PWM-synchronized analog to digital conversion. The PWM-synchronous analog watchdog has been configured in this way:

1. The ADC conversion is triggered by the PWM frequency; the sampling is synchronized with the PWM signal reducing the noise caused by the switching activity of power MOSFETs.

2. The ADC output is connected to the analog watchdog that is configured to trigger an interrupt in two cases:

   (a) the ADC converted value goes lower than the low threshold with a falling edge

   (b) the ADC converted value goes higher than the high threshold with a rising edge

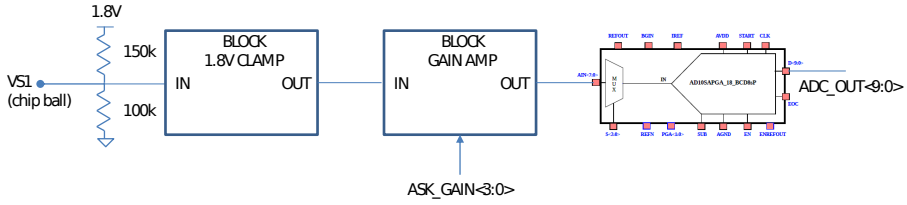


Figure 3.42: STWLC53 internal ASK demodulation front end, simplified block diagram

$$Clamp \begin{cases} OUT = 1.8V & if \quad IN > 1.8V \\ OUT = IN & if \quad 0 < IN < 1.8V \\ OUT = 0V & if \quad IN < 0V \end{cases} \tag{3.1}$$

$$Gain \begin{cases} OUT = IN * 3 & if \quad ASKGAIN(3) = 1 \\ OUT = IN * 2 & if \quad ASKGAIN(2) = 1 \\ OUT = IN * 1 & if \quad ASKGAIN(1) = 1 \\ OUT = IN * 0.5 & if \quad ASKGAIN(0) = 1 \end{cases} \tag{3.2}$$

3.4.6 Firmware

Firmware that has been embedded into the ASIC is very similar to the FPGA one with differences related to peripherals such the ADC. In the STWLC53 ASIC the embedded peripherals such as the ADC, demodulators, sensing circuits and PWM timers are different and the low level drivers interfacing with the Qi-specification protocol library has been customized.

The Qi library however is the same of the middleware depicted in Figure 3.15.

3.4.7 Characterization in transmission mode

3.4.7.1 Thermal performance

The STWLC53 chip has been characterized in temperature, measuring the maximum value achieved while transmitting the maximum power of 7.8 W. As depicted in Figure 3.43 the maximum temperature on the board is generated inside the STWLC53 chip by the power inverter MOSFETs. At room temperature of 24°C, the chip maintain a safety temperature of less than 40°C.

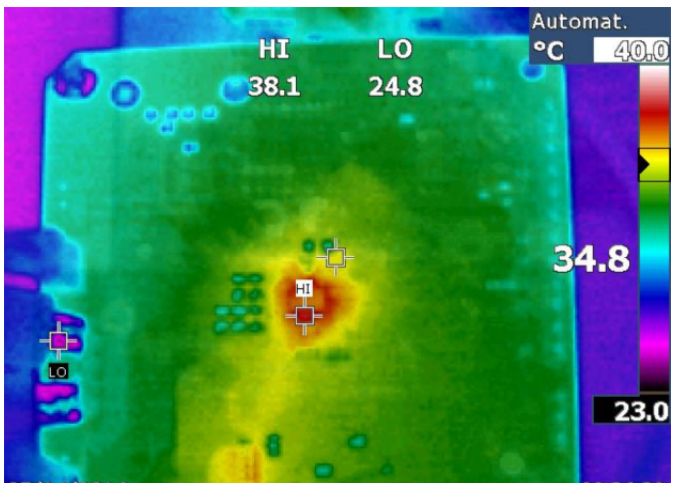


Figure 3.43: Thermal photography of the evaluation board while transmitting 1.3 A @ 6 V power supply (7.8 W). The temperature in the center, where is soldered the STWLC53 chip is lower than 40°C.

3.4.7.2 Efficiency

Preliminary measurements has been performed on the STWLC53 wireless power charger chip.

As shown in Figure 3.44 the overall efficiency of the system in receiver mode is higher than 80%, compared to an efficiency lower than 60% while in transmitting mode. The difference of the results could be due because of the different setup in the measurements:

1. STWLC53 as a receiver and Samsung PN920 as a transmitter has been used to measure the efficiency while the ASIC act as a receiver

2. STWLC53 both as power receiver and transmitter has been used to measure the efficiency of the ASIC while in transmitter mode

Moreover, the higher efficiency of the ASIC while acting as a receiver compared while acting as a transmitter could be due to the greater maturity of the firmware. The firmware while in transmitter mode is a porting of the firmware illustrated in Figure 3.11 and needs some fine tuning on the ASIC due to the completely different hardware. Furthermore, the measurements depicted in Figure 3.44 have been performed using the same coil, which is designed as a receiver. Receiver coils are not optimized to be used as a transmitter and this would explain the lower efficiency while acting as a transmitter with a receiver coil.

Nevertheless the efficiency difference, a great result has been achieved with this device, proving that is possible to have a single ASIC acting both as a power receiver and power transmitter as described in the patent pending application shown in Section 3.4.

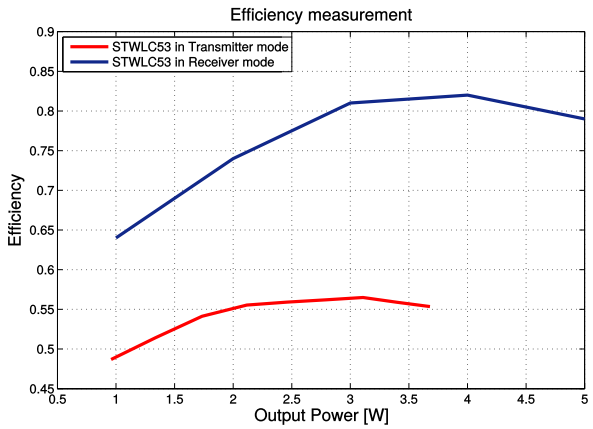


Figure 3.44: Efficiency measurement in Transmitter and Receiver mode

3.5 Conclusions

This chapter has treated the design and prototype of both wireless power transmitters and receivers. The unique design is base on standard microcontrollers and discrete components available on the market. A full microcontroller independent library written in ANSI-C code has been developed and designed to be easily integrated on the CubeMX hardware abstraction layer (HAL) provided by ST for its microcontrollers. The portability of the source code ensure a very simple porting between different microcontroller families.

As proof of portability of the developed library, this chapter treated the design of two wireless power transmitters in Section 3.1, one module made with a STM32L1 ultra low-power microcontroller and one evaluation kit made with an STM32F0 entry-evel micro-controller. The libraries running the Qi-specification are exactly the same and they use the HAL library available for the specific microcontroller (STM32L1 and STM32F0 respectively) to interface with the peripherals.

(a) STWLC53 acting as a receiver (b) STWLC53 acting as a transmitter

Figure 3.45: Concept of the patent-pending "*PowerShare*"

A design and develop of a wireless power receiver has been also illustrated in Section 3.3. The designed wireless power receiver is Qi-specification compatible and it is realized with discrete components available on the market too. In this design, an 8 bit ultra low-power microcontroller has been used and a specific library has been implemented. In this case, the wireless Power Receiver library use the standard peripherals library of this specific microcontroller but it is fairly portable on other platforms with different microcon-

troller.

The chapter ends with a design of a wireless power transmitter / receiver system made with an innovative ASIC. The design aims to join the design of wireless power receivers and transmitters in a single chip and it is, up to now, the unique chip available on the market to act both functionality. This ASIC, based on a patent-pending application, will bring the concept of "*PowerShare*" to the mass market.

The idea to turn a wireless power receiver into a wireless transmitter will become useful due to the spreading of hundreds of wearable devices such as smartwatches, activity trackers and so on. Wearable devices will be easily recharged using the wireless power charger chip embedded into smartphones. In this scenario, a smartphone can be recharged using conventional Qi-compliant wireless power transmitter, as in Figure 3.45a and according to requirements, the power *receiver* can wirelessly *transmit* power to the wearable device and charge it, as exemplified in Figure 3.45b. The library which turn the STWLC53 power receiver into a power transmitter is the same implemented into the wireless power transmitter treated in Section 3.1, with minor modifications.

3.5.1 Demonstration

The *PowerShare* concept illustrated in Figure 3.45 has been realized with the STWLC53 chip, and Figure 3.46 depicts a fully working demonstration of the initial concept.

The demonstration shows that a standard wireless power charger based on the Qi specification can recharge a smartphone which embeds the STWLC53 ASIC, as depicted in Figures 3.46a and 3.46b. When the mobile phone's battery has been recharged, its wireless power receiver can be switched into transmitter mode, as shown in Figure 3.46c, and starting from now the smartphone acts as a standard wireless power transmitter using exactly the same hardware configuration and the same coil. Finally Figure 3.46d shows the smartphone that is charging a smartwatch which has embedded the wireless battery recharge.

(a) Standard wireless power transmitter

(b) Charging the smartphone as usual

(c) Switching from receiver mode into transmitter mode

(d) Charging wirelessly a smartwatch with the smartphone

Figure 3.46: A fully working demonstration of the *PowerShare* concept

Conclusion

This thesis work, in the second chapter, the design, manufacturing and characterization of a wireless motion sensor platform for the Internet of Things (IoT) context has been discussed and treated. The resulting platform, named *SensorTile*, is a small PCB board with inertial, geomagnetic and audio sensors, low power processing capability and radio connectivity. The design and realization of the *SensorTile* platform has been driven by customers working in the IoT market and want a ready to use development platform in a small, wearable, form factor. Several use cases, covering some common requirements have been developed as examples. Characterization of the developed platform have been performed both for performance measurement and certification purpose.

The third chapter has been focused on the design of wireless power charger platforms. The chapter began with the design of two wireless power transmitters compatibles with the WPC's Qi specification. The final design of wireless power transmitter platforms have been based on standard microcontrollers and the developed firmware is very easily to maintain and debug. The firmware structure uses the hardware abstraction layer and has been designed to simplify the porting of the code on different microcontrollers.

In this chapter, the design of a wireless power receiver has been also presented. The receiver platform has been designed as a standalone module in small form factor and the PCB size measures only 13 mm x 13 mm. The designed power receiver comply with the Qi specification and supports an output power up to 5 W. The firmware, developed on an 8 bit microcontroller, maintain the flexibility and the possibility to port it on several different architectures, based on microcontrollers.

The third chapter concludes with the description of the design of a new silicon device, based on a U.S. patent pending application by M. Galizzi and A. Vitali. The silicon device, developed in STMicroelectronics, combines the functionality of wireless power transmitters and receivers and allows customers to easily develop wireless power charger devices

with bidirectional capability. With this new device, a standard wireless power receiver (for example, a smartphone) which can be charged wirelessly as usual, can switch into transmitter mode allowing the device to share its energy (for example, to wirelessly recharge *smartwatch*es). The development of this silicon involved different working groups in STMicroelectronics, with the hardware development based in Catania (Italy), the receiver firmware development performed in Prague (Czech Republic) and the development of the power transmitter firmware mainly developed in Santa Clara (California).

The next step on STWLC53 will be related to firmware customization for mass production. The same silicon will be renamed STWLC33 and some minor modifications to the wireless power transmitter firmware will be carried out. Source code optimization and compiled code size reduction is still an ongoing activity performed in order to fit additional features in the final firmware release.

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