UNIVERSITY OF BERGAMO

Doctoral Degree in Engineering and Applied Sciences

XXX Cycle

SSD: ING-INF/01 Electronics

Design and Test of Imaging and Particle Detection Microelectronic System for Frontier Research Applications

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Doctoral Thesis

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Academic Year 2016 / 2017

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Introduction

Over the last decades, the use of CMOS integrated circuits has largely diffused in many different fields and, in particular, in the readout of radiation detectors. Among the advantages of an integrated CMOS technology, high integration density, capability of handling large data rates, small form factor and last but not least, high radiation resistance are crucial to meet the demanding specifications of modern physics experiments using high granularity detectors.

In a well studied realization of an analog readout channel for a radiation detector, three foundamentals steps are needed:

- characterization of the CMOS nanoscale technology that will be adopted to design the analog channel;
- desing and simulation of the circuit;
- characterization and validation of the final chip.

Nanoscale CMOS technology are provided with detailed models capable of perfectly describing the behavior of the transistors for digital applications. Models describing transistors characteristics for analog applications can be not so accurate as far as noise and radiation effects are concerned. In particular noise characteristics, and above all flicker noise, are stongly dependent on the technology, thus an in-depth characterization is needed. Moreover, normally, there are no information regarding the radiation hardness of the technology, thus a detailed analysis at the expected radiation doseis needed depending on the scope of the electronic readout.

Once these peculiar aspects of the chosen technology are defined and analyzed, it is possible to move forward to the second step: design and simulate the circuit meeting the specifications required from the application.

Last but not least, there is the characterization and the validation of the final chip. This step has the goal of verifying the correct functioning of the system. Such phase could also highlight some problems of the designed circuits that ideal simulation did not point out, so that the designers will be able to cope such with defects in the following production steps.

Usually, chip development is not carried out only by one work group, but with a collaboration of different Universities and Institutions. In this thesis, all these steps were taken into account for three different projects: RD53, GAPS and DSSC. All these 3 projects require the design and test of custom integrated circuit for the readout of silicon pixel or strip detectors, with avdanced analog signal processing features providing a low noise performance. Additional requirements such as radiation hardness may depending on the application, as discussed in the following chapters.

In particular, the first Chapter provides an extensive analysis of total dose effects in devices belonging to a commercial 65 nm and 110 nm CMOS process, in the context of designing rad-hard analog integrated circuits for front-end applications in future colliders. This activity has been carried out in the framework of the RD53 collaboration. The aim of this project is to design the next generation of hybrid pixel readout chips for the silicon vertex inner tracker of the ATLAS and CMS detectors of the Lrge Hadron collider (LHC) at CERN facility.

The second Chapter concerns the design of the analog reading channel of a novel cosmic antideuteron detector. This work is carried out for the GAPS project that has the aim to realize a novel approach for indirect dark matter searches. NASA approved GAPS's proposal in September 2016. GAPS experiments is the result of the collaboration of different Universities and Institutes, e.g. MIT, UCLA, INFN and others. The balloon launch is expected by the end of year 2020 from the McMurdo station in Antarctica.

The third Chapter regards the characterization of silicon pixel detectors for DSSC project at European XFEL. The last part of this thesis presents the characterization of the readout ASIC functionality and the backside current of the first and second prototype of the bare modules of such project.

1 Radiation hardness of nanoscale CMOS technologies

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In the Microelectronics field, the rapid evolution of technological scaling has allowed for an uninterrupted increase in the performance and complexity of analog and digital integrated circuits. The very high integration density allows CMOS technology to have a very large diffusion in analog and digital circuits in different fields, including detectors signal processing. Nevertheless, due to this uninterrupted evolution, continuous analysis is needed to evaluate static and noise characteristics, in order to classify pros and cons of the technology in study.

Thanks to the *technology scaling* phenomenon, a reduced channel length L and a

thinner gate oxide t_{ox} are obtained. It is possible to take advantage of these properties in applications where rad-hard integrated CMOS circuits (IC) are required, such as in High Energy Physics (HEP), space radiation detectors and medical imaging detectors. Nowadays several HEP experiments such as ALICE, CMS and ATLAS have their frontend electronics designed in 250 nm technology and their upgrades are going to be designed in more scaled process. As an example, in next generation detectors, such as CMS phase 2, the frontend electronics of the inner tracker will be designed entirely in a 65 nm CMOS technology in order to achieve better results in terms of spacial resolution.

The aim of this chapter is to quantify how much the investigated devices are able to withstand the ionizing radiation levels expected in experiments such as CMS at High Luminosity LHC, X-ray imaging and space radiation detectors, where electronic chips will be exposed to very high doses, from a few Mrad up to 1 Grad of Total Integrated Dose. Great attention was focused on the study of the characteristics of components in the noise voltage spectrum (white and 1/f noise) which are usually of great importance in amplifying and filtering stages, thus they were examined in depth. In addition, other fundamental parameters such as the transconductance g_m and the threshold voltage V_{Th} were evaluated as well. This work is concentrated on applications in which power dissipation is critical, therefore, in order to satisfy this requirement, MOSFETs in the analog section of the processing chain have to be biased in the low current density range (from a few µA to a few hundreds of µA).

1.1 Noise Sources

Electronic noise is the result of spontaneous fluctuations occurring in some active and passive circuit components appearing as voltage or current variations whose temporal evolution is governed by statistical laws. Noise is a time-continuous stochastic process caused by some fundamental physical phenomena, such as thermal excitation of charge carriers in conductors or the granular structure of the electric charge. Electronic noise should not be confused with enviroment interferences (i.e. power supplies fluctuation, electromagnetic induction, etc...). Such interferences, ideally, can be removed by filtering techniques and shielding, wherease stochastic noise cannot be removed because it is directly linked to the operating principles of devices and circuit components. The study of noise characteristics in electronic circuits is important because noise limits the precision of the measurement of a signal. Since noise is a purely random phenomenon, the value of its waveform cannot be predicted for any time. As a consequence, noise variables are described quantitatively by the

mean square value (or the square root of the mean square value) and, in frequency domain, by their noise spectral density.

1.1.1 Spectral Power Density

The mean square value is associated with the concept of spectral power density that is valid under the hypothesis of *stationarity* and *ergodicity*:

- *Stationarity*: a process is stationary when its statistical properties (mean value, average quadratic value, etc ...) are invariant over time.

- *Ergodicity*: a stochastic process is called ergodic when the output waveform can be considered representative of the system.

Supposing that the noise is represented by a function $x(t)$ (see Figure 1.1) and considering that $x(t)$ in the range $[-T, T]$ can be represented by the following expression:

$$\begin{cases} x_T(t) = x(t) & \text{for } t < |T| \\ x_T(t) = 0 & \text{for } t > |T| \end{cases} \tag{1.1}$$

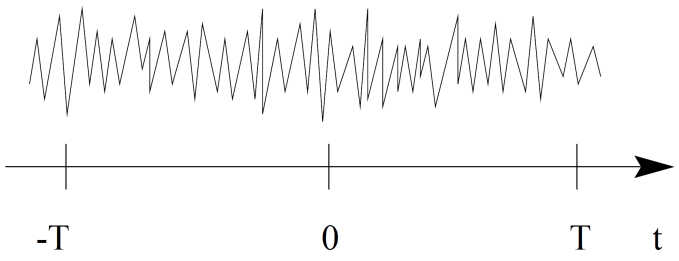


Figure 1.1: Noise waveform.

the mean square value of the limited $x(t)$ is:

$$\overline{x_T^2(t)} = \frac{1}{2T} \int_{-T}^{T} x_T^2(t) dt \tag{1.2}$$

and expressing it as its inverse Fourier transform it is possible to obtain:

$$\begin{aligned}\overline{x_T^2(t)} &= \frac{1}{2T}\int_{-T}^{T} x_T \frac{1}{2\pi}\int_{-\infty}^{\infty} V_T(\omega)e^{j\omega t}d\omega dt \\ &= \frac{1}{2T}\int_{-\infty}^{\infty} V_T(\omega)\frac{1}{2\pi}\int_{-T}^{T} x_T e^{j\omega t}dtd\omega \\ &= \int_{-\infty}^{\infty}\frac{V_T(\omega)^2}{2T}df \end{aligned} \tag{1.3}$$

where:

$$V_T(\omega) = \int_{-T}^{+T} x_T(t)e^{-j\omega t}df \tag{1.4}$$

and due to the fact that $x_T(t)$ is real: $V_T(-\omega) = V_T^*(\omega)$. For $T \to \infty$ it is possible obtain the mean square value of $x(t)$:

$$\overline{x_T^2(t)} = \int_{-\infty}^{\infty}\lim_{T\to+\infty}\frac{V_T(\omega)^2}{2T}df \tag{1.5}$$

Spectral Power Denisty of noise variable *x(t)* is the limit within the integral:

$$\frac{\overline{dx^2}}{df} = \lim_{T\to+\infty}\frac{V_T(\omega)^2}{2T} = S_x(\omega) \tag{1.6}$$

thus, knowing the power spectral density, the mean square value is:

$$\overline{x_T^2(t)} = \int_{-\infty}^{\infty} S_x(\omega)df \tag{1.7}$$

that represents the bilateral spectral density. In the following the unilateral spectral density is used.

1.1.2 Shot Noise

Shot noise is present in all devices when a relatively small number of charges have to cross a potential barrier. Shot noise can be represented by a current source whose power spectral density is:

$$\frac{\overline{di^2}}{df} = 2qI \tag{1.8}$$

where I is the device average current and q is the electron charge ($q = 1.6 \cdot 10^{-19}C$).

1.1.3 Thermal Noise

Random thermal electrons motion is the cause of *Thermal Noise*. It is independent of the presence of a direct current, whereas it depends on the temperature. Resistor thermal noise can be represented by a voltage source, according to the equivalent Thévénin circuit, with a power spectral density of:

$$\frac{\overline{de_R^2}}{df} = 4k_BTR \tag{1.9}$$

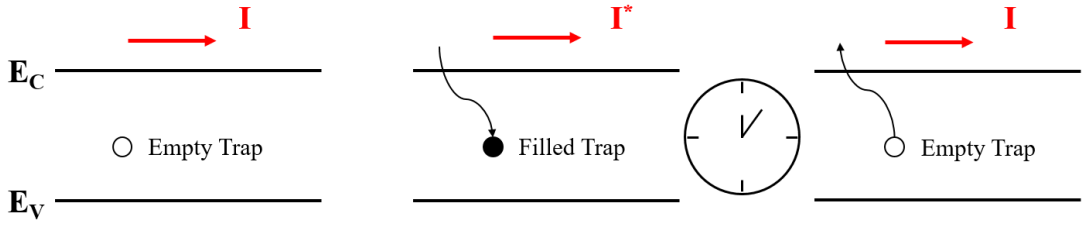
where k_B is the Boltzmann's constant ($k_B = 1.38 \cdot 10^{-23} J/K$) and T is the temperature. In alternative it can be represented by Norton equivalent circuit, with a current source with a noise spectrum density of:

$$\frac{\overline{di_R^2}}{df} = \frac{4K_BT}{R} \tag{1.10}$$

1.1.4 Flicker Noise

Flicker Noise is present in all active components and some discrete passive components such as carbon resistors. Flicker noise in the current of a semiconductor device is characterized by a power spectral density that is inversely proportional to frequency and for this reason is also known as "1/f noise". Such behaviour can be explained considering that there are a certain amount of donor/acceptor impurity atoms in the semiconductor whose energy level is more or less localized in the band gap. Although the trapping and emission process associated with these defects has little effect on static current behavior, noise is affected in the low frequency region. As one can see in Figure 1.2, a trapped charge will be released in an average time τ that depends on both the nature and the position of the trap. In Figure 1.2 I indicates the ideal channel current, if no trap are activated during the passage of the charges, q is the elementary charge, N_{TOT} is the total number of charge carriers, V_{BIAS} is the voltage bias, L is the channel length and I^* is the channel current if one trap is activated during the passage of the charge carriers. For a time τ, the current is varied by $\Delta I = {}^{I}/_{N_{TOT}}$. For frequency signals greater than $1/\tau$, no differences are noticeable, since the trap is always full or empty throughout the evolution of the signal. For signal frequencies lesser than $1/\tau$, effects are not negligible, in fact, the trap may act during the evolution of the signal.

As already mentioned each time the charge is trapped, the average stay time is τ. It is possible to modelize the phenomena as if a low frequency trapping filter handles the process. As a consequence, the noise voltage spectrum is expected to



$$I = qN_{TOT}\mu\frac{V_{BIAS}}{L^2} \qquad I^* = q(N_{TOT}-1)\mu\frac{V_{BIAS}}{L^2} \qquad I = qN_{TOT}\mu\frac{V_{BIAS}}{L^2}$$

Figure 1.2: Schematic of current fluctuations due to the trapping of charges.

be somewhat proportional to the square of such low pass filter transfer function $1/(1+(\omega\tau)^2)$. As a matter of fact, that is what one can observe. In particular, since all the impurity atoms should not be of the same species, τ will change both from one atom to another and with the temperature. The resulting noise is due to the overlapping of all these effects. The higher the number of impurities, the more the slope of the resulting noise becomes similar to 1/f (see Fig. 1.3).

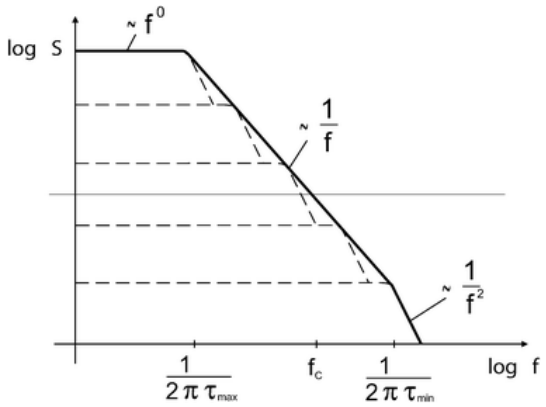


Figure 1.3: Schematic of current fluctuations due to the trapping of charges.

This situation is almost always verified for the traps present in the silicon dioxide, since in these cases τ depends also on the distance traveled by charged carriers in the oxide itself and a continuous distribution of values is assumed. Flicker noise is always associated with a current flux and has the following spectral density:

$$\frac{\overline{di_R^2}}{df} = k_1\frac{I^a}{f^b} \tag{1.11}$$

where I is the direct current, k_1 is a constant depending on the technology and dimensions of the device, a is a constant in the range $[0.5, 2]$ and b is a constant

approximately equal to 1. Flicker noise is different from other noise sources because it is not expressed by well-known physics constants like resistors or currents. k_1 is a not-known a-priori term and it may vary by several orders of magnitude from one technology to another and with different dimensions of the devices. For this reason, it is necessary to measure the power spectral density of the flicker noise.

1.1.5 MOSFET

The gate referred noise voltage spectrum of a MOSFET device $S_e^2(f)$ can be modeled by means of the following equation:

$$S_e^2(f) = S_W^2 + S_{1/f}^2(f) \tag{1.12}$$

The two terms of such equation will be discussed in what follows.

Channel Thermal Noise

The first term in (1.12) is determined by channel thermal noise and noise contributions from parasitic resistances (gate, bulk and source/drain resistance), which also exhibit thermal noise [1]. In the low current density operating region, the white noise voltage spectrum S_W^2 is dominated by channel thermal noise and can be expressed by means of the following equation:

$$S_W^2 = 4k_B T \alpha_W \frac{n\gamma}{g_m} \tag{1.13}$$

where T is the absolute temperature, $\alpha_W \geq 1$ is an excess noise factor, n is a coefficient proportional to the inverse of the subthreshold slope of I_D as a function of V_{GS} and γ is a coefficient ranging from 1/2 in weak inversion to 2/3 in strong inversion.

This coefficient can be calculated according to the following relationship for each I_D value:

$$\gamma = \frac{1}{1 + \frac{I_D L}{I_Z^* W}} \left[\frac{1}{2} + \frac{2}{3} \frac{I_D L}{I_Z^* W} \right]. \tag{1.14}$$

In equation (1.14) I_Z^* is a characteristic normalized drain current:

$$I_Z^* = 2\mu C_{OX} n V_T^2 \tag{1.15}$$

where μ is the channel mobility, C_{OX} is the effective gate capacitance per unit area and V_T=$k_B T/q$ is the thermal voltage. The thermal noise in the channel current

can also be expressed in terms of an equivalent resistance:

$$R_{eq} = \frac{S_W^2}{4k_BT} = \alpha_W \frac{n\gamma}{g_m} \tag{1.16}$$

Flicker Noise

The second term in (1.12) is determined by flicker noise and is characterized by a power spectral density that is inversely proportional to frequency. It can be modelized by the following relationship:

$$S_{1/f}^2(f) = \frac{K_f}{C_{OX}WL} \frac{1}{f^{\alpha_f}} \tag{1.17}$$

where K_f is an intrinsic process parameter, C_{OX} is the effective gate capacitance per unit area and the exponent α_f determines the slope of this low frequency noise term [1].

1.2 Radiation Effects on MOSFETs

The study of radiation effects on MOSFETs is very important because it provides essential informations to IC analog designers where rad-hard CMOS integrated circuits (IC) are required, such as in space, imaging and high energy physics detector applications. Interaction of radiation with matter can lead to three different types of effects:

- **Ionization (Total Ionizing Dose, TID)**: damage due to the increase of the trapped charge in SiO_2 structures. It occurs when the energy deposited by the passage of ionizing radiation creates electron-hole pairs within the oxide: holes are trapped inside the oxide region, because of their very low mobility, whereas electrons are swept away. Such phenomenon causes an increasing concentration of positive charge. This type of effect is mainly due to exposure to X-rays, γ-rays and most charged particles, however the effects depend mainly on the amount of energy deposited and not by the particular type of source.

- **Bulk Damage or Displacement**: it occurs when incident particles, along their trajectory inside the device, strike and bounce a silicon atom from the crystalline lattice of the substrate, altering its electrical properties. Displacement damage is caused especially by protons, neutrons and heavy ions.

- **Single Event Effects**: caused by the deposition of a large amount of charge, induced by the passage of a single highly ionizing particle (generally a heavy

ion) through an integrated circuit, causing the immediate malfunctioning of one or more transistors.

Bulk damage and *single event effects* have limited effects in CMOS analog circuits. For this reason, this thesis is focused on *Total Ionizing Dose* (TID) effects in view of the design of analog front-end circuits for silicon detectors.

1.2.1 Ionization Damage

An ionizing particle passing through the structure of a MOSFET deposits a certain amount of energy both in silicon and in silicon dioxide, ionizing the two materials and leaving along its path a column of electron-hole pairs, proportional to the energy released. A fraction of the pairs can recombine immediately after being generated, whereas the rest, due to the effect of the electric field of bias applied to the transistor, are separated before recombination and consequently start drifting. While the charges cross the silicon oxide layer between the gate and the substrate, the electrons maintain a high mobility, typically around $20\,\mathrm{cm^2V^{-1}s^{-1}}$, whereas the holes move slower, with a mobility from 5 to 12 orders of magnitude less than the one of the electrons. Once the holes are carried to a few nanometers from the Si/SiO_2 junction, they are highly likely to occupy the many trap states present in the region, created by imperfections in the reticular structure generated during silicon oxidation. As a result, a growing concentration of positive net charge close to the conductive channel of the MOSFET is created, which interferes with the behavior of the device. In modern CMOS technologies, the thickness of gate oxide is reduced to a few nanometers, so that the effects of trapped holes in the oxide have become almost negligible because holes are quickly removed by direct tunneling. On the contrary, external oxides have retained, in comparison, remarkable thicknesses, from 100 nm to 1 µm, and therefore have the potential to become areas of high accumulation of positive charge. Therefore, holes trapped in **shallow trench isolation (STI)** oxides became much more important. The basic structure of the MOSFET is generally surrounded by an area of silicon dioxide, which has the function of electrically isolating it from other components present in the same chip [2]. External insulation oxides undergo the same trapping phenomenon as for gate oxide with a radiation-induced progressive charge buildup as shown in Figure 1.4. If this occurs in an NMOS, the amount of positive charge in the insulating oxides can become large enough to attract a large number of electrons in the substrate and create a conductive channel linking the source and drain by circumventing the primary transistor, as highlighted in Figure 1.5. The new system formed by source, external channel and drain takes the name

of a *lateral parasitic transistor*, as it leads to the increase in the volume of the charge conduction area, and thus to a general increase in current. These parasitic effects are mainly visible through an increase in the current at $V_{GS} \approx 0\,\mathrm{V}$ (a.k.a *leakage current*), because for $V_{GS} \leq V_{th}$ the main transistor does not transmit significant current, whereas the external channels, which are kept energized by the deposited charge, allow conduction.

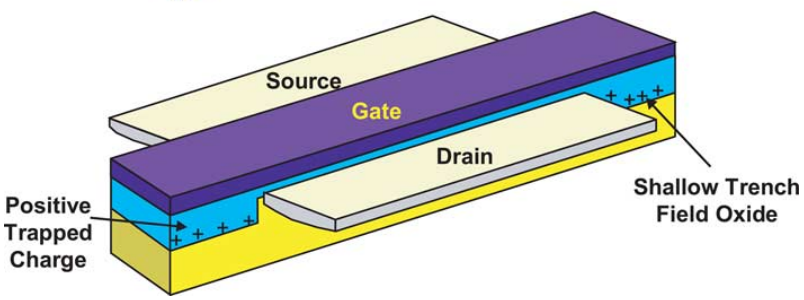


Figure 1.4: Trapped holes in STI regions.

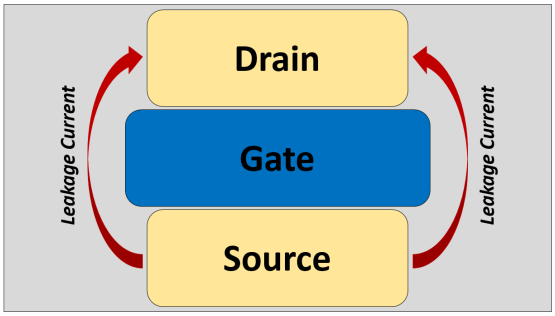


Figure 1.5: Leakage current possible paths.

Another important effect of ionizing radiation is the variation of the threshold voltage. As already mentioned, if a MOSFET is exposed to ionizing radiation its threshold voltage undergoes an alteration due to the parasitic charges accumulated within the gate oxide and the interface. In the case of NMOS this positive charge attracts the electrons that form the channel. Such effect is added to that of the positive voltage applied to the gate, so that the channel will be opened at a gate voltage less than would have been required under normal conditions. In the case of PMOS, in order to attract the holes that form the conductive channel the gate voltage must be negative. The presence of the positive charge in the oxide rejects these holes. It is therefore necessary that the voltage applied to the gate is smaller than the initial one, in order to balance the repulsive effect. As a result, in both cases the charges in the oxide reduce the threshold voltage.

Another non-negligible effect appearing at high dose, i.e. greater than 100 Mrad, is the fact that negative are trapped in the interface states at STI oxides. In case of PMOS devices this effect is in addiction to the trend given by the oxide-trapped charge, whereas for NOMS devices effects of inteface states can compensate oxide-trapped positive charge and even become dominant.

1.3 Experimental Details

1.3.1 Investigated devices

The MOSFETs studied in this work are standard threshold voltage (SVT) devices belonging to a 110 nm CMOS process and to a Low Power (LP) 65 nm CMOS process.

For 110 nm technology, the maximum allowed supply voltages V_{DD} is 1.4 V for core devices and 2.5 V for I/O devices with thicker gate oxide. The electrical oxide thickness t_{ox} is 3 nm for NMOS and 3.2 nm for PMOS which corresponds to a gate capacitance per unit area C_{ox} of about 10.8 fF/µm^2 for NMOS and 11.5 fF/µm^2 for PMOS. For 110 nm CMOS technology three types of devices are available for measurements:

- **Core devices with open layout:** the MOSFETs are laid out using a standard open structure, interdigitated configuration, with gate finger width of $W_f = 20$ µm, with the exception of the NMOS with $W/L = 600/0.12$ which is available also with $W_f = 10$ µm and 40 µm.
- **Core devices with enclosed layout:** NMOS devices are designed with an enclosed layout (ELT). Ten parallel devices are used for each geometry.
- **I/O devices with open layout:** these MOSFETs have a thicker gate oxide which allows for a maximum supply voltage $V_{DD} = 2.5$ V. Devices are laid out using a standard open structure, interdigitated configuration, with gate finger width of 30 µm.

Devices with enclosed geometry (edgeless layout transistor or ELT) are characterized by having a ring structure instead of a linear structure for the gate terminal. Such geometry in principle should not exhibit any radiation induced leakage current [3]. Gate dimensions (channel width W and length L) of 110 nm technology devices available for measurements are shown in Table 1.1. As shown in the Table 1.1, for some geometries, I/O devices with a gate oxide t_{OX} of 5.6 nm for NMOS and 5.9 nm for PMOS (thick gate oxide), and a deep N-well NMOS (DNW) are also available.

		Core Open		Core ELT		I/O Open	
W[µm]	L[µm]	N	P	N	P	N	P
100	0.12	∗	∗				
	0.24	∗	∗				
	0.36	∗	∗				
	0.72	∗	∗				
200	0.12	∗	∗	∗			
	0.24	∗	∗	∗			
	0.36	∗	∗				
	0.72	∗	∗				
600	0.12	∗	∗	∗			
	0.24	∗	∗	∗			
	0.34					∗	
	0.36	∗	∗				
	0.37						∗
	0.72	∗	∗	∗			

Table 1.1: 110 nm technology: gate geometries of the available N-channel and P-channel devices. Option availability is indicated with ∗ symbol.

For what concernes 65 nm technology, the maximum allowed supply voltage V_{DD} is 1.2 V. The electrical oxide thickness t_{ox} is 2.6 nm for NMOS and 2.8 nm for PMOS which corresponds to a gate capacitance per unit area C_{ox} of about 13 fF/µm^2 for NMOS and 12 fF/µm^2 for PMOS. Devices available for measurements are MOSFETs laid out using a standard open structure, interdigitated configuration MOSFETs designed with an enclosed layout (ELT). Gate dimensions (channel width W and length L) of devices available for measurements are shown in Table 1.2: the same geometries are available for both device polarity.

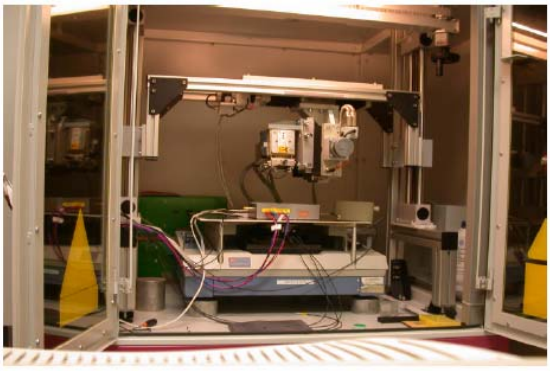
1.3.2 Irradiation Procedures

110 nm CMOS devices were irradiated at CERN facility, whereas 65 nm CMOS devices were irradiated at Laboratori di Legnaro, INFN. In all irradiations, the machine used is of the type Seifert model RP149 [4], Figure 1.6a, capable of supplying a maximum voltage of 50 kV and a maximum current of §50mA. It is equipped with electronic control of the X-Y position of the radiogenic tube, the power and intensity of the beam. The distance from the source to the target can be adjusted manually. The spectrum radiation, Figure 1.6b, of the tungsten anode consists of

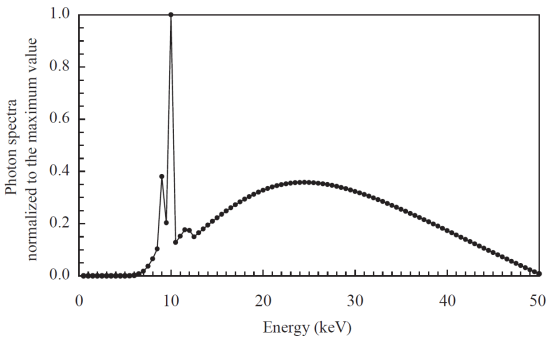
W[µm]	L[µm]	Note
0.12	0.065	
0.24	0.065	
	0.065	ELT
	0.50	
0.48	0.065	
1	0.065	
100	0.13	
	0.35	
200	0.065	
	0.13	
	0.35	
	0.50	
	0.70	
600	0.065	
	0.13	
	0.35	
	0.35	50 f
	0.35	120 f
	0.50	
	0.70	

Table 1.2: 65 nm technology: available gate geometries of channel N and P devices.

level L characteristic peaks, around 10 keV, and of the Bremsstrahlung component. The lower spectrum components are filtered by an aluminum foil of 150 µm. To change the dose rate, measured by a silicon diode, it is possible to act on the source power supply, or on the sample distance from the tube.



(a) X-ray radiation source.



(b) Normalized tungsten spectrum.

Figure 1.6: Irradiation setup and source spectrum.

The devices were irradiated with a dose rate of 9 krad(SiO_2)/s up to a total ionizing dose (TID) of 200 Mrad-600 Mrad and 5 Mrad (SiO_2) for 65 nm and 110 nm

technology respectively. The choice of the dose rate was dictated by the fact that a very high total dose had to be reached in a reasonable short time. During the irradiations, MOS devices were biased in the so called worst-case configuration (as reported in [5]). All terminals were connected to ground, except in the case of NMOS devices, where the gate was connected to the maximum bias voltage allowed by the technology. In such configuration, the transport of radiation-generated holes towards the Si-SiO_2 interface is maximized.

1.3.3 Measurements Setup

Measurements of static and signal parameters were carried out with an Agilent E5270B Precision Measurement Mainframe with E5281B SMU Modules. For Core and ELT devices the following measurements have been performed to study the static behavior:

- I_D-V_{GS} characteristics
  - V_{GS} from $-0.3\,\mathrm{V}$ to V_{DD} with $5\,\mathrm{mV}$ step
  - V_{DS} from $0\,\mathrm{V}$ to V_{DD} with $0.2\,\mathrm{V}$ step + $V_{DS} = 10\,\mathrm{mV}$
- I_D-V_{DS} characteristics
  - V_{DS} from $0\,\mathrm{V}$ to V_{DD} with $5\,\mathrm{mV}$ step
  - V_{GS} from $0\,\mathrm{V}$ to V_{DD} with $0.2\,\mathrm{V}$ step

For I/O devices measurements have been extended to a maximum supply voltage of $V_{DD} = 2.5\,\mathrm{V}$.

The value of the transconductance g_m was extracted from I_D-V_{GS} curves and its behavior has been studied as a function of the gate-to-source voltage V_{GS} and of the drain current I_D.

From the standpoint of ionizing radiation effects, the variation of the following static parameters is of utmost importance:

- **Threshold voltage (V_{Th}):** obtained with the quadratic extrapolation method from the $I_D - V_{GS}$ plot measured at $V_{DS} = 1.2\,\mathrm{V}$ for Core and ELT devices and at $V_{DS} = 2.5$ V for I/O devices.
- **OFF current (I_{off}):** subthreshold leakage current measured at $V_{GS} = 0$ and $V_{DS} = 1.2$ V for Core and ELT devices and at $V_{DS} = 1.2\,\mathrm{V}$ for I/O devices.
- **ON current (I_{on}):** maximum drive current measured at $V_{GS} = V_{DS} = 1.2$ V for Core and ELT devices and at $V_{GS} = V_{DS} = 2.5$ V for I/O devices.

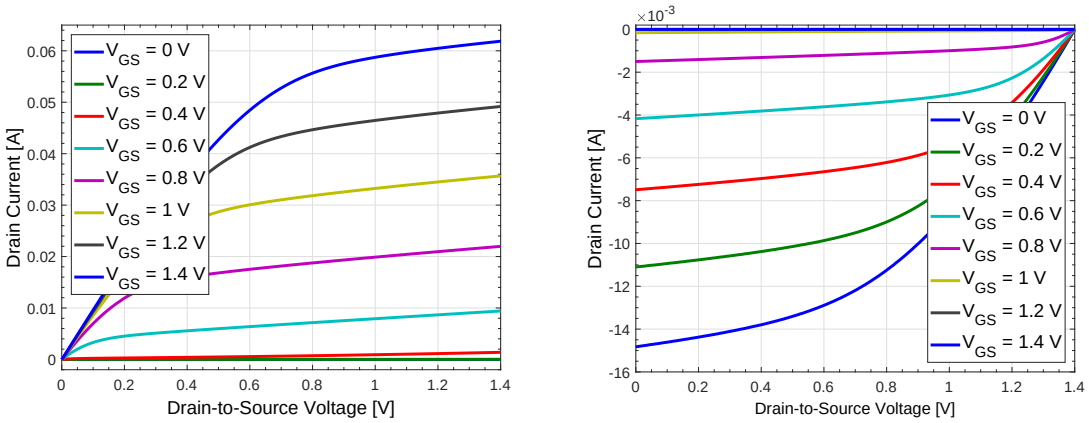
- **Maximum transconductance ($g_{m,max}$):** maximum value of the channel transconductance extracted from the $I_D - V_{GS}$ curve measured at $V_{DS} = 1.2\,\text{V}$ for Core and ELT devices and at $V_{DS} = 1.2\,\text{V}$ for I/O devices.

The spectral density of the noise in the the channel current was studied by measuring the equivalent noise voltage spectrum referred to the gate. These measurements were carried out with a Network/Spectrum Analyzer (Agilent 4395A). This instrument allows for noise measurements within the 100 Hz - 200 MHz frequency range [6]. In order to measure the noise power spectral density of a single device (or also an integrated circuit), an ad-hoc interface circuit able to amplify noise to be measured is needed. In the case of single device, such circuit has to correctly polarize the device. This circuit is called preamplifier and has been designed in order to show negligible noise component with respect to those featured by the devices under test.

1.4 Experimental Results - Static and Signal Parameters

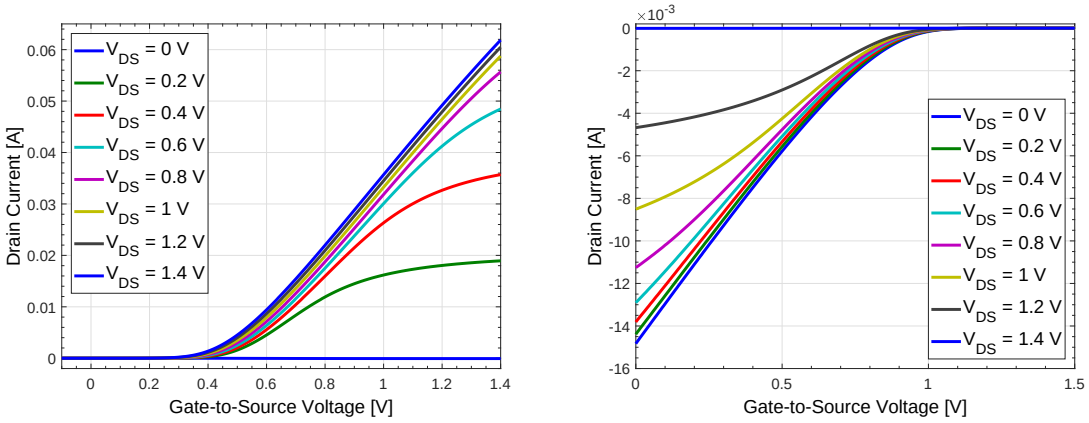
1.4.1 110 nm technology

A typical set of plots obtained from static and signal measurements of two packages (package #5 for NMOS devices and package #2 for PMOS devices) have been gathered in Fig. 1.7a, 1.7b, 1.8a, 1.8b, 1.9a and 1.9b.



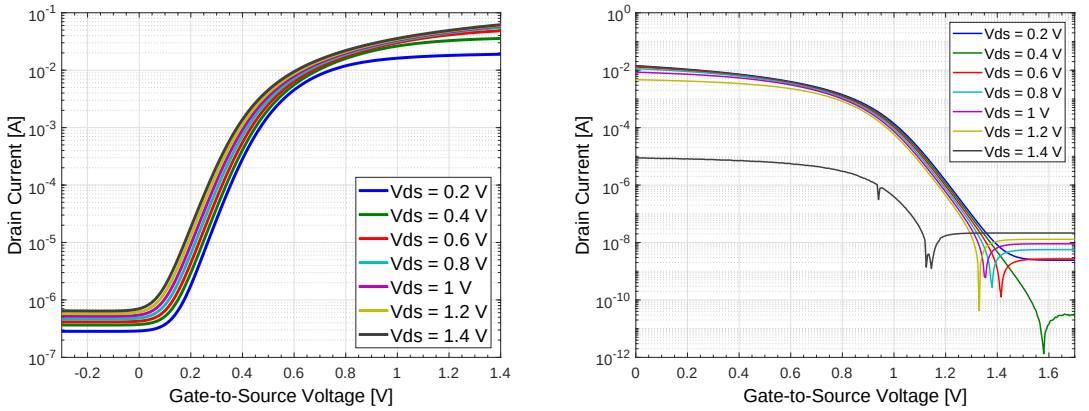
(a) N-channel $W/L = 100/0.12$. **(b)** P-channel $W/L = 100/0.12$.

Figure 1.7: Drain current I_D as a function of V_{DS} with V_{GS} as parameter.



(a) N-channel $W/L = 100/0.12$. **(b)** P-channel $W/L = 100/0.12$.

Figure 1.8: Drain current I_D as a function of V_{GS} with V_{DS} as parameter.



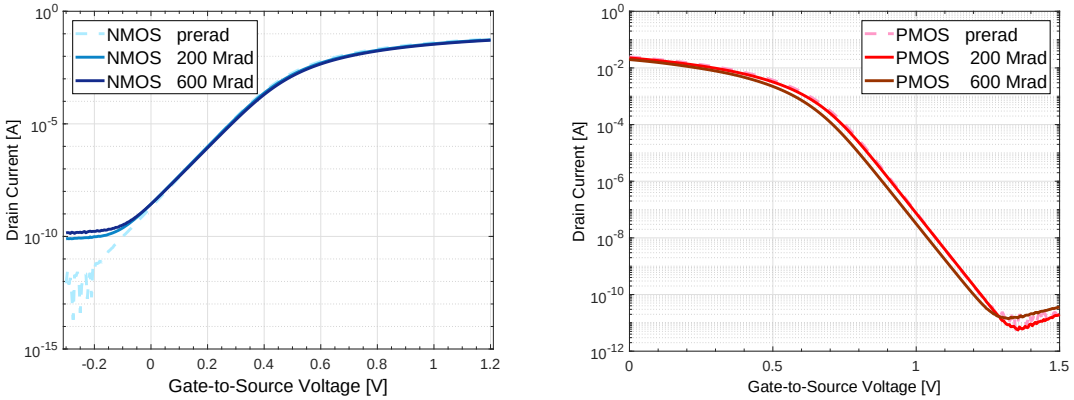
(a) N-channel $W/L = 100/0.12$. **(b)** P-channel $W/L = 100/0.12$.

Figure 1.9: I_D as a function of V_{GS} in log scale with V_{DS} as parameter.

Drain Current Characteristics

Figures 1.10a and 1.10b show the typical behaviour of the drain current as a function of gate-to-source voltage for an NMOS and a PMOS devices respectively, before and after irradiation at 5 Mrad of 110 nm technology. Little variations of the leakage current are observed. As expected such difference is more appreciable in NMOS devices than PMOS devices.

Regarding current measurements, the OFF current (I_{off}) was measured at $V_{GS} = 0\,\text{V}$ and $|V_{DS}| = 1.4\,\text{V}$ for Core and ELT devices and at $|V_{DS}| = 2.5\,\text{V}$ for devices of the I/O type before and after irradiation. It is possible to observe that there is an appreciable increase of this constant leakage current for NMOSFETs of the order of hundreds of nA, whereas for PMOS devices there is a very tiny decrease (less than 1 nA). As a matter of fact, positive charge accumulated in PMOSFETs oxides tends



(a) N-channel with $W = 200\,\mu m$ and $L = 0.12\,\mu m$.

(b) P-channel with $W = 200\,\mu m$ and $L = 0.12\,\mu m$.

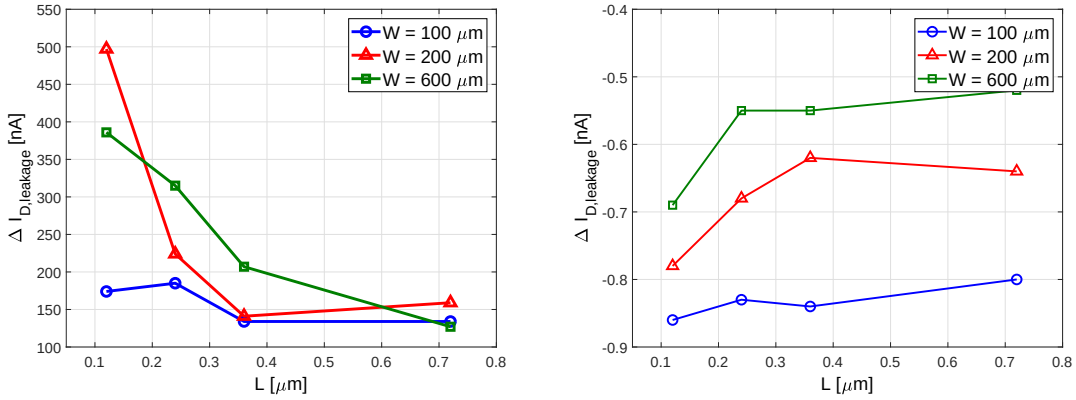
Figure 1.10: Drain current I_D with respect to V_{GS} for devices biased at $|V_{DS}| = 1.4\,V$ and $V_{BS} = 0\,V$, before and after irradiation up to 5 Mrad TID.

to switch off parasitic leakage current paths. On the contrary the increase of the NMOS leakage current is probably caused by edge effects due to radiation-induced charge at shallow trench isolation (STI) oxides [7], [8]. Table 1.3 reports all measured I_{off} of 110 nm CMOS technology devices. Figures 1.11a and 1.11b show the trend of $\Delta I_{D,leakage}$ as a function of the channel length L for different channel widths W, respectively for NMOSFETs and PMOSFETs. It is possible to observe a larger increment for shorter channel devices.

W/L	**# finger**	**NMOS I_{off} [nA]**			**PMOS I_{off} [nA]**		
		Before	**5 Mrad**	**ΔI_{off}**	**Before**	**5 Mrad**	**ΔI_{off}**
100/0.12	5	756	930	174	9.27	8.41	-0.86
100/0.24	5	752	937	185	9.38	8.55	-0.83
100/0.36	5	752	886	134	9.51	8.67	-0.84
100/0.72	5	749	883	134	9.61	8.81	-0.8
200/0.12	10	762	1259	497	9.92	9.14	-0.78
200/0.24	10	756	980	224	9.72	9.04	-0.68
200/0.36	10	758	899	141	9.9	9.28	-0.62
200/0.72	10	759	918	159	9.9	9.26	-0.64
600/0.12	30	786	1172	386	10.53	9.84	-0.69
600/0.24	30	768	1083	315	10.29	9.74	-0.55
600/0.36	30	768	975	207	10.32	9.77	-0.55
600/0.72	30	766	893	127	10.32	9.8	-0.52

Table 1.3: I_{off} measurements of all 110 nm CMOS technology.

The ON current (I_{on}) was measured at $|V_{DS}| = |V_{GS}| = 1.4\,V$ for Core and ELT devices and at $|V_{DS}| = |V_{GS}| = 2.5\,V$ for thick oxide I/O devices of 110 nm



(a) N-channel devices. **(b)** P-channel devices.

Figure 1.11: $\Delta I_{D,leakage}$ with respect to the length L for different widths W.

technology and $|V_{DS}| = |V_{GS}| = 1.2\,\text{V}$ for Core and ELT devices of 65 nm technology. This parameter was measured before and after irradiations.

Data point out that there are no significant changes due to ionizing radiation, in fact the highest increase is around 0.2% with respect to the initial I_{ON}, for Core, Enclosed Layout and thick oxide I/O.

Threshold Voltage

Threshold voltage (V_{Th}) was obtained with the quadratic extrapolation method from the $I_D - V_{GS}$ plot measured at $|V_{DS}| = 1.2\,\text{V}$ for Core and ELT devices and at $|V_{DS}| = 2.5\,\text{V}$ for thick oxide I/O devices [9].

Ionizing radiation seems to cause no appreciable effects for $|V_{GS}| \geq |V_{Th}|$ either for Core, Enclosed Layout and I/O devices. The threshold voltage shift averaged on all samples for linear and enclosed layout ΔV_{Th} is very small: $\Delta V_{Th} = -0.6\,\text{mV}$ for N-channel MOS devices and $\Delta V_{Th} = 1.9\,\text{mV}$ for P-channel MOS devices. Thick oxide I/O devices show a higher threshold voltage shift $|\Delta V_{Th}| \approx 10\,\text{mV}$. This phenomenon can be ascribed to their thicker gate oxide. Table 1.4 reports all measured threshold voltage of 110 nm technology linear core devices.

Transconductance

Transconductance g_m is an index regarding the amplifying characteristics of the MOSFET, because drain current is a function of gate to source voltage. The transconductance is defined as the derivative of I_D with respect to V_{GS}:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{1.18}$$

W/L	# finger	NMOS V_{th} [mV] Before	5 Mrad	ΔV_{th}	PMOS V_{th} [mV] Before	5 Mrad	ΔV_{th}
100/0.12	5	288.5	287.9	-0.6	327.8	329.0	1.2
100/0.24	5	337.4	337.1	-0.3	365.5	366.4	0.9
100/0.36	5	333.1	332.5	-0.6	363.8	365.7	1.9
100/0.72	5	324.8	323.5	-1.3	361.9	363.7	1.8
200/0.12	10	264.0	264.2	0.2	305.6	308.2	2.5
200/0.24	10	318.7	318.3	-0.3	352.6	354.8	2.2
200/0.36	10	314.8	314.5	-0.3	352.2	354.5	2.3
200/0.72	10	307.9	307.2	-0.6	354.3	356.5	2.1
600/0.12	30	221.4	220.6	-0.8	267.3	269.3	2.0
600/0.24	30	280.9	279.8	-1.1	324.2	326.5	2.3
600/0.36	30	279.1	278.4	-0.7	326.4	328.7	2.3
600/0.72	30	275.0	274.4	-0.6	332.8	334.2	1.4

Table 1.4: V_{th} measurements of all 110 nm CMOS technology.

The value of the transconductance g_m was extracted from $I_D - V_{GS}$ curves and its behavior has been studied as a function of the gate-to-source voltage V_{GS} and of the drain current I_D before and after irradiations. Figure 1.12 shows the transconductance g_m as a function of the drain current I_D, up to $I_D = 1\,\text{mA}$, before and after exposure to X-rays, for PMOS and NMOS devices with $W/L = 100/0.36$ biased at $|V_{DS}| = 0.6\,\text{V}$ and $V_{BS} = 0\,\text{V}$. As expected from the $I_D - V_{GS}$ curves, ionizing radiation seems to give no appreciable variations of the transconductance. All other devices (Core, ELT and I/O) show the same behaviour for all the considered drain to source voltage.

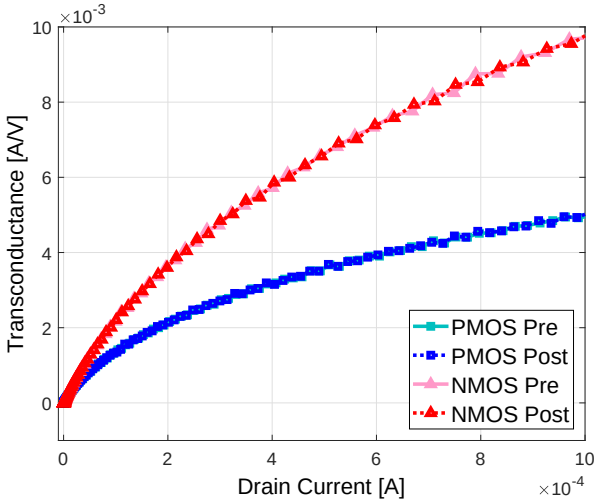
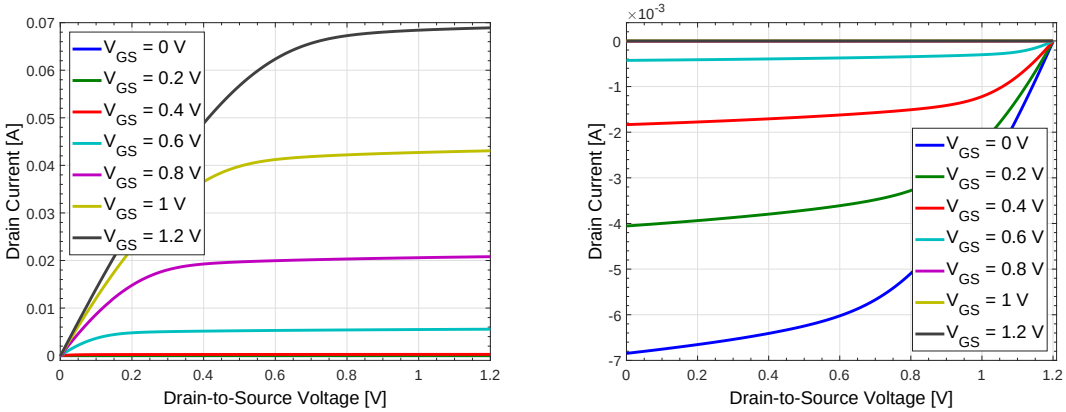


Figure 1.12: Transconductance g_m as a function of the drain current I_D, before and after irradiation up to 5 Mrad total dose, for PMOS and NMOS devices with $W/L = 100/0.36$ biased at $|V_{DS}| = 0.6\,\text{V}$ and $V_{BS} = 0\,\text{V}$.

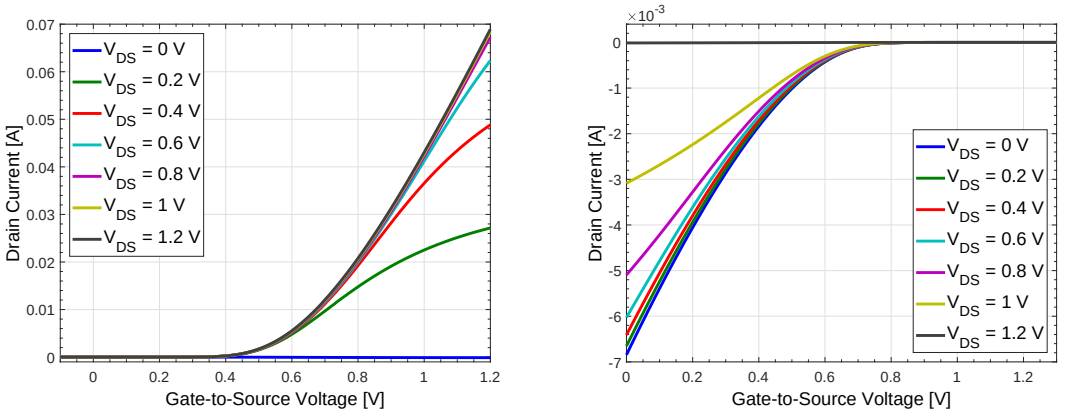
1.4.2 65 nm technology

A typical set of plots obtained from static and signal measurements of two packages (package #1 for NMOS devices and package #2 for PMOS devices) have been gathered in Fig. 1.13a, 1.13b, 1.14a, 1.14b, 1.15a, 1.15b, 1.16a and 1.16b.



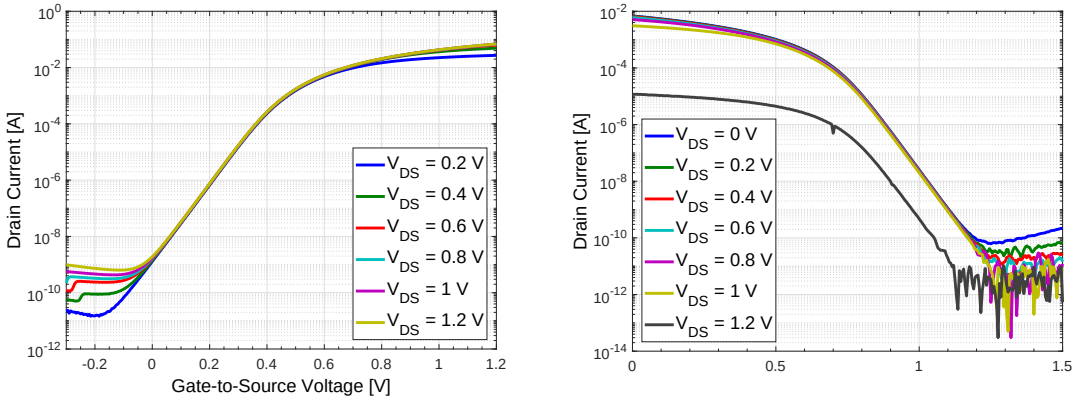
(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

Figure 1.13: Drain current I_D as a function of V_{DS} with V_{GS} as parameter.



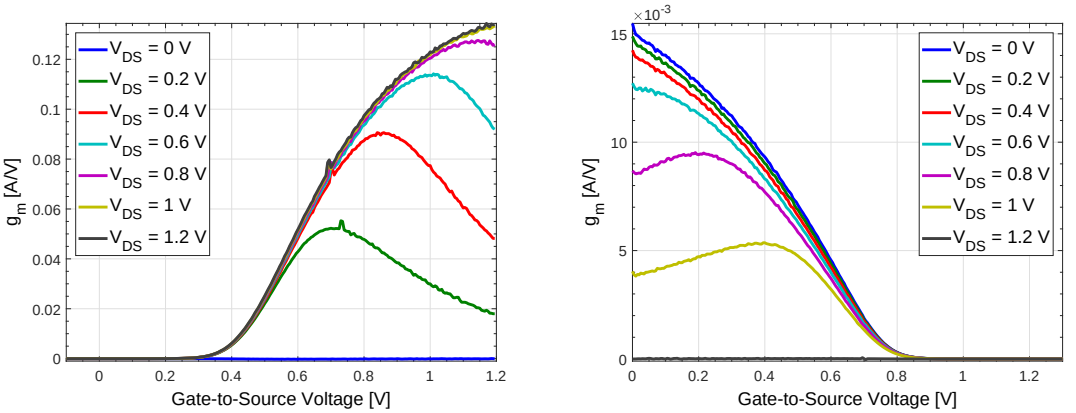
(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

Figure 1.14: Drain current I_D as a function of V_{GS} with V_{DS} as parameter.



(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

Figure 1.15: I_D as a function of V_{GS} in log scale with V_{DS} as parameter.



(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

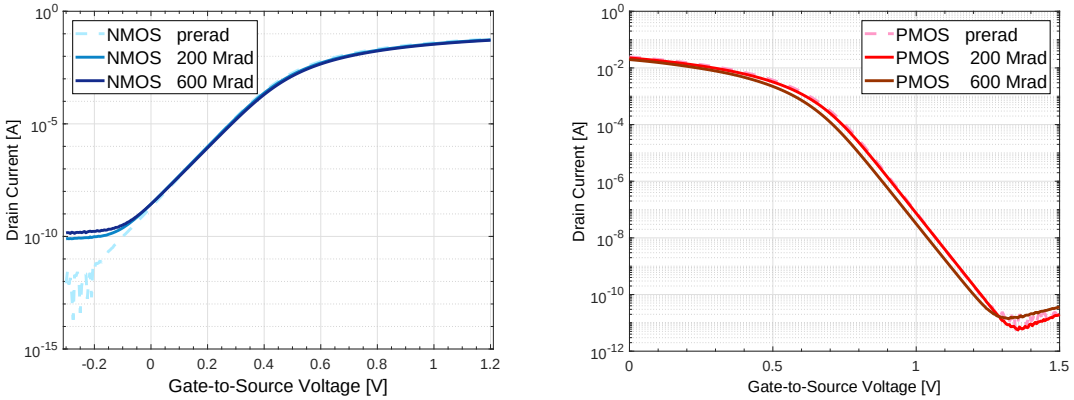
Figure 1.16: Transconductance g_m as a function of V_{GS} with V_{DS} as parameter.

Drain Current Characteristics

Figures 1.17a and 1.17b show the typical behaviour of the drain current as a function of gate-to-source voltage for an NMOS and a PMOS devices respectively, before and after irradiation at 200 Mrad and 600 Mrad.

A variation of the leakage current is observed. As predicted from the theory, such difference is more appreciable in NMOS devices.

Regarding current measurements, the OFF current (I_{off}) was measured at $V_{GS} = 0\,\text{V}$ and $|V_{DS}| = 1.2\,\text{V}$ for all devices before and after all irradiations. It is possible to observe that there is very little increase of this constant leakage current for NMOSFETs equivalent in the worst case to $\sim 30\,\text{nA}$, after both irradiations. Consinstently to 110 nm technology, for PMOS devices there is a very tiny decrease (less than 0.1 nA). Generally a higher TID for 65 nm technology devices seems to cause much smaller effects than the ones detected for 110 nm CMOS technology. Table 1.5



(a) N-channel with $W = 200\,\mu m$ and $L = 0.13\,\mu m$.

(b) P-channel with $W = 200\,\mu m$ and $L = 0.13\,\mu m$.

Figure 1.17: Drain current I_D with respect to V_{GS} for devices biased at $|V_{DS}| = 1.2\,V$ and $V_{BS} = 0\,V$, before and after irradiation up to 200 Mrad and 600 Mrad TID.

reports all measured I_{off} of 65 nm CMOS technology devices. One particular fact that can be observed from this table is that the two PMOS with $W/L = 600/0.350$ but with slightly different number of fingers show different ΔI_{off}. In particular, the 120 fingers device shows an I_{off} before irradiations and a $|\Delta I_{off}|$ higher than the 50 fingers ones. This fact can be ascribed to the larger number of external channels, due to the greater number of fingers.

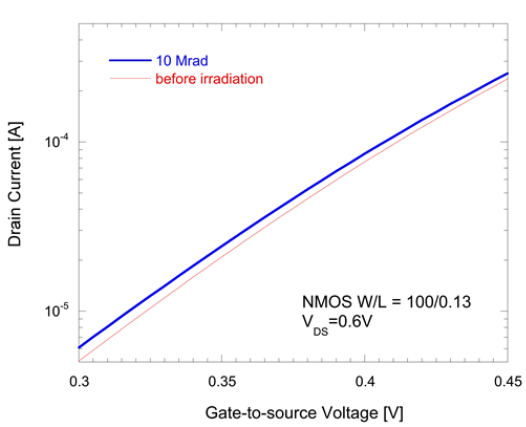
Generally, for NMOS devices, no sizable effects can be seen in devices with large W/L, except in the leakage current region. Comparing to a previous irradiation campaign [10], it is possible to see interesting effects that may be correlated with the behavior of noise in irradiated devices (see paragraph 1.5.2). In figures 1.18a and 1.18b $I_D - V_{GS}$ curves appear to shift in different directions, moving up at 10 Mrad, i.e. higher drain curretn at same V_{GS}, and then down at 200 Mrad and 600 Mrad, i.e. lower drain current at same V_{GS}.

This effect can be ascribed to the fact that at low TID, positive charge in STI oxides switches on lateral devices, increasing I_D (for the same V_{GS}). At higher doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge, switching off lateral parasitic transistors and reducing I_D (for the same V_{GS}), e.g. figure 1.19a and 1.19b shows the behaviour of NMOS with $W/L = 100/0.13$.

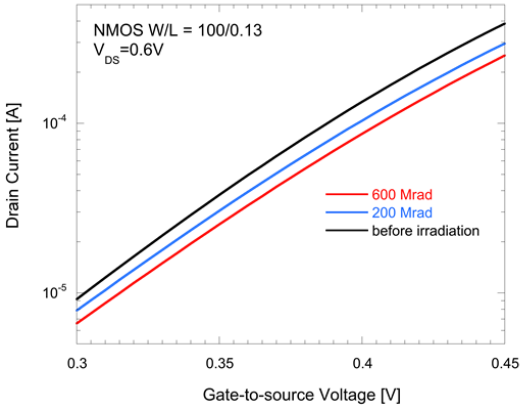
For what concernes PMOS devices, comparing results to previous irradiation tests at 5 Mrad [10], $I_D - V_{GS}$ curves appear to shift in the same direction (left) both at 5 Mrad (very slightly) and at 200 Mrad and 600 Mrad, see figure 1.20a and 1.20b. Figure 1.21 shows the drain current percentage variation of a PMOS with

W/L	NMOS I_{off} [A]			PMOS I_{off} [A]		
	Prerad	200 Mrad	600 Mrad	Prerad	200 Mrad	600 Mrad
0.12/0.065	$1.55 \cdot 10^{-10}$	$4.50 \cdot 10^{-9}$	$5.52 \cdot 10^{-9}$	-	-	-
0.24/0.065	-	-	-	$6.99 \cdot 10^{-11}$	$2.33 \cdot 10^{-9}$	$2.66 \cdot 10^{-9}$
0.24/0.065 EL	$2.02 \cdot 10^{-10}$	$4.45 \cdot 10^{-9}$	$5.42 \cdot 10^{-9}$	$5.01 \cdot 10^{-12}$	$7.89 \cdot 10^{-12}$	$2.14 \cdot 10^{-12}$
0.48/0.065	$5.78 \cdot 10^{-12}$	$2.10 \cdot 10^{-10}$	$2.57 \cdot 10^{-10}$	-	-	-
1/0.065	$3.12 \cdot 10^{-8}$	$5.5 \cdot 10^{-8}$	$3.48 \cdot 10^{-8}$	-	-	-
100/0.130	$9.17 \cdot 10^{-10}$	$1.35 \cdot 10^{-9}$	$1.32 \cdot 10^{-9}$	-	-	-
100/0.350	$2.36 \cdot 10^{-10}$	$3.52 \cdot 10^{-10}$	$3.70 \cdot 10^{-10}$	$5.31 \cdot 10^{-11}$	$3.57 \cdot 10^{-11}$	$2.32 \cdot 10^{-11}$
200/0.065	-	-	-	-	-	-
200/0.130	$1.97 \cdot 10^{-9}$	$2.74 \cdot 10^{-9}$	$2.72 \cdot 10^{-9}$	$1.96 \cdot 10^{-10}$	$2.10 \cdot 10^{-10}$	$1.01 \cdot 10^{-10}$
200/0.350	$6.46 \cdot 10^{-10}$	$4.99 \cdot 10^{-10}$	$6.03 \cdot 10^{-10}$	$9.46 \cdot 10^{-11}$	$9.25 \cdot 10^{-11}$	$5.61 \cdot 10^{-11}$
200/0.500	$1.30 \cdot 10^{-8}$	$1.89 \cdot 10^{-8}$	$2.04 \cdot 10^{-8}$	$6.46 \cdot 10^{-11}$	$7.12 \cdot 10^{-11}$	$62.56 \cdot 10^{-11}$
200/0.700	$5.30 \cdot 10^{-10}$	$4.73 \cdot 10^{-9}$	$6.00 \cdot 10^{-9}$	$5.44 \cdot 10^{-11}$	$5.28 \cdot 10^{-11}$	$2.59 \cdot 10^{-11}$
600/0.065	$1.51 \cdot 10^{-7}$	$1.80 \cdot 10^{-7}$	$1.59 \cdot 10^{-7}$	$6.02 \cdot 10^{-9}$	$4.48 \cdot 10^{-9}$	$4.58 \cdot 10^{-9}$
600/0.130	$5.94 \cdot 10^{-9}$	$8.92 \cdot 10^{-9}$	$8.63 \cdot 10^{-9}$	$5.76 \cdot 10^{-10}$	$6.39 \cdot 10^{-10}$	$4.80 \cdot 10^{-10}$
600/0.350 50 finger	-	-	-	$3.14 \cdot 10^{-10}$	$2.64 \cdot 10^{-10}$	$2.19 \cdot 10^{-10}$
600/0.350 120 finger	$1.55 \cdot 10^{-9}$	$2.37 \cdot 10^{-9}$	$2.17 \cdot 10^{-9}$	$3.48 \cdot 10^{-10}$	$2.79 \cdot 10^{-10}$	$2.35 \cdot 10^{-10}$
600/0.500	$1.36 \cdot 10^{-9}$	$1.89 \cdot 10^{-9}$	$1.89 \cdot 10^{-9}$	$2.70 \cdot 10^{-10}$	$2.17 \cdot 10^{-10}$	$1.74 \cdot 10^{-10}$
600/0.700	$1.19 \cdot 10^{-9}$	$1.70 \cdot 10^{-9}$	$1.57 \cdot 10^{-9}$	$2.13 \cdot 10^{-10}$	$1.71 \cdot 10^{-10}$	$1.55 \cdot 10^{-10}$

Table 1.5: I_{off} measurements of all 65 nm CMOS technology.

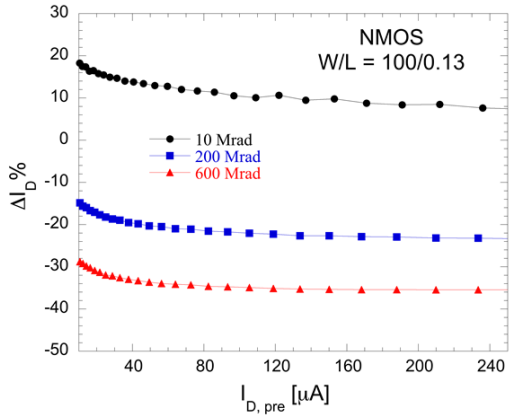


(a) Irradiation up to 10 Mrad.

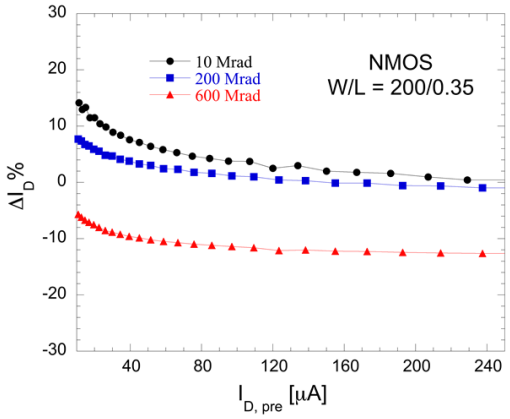


(b) Irradiation up to 200 Mrad and 600 Mrad.

Figure 1.18: Detail of I_D as a function of V_{GS} for NMOS with $W/L = 100/0.13$.



(a) NMOS with $W/L = 100/0.13$.

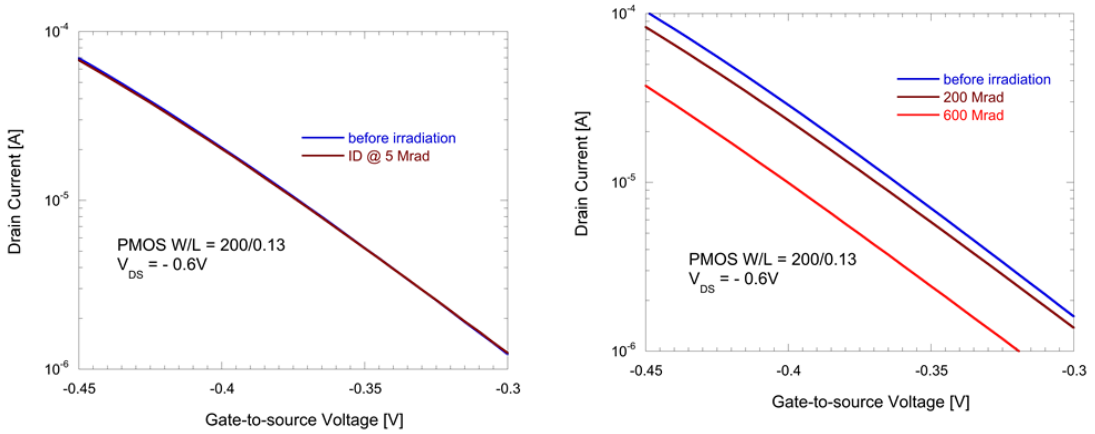


(b) NMOS with $W/L = 200/0.35$.

Figure 1.19: Detail of I_D as a function of V_{GS} for NMOS devices.

$W/L = 200/0.13$ for TID up to 600 Mrad. This behavior confirms that, unlike NMOS devices, trapped charge in the oxide region are not compensated by interface states, but they contribute in the same direction.

The ON current (I_{on}) was measured at $|V_{DS}| = |V_{GS}| = 1.2\,\text{V}$ for Core and ELT devices. This parameter was measured before and after irradiations. Table 1.6 reports averaged values of percentage variation of I_{on} current for both NMOS and PMOS with a channel width greater or lower than 1 µm. Such value was chosen because, for $W > 1\,\mu\text{m}$, I_{on} current devices seems to be less affected by ionizing radiation, i.e. the averaged decrease of I_{on} current is greater for $W \leq 1\,\mu\text{m}$ for both polarity.



(a) Irradiation up to 5 Mrad.

(b) Irradiation up to 200 Mrad and 600 Mrad.

Figure 1.20: Detail of I_D as a function of V_{GS} for PMOS with $W/L = 200/0.13$.

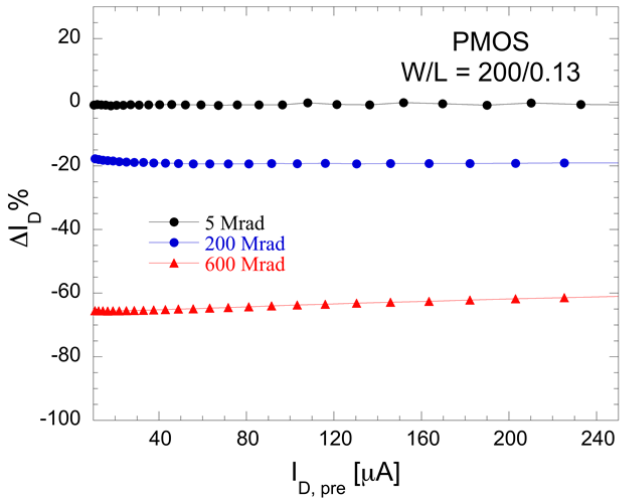


Figure 1.21: $\Delta I_D\%$ for PMOS $W/L = 200/0.13$ belonging to 65 nm technology at different TID.

W [µm]	NMOS TID		PMOS TID	
	200 Mrad	600 Mrad	200 Mrad	600 Mrad
$W \leq 1$	-15%	-20%	-25%	-43%
$W > 1$	-6%	-9%	-5%	-13%

Table 1.6: Averaged values of percentage variation of I_{on} current for both NMOS and PMOS with a channel width greater or lower than 1 µm.

Threshold Voltage

Threshold voltage (V_{Th}) was obtained with the quadratic extrapolation method from the $I_D - V_{GS}$ plot measured at $|V_{DS}| = 1.2$ V for Core and ELT devices [9]. The be-

havior of the drain current is confirmed by the trend of the radiation-induced threshold shift, which in NMOSFETs is negative at 10 Mrad and positive at 200 Mrad and 600 Mrad. Because of the effect of interface states, $I_D - V_{GS}$ curves are also stretched at high TID. For PMOSFETs the maximum $|\Delta V_{th}|$ is smaller than 40 mV and increases with the TID, see figure 1.22. For NMOSFETs at relatively low dose, i.e. 10 Mrad, the threshold voltage is lower the one extrapolated before irradiation, whereas for high dose, i.e. 200 Mrad and 600 Mrad, the threshold voltage is higher than the one extrapolated before irradiation. Such "change in direction" is another confermation to the fact that at higher doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge.

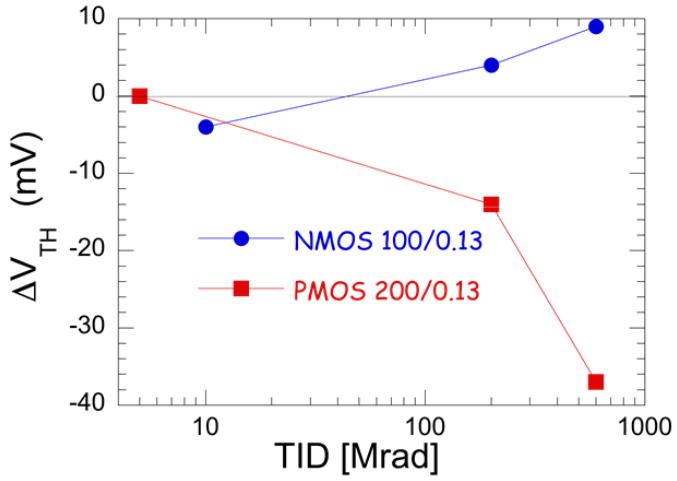


Figure 1.22: Threshold Voltage shift for NMOS with $W/L = 100/0.13$ and PMOS $W/L = 200/0.13$ belonging to 65 nm technology at different TID.

Transconductance

The value of the transconductance g_m was extracted from $I_D - V_{GS}$ curves and its behavior has been studied as a function of the gate-to-source voltage V_{GS} and of the drain current I_D before and after irradiations. No appreciable variations of the transconductance are detected. Figure 1.23 shows the transconductance g_m as a function of the drain current I_D, up to $I_D = 30$ mA, before and after exposure to X-rays, for PMOS and NMOS devices with $W/L = 100/0.35$ biased at $|V_{DS}| = 0.6$ V and $V_{BS} = 0$ V. As for the 110 nm technology such results was expected from the $I_D - V_{GS}$ curves.

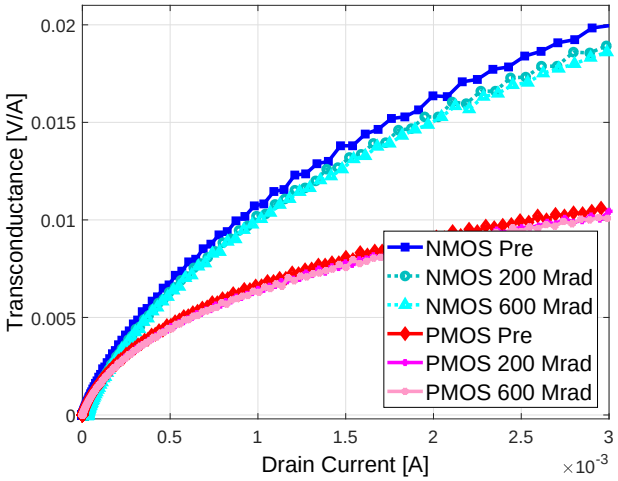


Figure 1.23: Transconductance g_m as a function of the drain current I_D, before and after irradiations up to 200 Mrad and 600 Mrad total dose, for PMOS and NMOS devices with $W/L = 100/0.35$ biased at $|V_{DS}| = 0.6\,\text{V}$ and $V_{BS} = 0\,\text{V}$.

1.5 Experimental Results - Noise Voltage Spectrum

1.5.1 110 nm technology

As already metioned in 1.1.5, Noise Voltage Spectrum of a MOSFET device can be modeled by the sum of two noise term: flicker or 1/f noise and white noise. Flicker noise is characterized by a power spectral density that is inversely proportional to frequency:

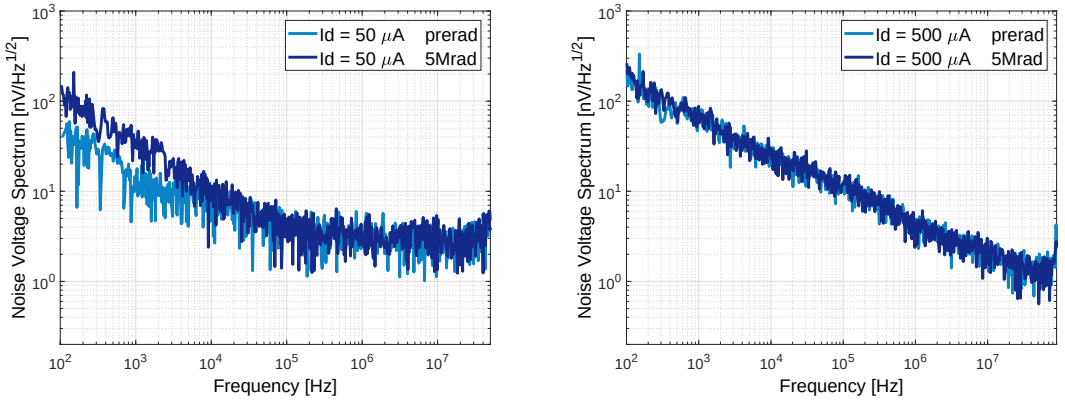
$$S^2_{1/f}(f) = \frac{K_f}{C_{OX}WL}\frac{1}{f^{\alpha_f}} \tag{1.19}$$

For the examined 110 nm technology, typical α_f values are 1.01 for the PMOS and 0.93 for the NMOS. Different profile of oxide traps interacting with carriers of different polarity might be the cause of this behavior ([11] [12]). Previous studies of the noise properties of scaled CMOS processes pointed out that α_f is independent of the device drain current and of the gate length and width ([13] [14]). The behavior of the 1/f and channel thermal noise components was monitored before and after irradiation.

Effects on Noise Voltage Spectrum of 110 nm technology will be discussed in what follows.

Figures 1.24a and 1.24b show data for open layout NMOSFETs devices whereas Figure 1.25 shows data for an enclosed layout NMOS device. In agreement with the negligible post-irradiation change of the transconductance, channel thermal noise does not seem to be affected by ionizing radiation. The increase of 1/f noise is

small, too. In particular, both open layout and enclosed layout devices show a comparable slight rise in the 1/f noise. This little noise sensitivity is likely to be associated with the very thin gate oxide and correlated to the negligible threshold voltage shift. This change in the 1/f noise component becomes less important at higher I_D, in fact in Figure 1.24a, where the devices was operating at $I_D = 50\,\mu A$, it is possible to observe a larger increase of the flicker noise than the one detected in Figure 1.25, where the devices was operating at $I_D = 500\,\mu A$. This can be related to the larger impact of noise associated to the lateral parasitic transistors at small I_D density [15], in fact this effect is less evident in enclosed layout devices as represented in Figure 1.25.



(a) NMOS with $W/L = 600/0.72$ at $I_D = 50\,\mu A$.

(b) NMOS with $W/L = 600/0.12$ at $I_D = 500\,\mu A$.

Figure 1.24: Noise voltage spectra before and after exposure to X-rays (5 Mrad integrated dose) of 110 nm CMOS technology devices

As far as PMOSFETs are concerned, the behaviour after irradiation is slightly different. Although no changes either in white noise or in 1/f noise are detected, a Lorentzian noise component appears in the noise voltage spectrum. This can be modeled by an additional term in equation (1.12):

$$S_L^2 = \frac{A_L}{1 + (2\pi f)^2 \tau_L^2} \tag{1.20}$$

This Lorentzian term may arise from radiation-induced defects which act as traps for charge carriers in the device channel. In (1.20), A_L and τ_L are determined by the physical nature of the traps. The Lorentzian term has a constant amplitude A_L up to the frequency $f_L = 1/(2\pi\tau_L)$ and then falls off as $1/f^2$. This contribution is much more evident for bigger devices, in fact figures 1.26a and 1.26b represent PMOS devices with $W/L = 600/0.12$ and $W/L = 200/0.12$ respectively. Further studies are needed to investigate the reason of this behaviour.

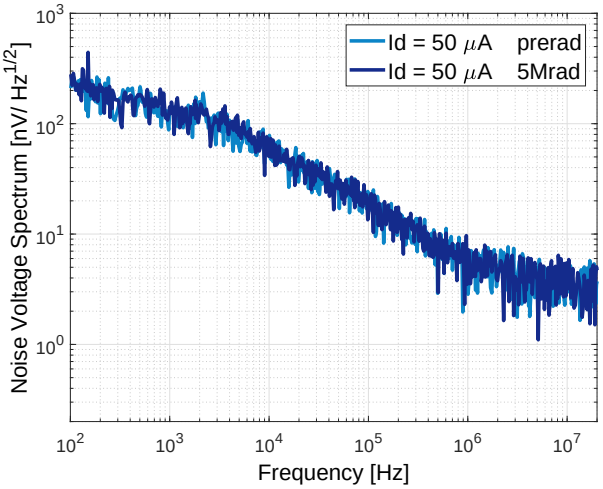
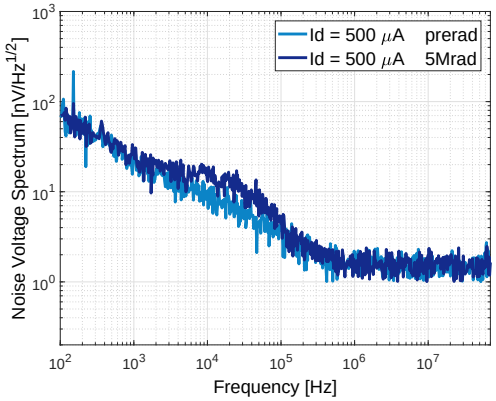
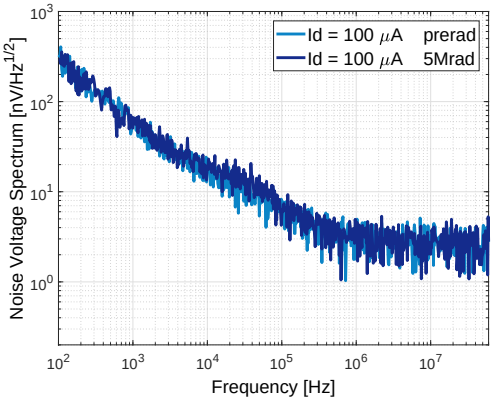


Figure 1.25: Noise voltage spectra before and after exposure to X-rays (5 Mrad integrated dose) of an NMOS with $W/L = 200/0.12$ EL belonging to the 110 nm technology at $I_D = 50\,\mu A$.



(a) PMOS with $W/L = 600/0.12$ at $I_D = 500\,\mu A$.



(b) PMOS with $W/L = 200/0.12$ at $I_D = 100\,\mu A$.

Figure 1.26: Noise voltage spectra before and after exposure to X-rays (5 Mrad integrated dose) of 110 nm CMOS technology devices

1.5.2 65 nm technology

For the examined 65 nm CMOS technology, typical α_f values are 0.88 and 1.19 for NMOS and PMOS respectively.

Regarding radiation effects on Noise Voltage Spectra of 65 nm technology devices, the following phenomena have been observed.

Figure 1.27 shows typical data for open layout NMOSFETs device operating at low current density. In agreement with the negligible post-irradiation change of the transconductance, channel thermal noise does not seem to be affected by ionizing radiation. The increase of 1/f noise is small, too. Consistently with 110 nm tech-

nology, this little noise sensitivity is likely to be associated with the very thin gate oxide.

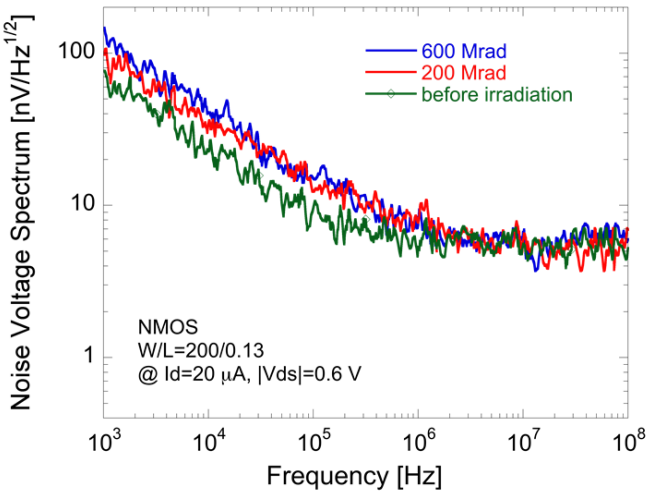
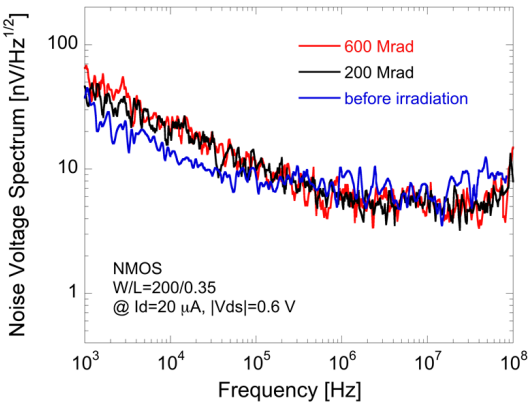
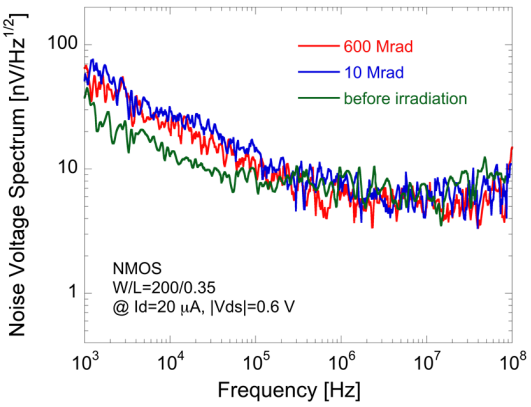


Figure 1.27: Noise voltage spectra before and after exposure to X-rays (200 and 600 Mrad integrated dose) of an NMOS with $W/L = 200/0.13$ belonging to the 65 nm technology at $I_D = 20\,\mu A$.

At 200 Mrad (and even 600 Mrad), at low I_D 1/f noise increase with respect to pre-irradiation values is smaller than the one detected in previous irradiation tests at 10 Mrad [10], as shown in figures 1.28a and 1.28b. Such effect can be correlated with the evolution of radiation effects at increasing TID and with the behavior of $I_D - V_{GS}$.



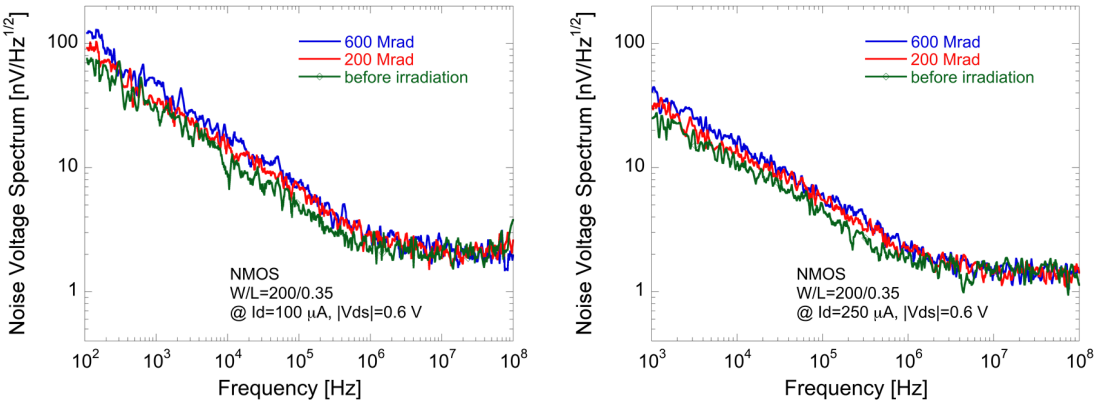
(a) Noise Voltage Spectrum before and after 200 Mrad and 600 Mrad of TID.



(b) Noise Voltage Spectrum before and after 10 Mrad and 600 Mrad of TID.

Figure 1.28: NMOS device with $W/L = 200/0.35$ belonging to 65 nm CMOS technology operating with $I_D = 20\,\mu A$.

The change in the 1/f noise component becomes less important at higher I_D, in fact in figure 1.27, where the device was operating at $I_D = 20\,\mu A$, it is possible to observe a larger increase of the flicker noise than the detected ones in figures 1.29a and 1.29b, where the device was operating at $I_D = 100\,\mu A$ and $I_D = 250\,\mu A$ respectively. Consistently with the 110 nm technology, this can be related to the larger impact of noise associated with the lateral parasitic transistors at small I_D density [15].



(a) $I_D = 100\,\mu A$. **(b)** $I_D = 250\,\mu A$.

Figure 1.29: Noise Voltage Spectrum before and after 200 and 600 Mrad of TID of NMOS device with $W/L = 200/0.35$ belonging to 65 nm CMOS technology.

The effect of 1/f noise increase can be nonnegligible. As already metioned in section 1.1.5, the gate referred noise voltage spectrum of a MOSFET device $S_e^2(f)$ can be modeled by the sum of two components, white noise $S_W^2(f)$ and 1/f noise $S_{1/f}^2(f)$, i.e. equation (1.12): $S_e^2(f) = S_W^2 + S_{1/f}^2(f)$. Figure 1.30 shows the ratio between $S_{1/f}^2(f)$ after and before the irradiation. It is possblie observe that at 600 Mrad the 1/f noise coefficient increases by about a factor 3 at low currents (70% increase of the contribution to the ENC of a detector readout channel). The lowering of 1/f noise contibution from 10 Mrad to higher doses can be explained by the fact that at very high doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge, switching off lateral parasitic transistors. Thus, noise contributions by these parasitic devices become less important. The 1/f noise increase from 200 Mrad to 600 Mrad can be explained by other effects, such as the increase of border traps in gate oxides or defects in spacer dielectrics.

For what concernes PMOSFET devices, figures 1.31a and 1.31b show the typical behavior before and after irradiation up to 200 Mrad to 600 Mrad. Again no effect is

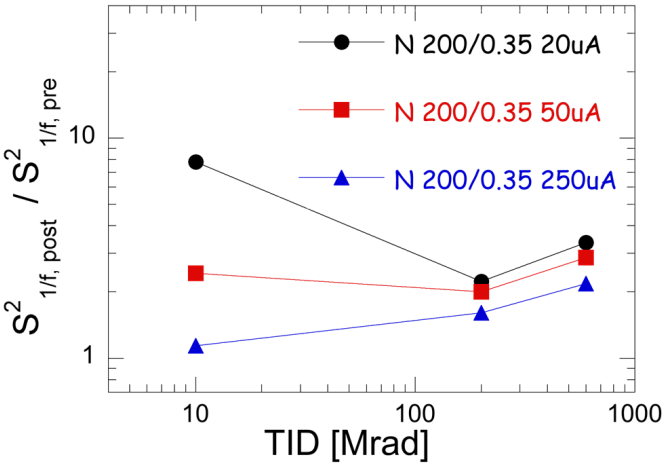
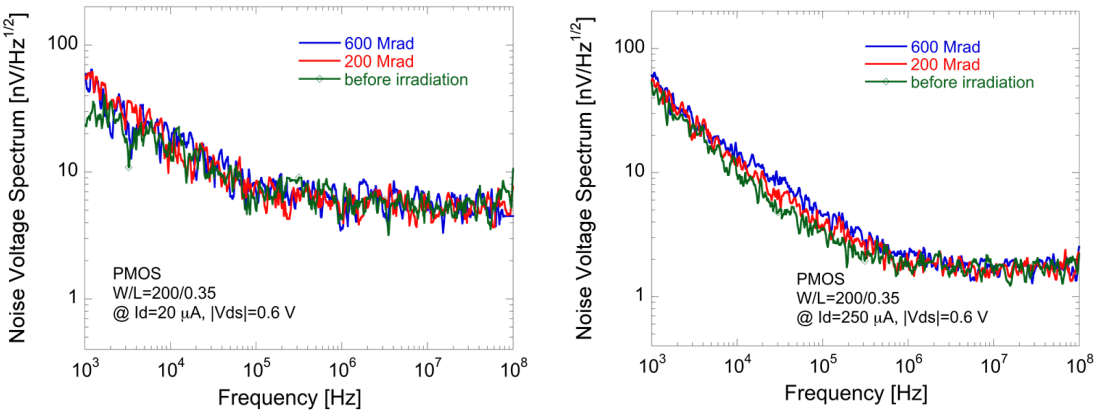


Figure 1.30: $S^2_{1/f,post}/S^2_{1/f,pre}$ with respect to TID of an NMOS with $W/L = 200/0.35$ belonging to the 65 nm technology at $I_D = 20, 50$ and 250 µA.

detected in the white noise region, whereas 1/f noise moderately increases. Unlike NMOS devices, lateral parasitic devices do not play a role here. Positive charge is accumulated both in oxides and at interface states, so there is no dependence on the drain current density.



(a) $I_D = 20$ µA. **(b)** $I_D = 250$ µA.

Figure 1.31: Noise Voltage Spectrum before and after 200 and 600 Mrad of TID of PMOS device with $W/L = 200/0.35$ belonging to 65 nm CMOS technology.

Like NMOS, also for PMOS the effect of 1/f noise increase can be nonnegligible. Figure 1.32 shows the ratio between $S^2_{1/f}(f)$ after and before the irradiation. It is possblie observe that at 600 Mrad the 1/f noise coefficient increases by about a factor 2 (40% increase of the contribution to the ENC of a detector readout channel). Unlike 110 nm technology no Lorentzian component is visible after irradiations.

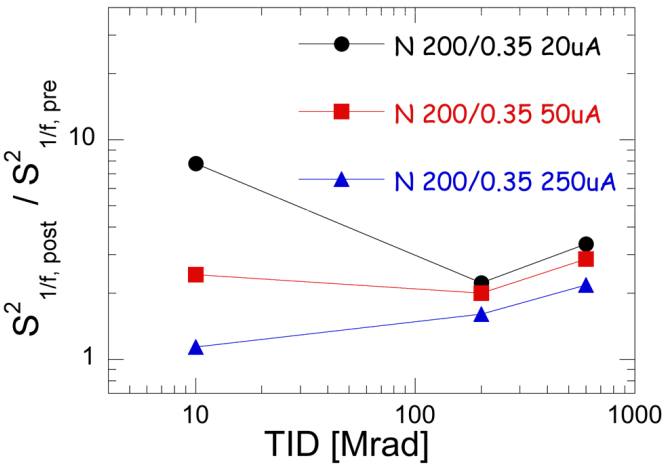


Figure 1.32: $S^2_{1/f,post}/S^2_{1/f,pre}$ with respect to TID of an PMOS with $W/L = 200/0.35$ belonging to the 65 nm technology at $I_D = 20, 50$ and $250\,\mu A$.

1.6 Discussion

A set of test devices in the 110 nm technology and in the 65 nm technology were irradiated up to 5 Mrad and 600 Mrad and their behavior after irradiation was studied, especially focusing on the noise performance.

It is possible to conclude that for what concernes 110 nm technology a large degree of tolerance up to Total Ionizing Dose of 5 Mrad is observed. This behaviour might be ascribed to their thin gate oxide. Little threshold voltage shift and negligible transconductance decrease were detected either for Core, Enclosed Layout and I/O devices. Despite there was almost no change in static characteristics, it is possible to observe a degradation of the low-frequency noise. In particular at 5 Mrad, PMOSFET devices show a Lorentzian noise term, instead NMOSFETs exhibit a moderate increase of 1/f noise at low current density. Overall, these result lead to the conclusion that this technology is suitable for the design of analog circuits with a good degree of radiation tolerance up to first step of 5 Mrad total dose. Further irradiation steps are programmed in order to study effects up to 10 Mrad and 50 Mrad TID.

On the other hand, 65 nm devices show a good degree of tolerance to ionizing radiation up to a total dose of 600 Mrad. Negligible transconductance increase was detected for all devices. A threshold voltage shift lesser than 40 mV is detected. With increasing TID, NMOS devices show $I_D - V_{GS}$ characteristic moving in different directions. This effect can be ascribed to the fact that at low TID, positive charge in STI oxides switches on lateral devices, increasing I_D for the same V_{GS} and reducing the threshold voltage value. At higher doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge, switching off lateral parasitic transistors and reducing I_D for the same V_{GS}, increasing the threshold voltage value. For both NMOSFET and PMOSFET no effect is detected in the white noise region. On the contrary, the effect of 1/f noise increase can be nonnegligible both for N-channel and P-channel devices. In particular, for what concerns NMOS devices, at 600 Mrad the 1/f noise coefficient increases by a factor 3 at low currents. Regarding PMOS devices, at 600 Mrad the 1/f noise coefficient increases by about a factor 2. Unlike 110 nm technology no Lorentzian component is visible after irradiations. Such results, in particular the flicker noise increase, can explain results obtained with chips designed in 65 nm CMOS technology in the frame of the RD53 and CHIPIX65 collaborations [16] [17]. A further irradiation step is programmed in order to study effects up to a Total Ionizing Dose of 1 Grad.

2 Design of the Charge Sensitive Amplifier for the GAPS experiment

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The two towering problems of early 21^{st} century physics are the nature of Dark Matter (DM) and Dark Energy (DE). Physicists believe that the 85% of the matter in the known universe is something called *Dark Matter*. Unlikely "normal matter", dark matter is very hard to detect due to the nature of its interactions, infact it does not emit electromagnetic radiation, but it is possible to observe only its gravitational effects. This means that most of the matter in the universe is not the kind we have been studying for centuries, in fact ordinary matter is only 5% of the matter and energy in the known universe.

Dark Matter existence was first proposed in the 1920s and first taken seriuosly in the 1960s when astronomers noticed that galaxies were spinning faster than the calculations predict, using only the "normal matter". In order to explain such high rotational speed a huge amount of mass have to be added to the calculations. Another important clue to confirm the existence of Dark Matter is called *gravitational lensing*. This phenomena is the observation of the same galaxy in two distinct space coordinates: it can be explained by the presence of a massive object able to bend light trajectory by means of its gravitational field, as shown in figure 2.1.

The General AntiParticle Spectrometer (GAPS) is a balloon experiment with a

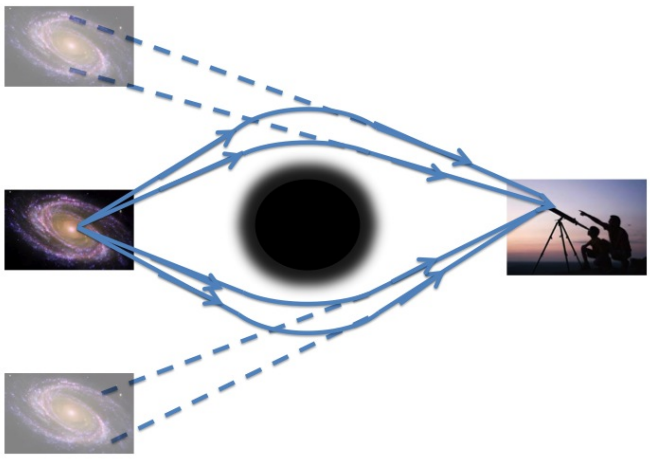

Figure 2.1: Gravitational lensing basic scheme.

novel approach for indirect dark matter searches that exploits cosmic antideuterons. It is a collaboration of many Universities and Institutions, such as Columbia University, Massachusetts Institute of Technology, California Universities Berkley and Los Angeles, and the italian INFN ("Istituto Nazionale di Fisica Nucleare"). The balloon launch is expected by the end of year 2020 from the McMurdo station in Antartica and the launch is approved by NASA. GAPS will utilize a high-altitude balloon to look for low energy antideuteron particles (with energy per nucleon $< 0.3\ ^{GeV}/_{n}$). Astrophysically produced antideuterons have never been detected and so the unambiguous detection of even a single event would be very significant. Antideuterons could be a tell-tale signature of dark matter annihilations, because they may be produced when Cold Dark Matter(CDM) particles annihilate in the galactic halo.

Weakly Interacting Massive Particles (WIMPs) are the leading candidates for cold dark matter and antideuterons are predicted to be generated in WIMP–WIMP annihilation in a broad class of theories invoking beyond Standard Model physics. WIMPs generating antideuterons are found in various supersymmetric and supergravity theories.

It is possible to observe that the antideuteron flux produced by cosmic ray collisions with the interstellar medium (secondary flux) falls sharply at low energy, whereas the antideuteron flux produced by WIMP–WIMP annihilation (primary flux) is predicted to have a maximum at low energy [18]. Thus, a low energy search for antideuterons should provide a clean signature for dark matter, since the primary antideuteron flux completely dominates the secondary antideuteron flux, as illustrated in figure 2.2 [19]. The other dark matter annihilation products such as antiprotons, electrons, γ-rays, neutrinos, etc., are confounded by conventional astro-

physical backgrounds. The expected primary antideuteron flux for three dark matter candidates, i.e. a neutralino (LSO) in a $b\bar{b}$ decay mode, a lightest Kaluza-Klein particle (LKP) and a right-handed neutrino (LZP) in universal extra dimension model, and the predicted secondary antideuteron flux are shown in figure 2.2. Such figure reports also a comparison between experiment GAPS sensitivity and other antideuteron detector experiments such as BESS (balloon-based superconducting magnet) and AMS (Alpha Magnetic Spectrometer).

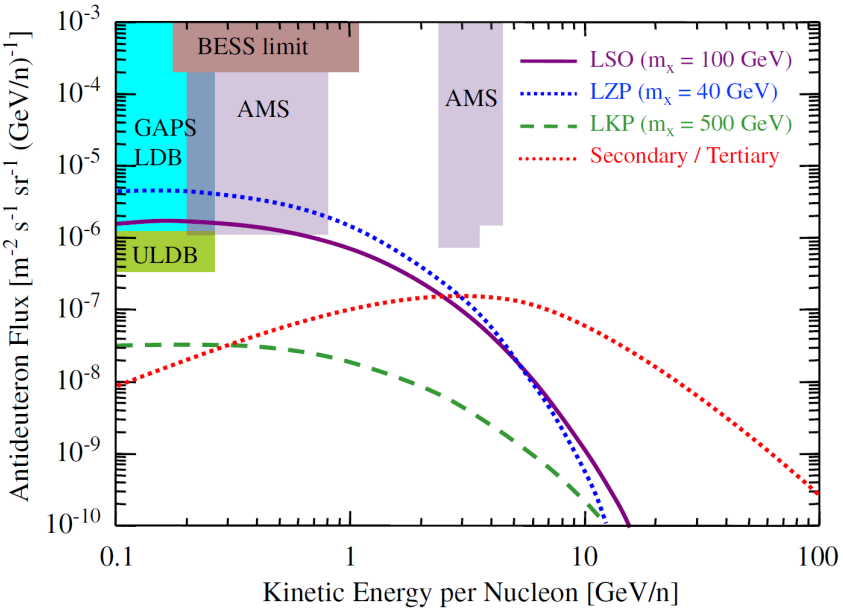

Figure 2.2: Antideuteron flux at the top of the atmosphere, compared with the BESS upper limit, and GAPS and AMS sensitivity.

The GAPS detection method involves the time of flight (TOF) technique: makes it possible to discriminate between a lighter and a heavier elementary particle of same momentum using their time of flight between two scintillators.

The signals generated by all detectors in response to the incident radiation must be suitably amplified and filtered to optimize the signal-to-noise ratio before sending them to the digital section. This task is carried out by an analogue channel which includes a preamplification stage and a shaping stage, followed by stages that allow for further signal processing.

The detection of the exotic GAPS atoms has already been successfully tested by the KEK accelerator in 2004 and 2005. In order to test the appropriate GAPS hardware, a balloon with a prototype consisting of a 6-detector system was launched in June 2012 from the Taiki base in Japan by the JAXA space agency [20]. The channel readout circuit of this prototype, referred to as pGAPS, was composed by a discrete preamplifier and commercial devices for the rest of the processing chain,

i.e. a shaper and a multi-channel analyzer.

Normally, the readout electronics is located as close to the detector as possible. In the GAPS experiment, the detectors are in a cryostat at temperature $T = -50\,°C$. The disadvantage of a discrete readout chain is that it dissipates too much power, causing a rise in temperature. To overcome such problem, it would be better to put the electronics out of the cryostat, but this goes against the principle of having the electronics nearby the detector. Furthermore, there would be a very high number of cables for signal transmission (approximately 1350 x 4 cables). The solution of an integrated electronics, on the other hand, is excellent from this point of view. An IC circuit dissipates little power, allowing to put everything in the cryostat. Moreover it would be possible to serialize the outputs of multiple channels so there would be a few cables out of the cryostat. In GAPS collaboration, two different solution will be studied in parallel:

- hybrid analog channel, with a discrete preamplifier followed by an IC stage for the filtering and shaping of the signal;
- fully CMOS analog channel.

This thesis work is focused on the development of the first front-end IC analog block: the Charge Sensitive preAmplifier.

2.1 Readout Channel for the GAPS Tracker Detector

In what follow a brief introduction on the GAPS detector and its readout channel is given.

2.1.1 Time Of Flight and Tracker Detector structure

The GAPS detection method involves capturing antiparticles into a target material with subsequent formation of an excited exotic atom. The exotic atom de-excites in a complex process involving Auger ionization and electron refilling in high quantum number states, followed by the emission of X-rays from the lower quantum states. Ultimately the antiparticle is captured by the nucleus, where it is annihilated with the emission of pions and protons. This process is illustrated in figure 2.3. The entire course of events takes place in less than a few nanoseconds. With known atomic number of the target, the Bohr formula for the photon energy uniquely determines the mass of the captured antiparticle.

GAPS will employ a tracking geometry with 13 layers (2 m $\times$ 2 m) of Si(Li) detectors surrounded by time-of-flight plastic scintillators. Each Si(Li) detector (4

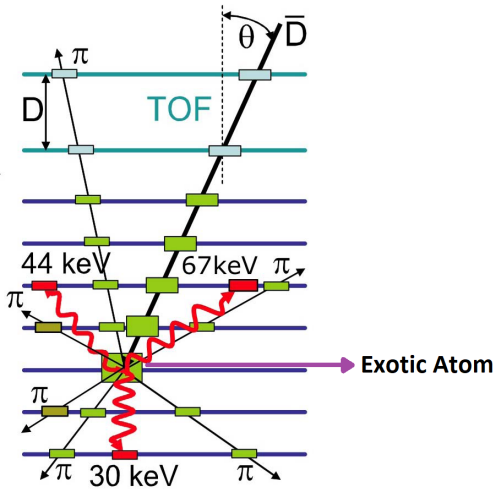

Figure 2.3: Schematic for GAPS detection method. An antiparticle slows down and stops in the Si(Li) target forming an exotic atom. The atomic X-rays will be emitted as it de-excites followed by the pion (and proton) emission in the nuclear annihilation.

in. diameter, 2.5 mm thick) is segmented into eight or four strips and adjacent tracking layers have their strips positioned orthogonally, which provides modest three-dimensional tracking. Since strips are relatively small, $\sim$ 1 cm wide, X-rays and charged particles can be detected separately in the different strips/channels. The tracking geometry can count the number of particles produced in the nuclear annihilation and separately identify atomic X-rays from particle tracks. It also permits direct measurement of particle stopping depth and naturally conforms to the multi-detector geometry. Each Si(Li) layer also works as a degrader and a target material to slow down the incoming antiparticle and to form an exotic atom. The X-rays and the number of pions and protons emitted from the exotic atom uniquely identify the mass of the antiparticle, as do the depth of absorption and the $^{dE}/_{dx}$ loss in the Si(Li) layers, once the antiparticle velocity is determined by time-of-flight. Antiprotons, which can also form exotic atoms and emit atomic X-rays and charged particles, are a major background, but simulations for the experimental design show that antideuterons can be distinguished from antiprotons using background rejection techniques with the required rejection factor of $> 10^6$.

When X-rays come into the intrinsic region and interact with the silicon lattice, electron-hole pairs will be created. The number of created electron-hole pairs is proportional to the deposited energy. These electrons and holes will be separated by the applied reverse bias and collected into the charge sensitive preamplifier. Consequently to this shift of charges a current signal is generated. Some essential particle informations, such as the initial energy, the arrival time and the trajectory, can be

obtained from the readout and subsequent process of such signal.

Normally, in this type of detector, charge collection takes place in the order of ten nanoseconds, generating a current pulse of equal duration. This pulse must be processed by the front-end electronics connected to the detector. From the description of the detector, there is therefore the problem of creating an analog readout channel, which makes it possible to read the charge produced by the detector with the best possible accuracy.

According to what has been already described above, a detector can be modeled as a current generator that generates a charge pulse whose value is proportional to the detected particle energy. Moreover, since the reverse polarized junction has a capacitive behavior, the model must also include a capacitance C_d that identifies the sensor capacitance, as shown in figure 2.4.

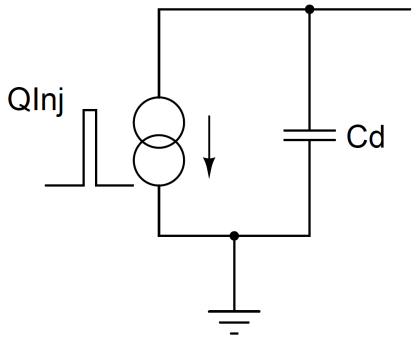

Figure 2.4: Ideal semiconductor detector model.

The energy pulse can be simulated with a current signal having the trend shown in figure 2.5, with a *Rise Time (t_r)* and a *Fall Time (t_f)* that can be choosen equal to 1 ns and a pulse duration (t_d) equal to 9 ns. In this way the charge injected by the detector, in Coulomb, is given by the equation:

$$Q_{inj} = I_A \cdot (t_r + t_d) = I_A \cdot 10\,\text{ns} \tag{2.1}$$

where I_A is the pulse amplitude. The number of electrons-holes pair producted can be obtained dividing Q_{inj} by elementary charge $q = 1.6 \cdot 10^{-19}\,\text{C}$. In order to express the injected current as a function of the detected energy, it has to be taken into account that the needed energy to produce one electron-hole pair in Si is 3.6 eV, thus:

$$I_{inj} = 4.43 \cdot 10^{-9} \times E \tag{2.2}$$

where E is the energy expressed in keV and $4.43 \cdot 10^{-9}\,{}^{\text{A}}/_{\text{keV}}$ is the result of ${}^{(q \cdot 1000)}/_{(10\,\text{ns} \cdot 3.6\,\text{eV})}$

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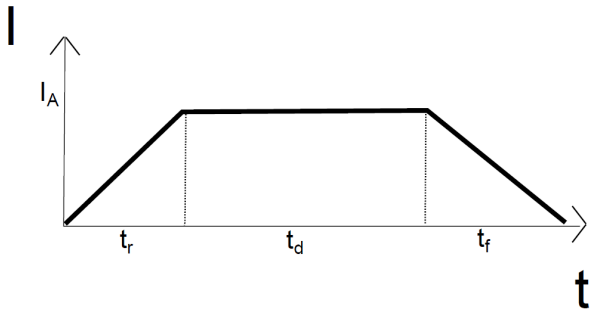


Figure 2.5: Ideal detector current pulse.

The energy range expected in GAPS is very wide. It goes from 10 keV to 50 MeV, thus the analog channel must be able to keep a good signal to noise ratio in all this range, eventually changing the gain from low energy to high energy. In fact at low energies X-rays emitted from the exotic atoms will be detected, whereas in the high energy range annichilation products such as pions and protons will be detected. In order to satisfy such request a signal compression technique will be adopted and discussed later.

The gain in low energy is expected to be at least $\sim 100\,{}^{\mu V}/_{keV}$, whereas in the high energy region this gain can be lowered to $\sim 5\,{}^{\mu V}/_{keV}$.

2.1.2 Analog readout channel

The analog channel captures the signal from each single detector strip in order to extract informations about the incident particles. The block diagram of the developed channel in this thesis for the GAPS experiment is shown in the figure 2.6.

The first block is the **Charge Sensitive Amplifier (CSA)**, which has the function of converting the current pulse, generated in the detector, to an output voltage step whose amplitude is proportional to the injected input charge value. The second stage is the **Shaper**, which has the function of filtering the output signal of the amplifier in order to optimize the signal-to-noise ratio. In this readout channel, a $CR-(RC)^2$ semigassian filter of the second order is adopted. It is obtained by deriving the input signal once and integrating it twice. The order of the filter has been chosen as a trade-off between the occupancy area and the Signal to Noise ratio. After the shaper, there are the **Threshold Circuit** and the **Comparator**, which compares the output signal with a reference voltage. The analog channel ends with a control switch called **kill**, which has the function of disabling the channel when it is necessary.

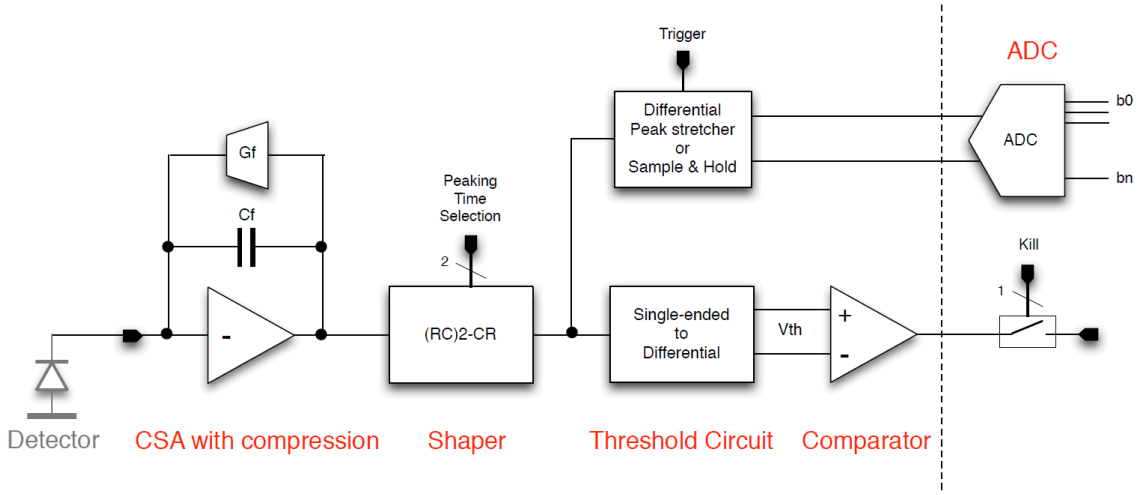


Figure 2.6: Ideal detector current pulse.

The channel has been designed in order to maximize the signal-to-noise ratio $^{S}/_{N}$. In this type of application, the low noise characteristics must be guaranteed in order to obtain a resolution of at least 4 keV in the low energy range. The signal-to-noise ratio optimization can be obtained by estimating the *equivalent noise charge (ENC)*, a parameter that must be calculated throughout the chip development process. ENC has to be considered especially during the design of the preamplifier circuit, infact, in a well-designed system, the preamplifier itself is the element that contributes most to the input noise [25].

2.2 Charge Sensitive Amplifier

The Charge Sensitive Amplifier stage has the function of integrating the charge pulse generated in the detector, Q, by means of the feedback capacitance C_f and converting it into a voltage step of magnitude equal to $\frac{Q}{C_f}$. The CSA must meet two basic requirements:

- provide as low noise as possible;
- provide an output as near as possible to an ideal step.

For this latter requirement, it is necessary to impose that the recovery time, i.e. the time necessary for the restore the feedback capacitance, is sufficiently long with respect to the time needed from the stages following the CSA to process the signal, i.e. peaking time t_p. Furthermore the response time of the CSA t_{res}, i.e. the rise time of the signal, has to be much shorter than the peaking time: $t_{res} \ll t_p$.

The CSA consists of a high-gain inverter amplifier whose feedback stage is composed by:

- a CMOS capacitance;
- a transconductance stage.

The first one has to be able both to integrate the current pulse and set the gain of the preamplifier. The second one has the task of fixing the DC operating point and providing a discharge path for the charge accumulated in the CMOS capacitance.

The simplest model of a detector is described by a pulse generator with amplitude Q_{inj}, equal to the amount of detected charge, so the input signal to the CSA is given by the following equation:

$$I(t) = \delta(t) \cdot Q_{inj} \tag{2.3}$$

Figure 2.7 shows a simplified scheme of the CSA with the charge pulse input given by the detector. The preamplifier transfer function is described by the following

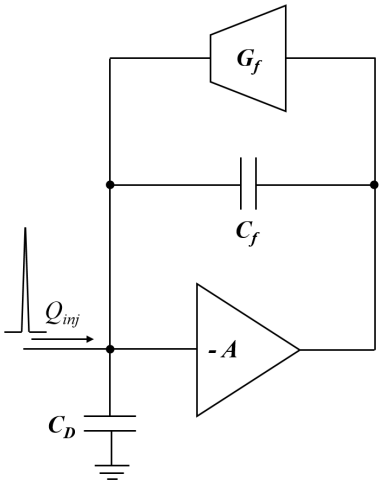


Figure 2.7: Simplified scheme of the Charge Sensitive Amplifier.

equation:

$$V_{out}(s) = -\frac{I(s)}{\frac{sC_D}{A} + sC_f(\frac{1}{A}+1) + G_f + \frac{G_f}{A}} =$$
$$V_{out}(s) = -\frac{1}{\frac{sC_D}{A} + sC_f(\frac{1}{A}+1) + G_f + \frac{G_f}{A}} \cdot Q_{inj} \tag{2.4}$$

where G_f is the transconductance value. Evaluating equation (2.4) for $A \to \infty$, the output voltage becomes:

$$V_{out}(s) = -\frac{Q_{inj}}{sC_f + G_f} \tag{2.5}$$

It is possible to obtain the amplifier responce in the time domain by applying the inverse Laplace transform to equation (2.5):

$$v_{out}(t) = -\frac{Q_{inj}}{C_f} e^{-t/\tau} \tag{2.6}$$

where $\tau = \frac{C_f}{G_f}$. Equation (2.6) points out that the preamplifier response to a pulse is a step decreasing exponentially with a time constant τ. The time constant τ of the CSA has to be greater than the peaking time t_p of the shaper in order to approximate the output of the preamplifier to a step voltage. This stage sensibility is $\frac{1}{C_f}$, thus the amplitude of the CSA output voltage step is $\frac{Q_{inj}}{C_f}$.

In the present implementation the feedback capacitance consists of an NMOS device acting as a compressing element. This solution has been adopted in order to meet the required specifications. As already said, in the low energy range a gain of $\sim 100\,\mu\text{V}/\text{keV}$ is needed and, in this case, the range of $0 - 50\,\text{MeV}$ would imply an output range of 5 Vwhich exeeds the the maximum power supply voltage of the chosen technology, 1.8 V. To comply with this requirement, a non-linear characteristic of the front-end is required. The solution adopted in this work is based on the dynamic signal compression technique which exploits the non-linear features of an inversion-mode MOS capacitor [26]. Knowing that the detector collects electrons, i.e. negative charges and a positive step, for a correct functioning of the feedback capacitance, the drain and source of the device are shorted together to form one capacitor terminal and connected to the input of the circuit, whereas the gate is connected to the output of the circuit. The value of the resulting capacitance, denoted here as C_{GS}, depends on the voltage between the gate and the source-drain terminal V_{GS} and varies non-linearly as the MOSFET is biased through accumulation, depletion and inversion region. In order to obtain a monotonic function of C_{GS} the transistor must not enter in the accumulation region for all V_{GS} values. Normally, such condition can be satisfied connecting, in case of an NMOS device, the bulk to the lowest voltage available in the circuit (i.e. the ground reference), whereas, in case of a PMOS device, the n-well to the highest voltage (the power supply V_{DD}). In both configurations, the devices can only operate in inversion mode. Figure 2.8 shows the $C_{GS} - V_{GS}$ characteristic for a device operating in inversion mode. For $0 < V_{GS} \ll V_{Th}$ the value of C_{GS} is minimum and it is mainly due to the overlap of the gate dielectric with the source and drain diffusions. Therefore, it can be modeled by means of the following equation:

$$C_{GS,min} \approx C_{ov} = \varepsilon \frac{2W\Delta L}{t_{ox}} \tag{2.7}$$

where $\varepsilon = \varepsilon_0 \varepsilon_r$ is typical of the material, ΔL is the overlap of the dielectric gate with the source diffusion and W is the gate width. Characteristic in figure 2.8 is monotonic and presents a sharp increase when gate to source voltage V_{GS} value is approximately equal to the threshold voltage V_{Th} value. For $V_{GS} \gg V_{Th}$ a conductive channel appears under the gate oxide and, consequently, C_{GS} reaches its maximum value which is mainly given by the gate-to-channel capacitance:

$$C_{GS,max} = \varepsilon \frac{WL}{t_{ox}} \tag{2.8}$$

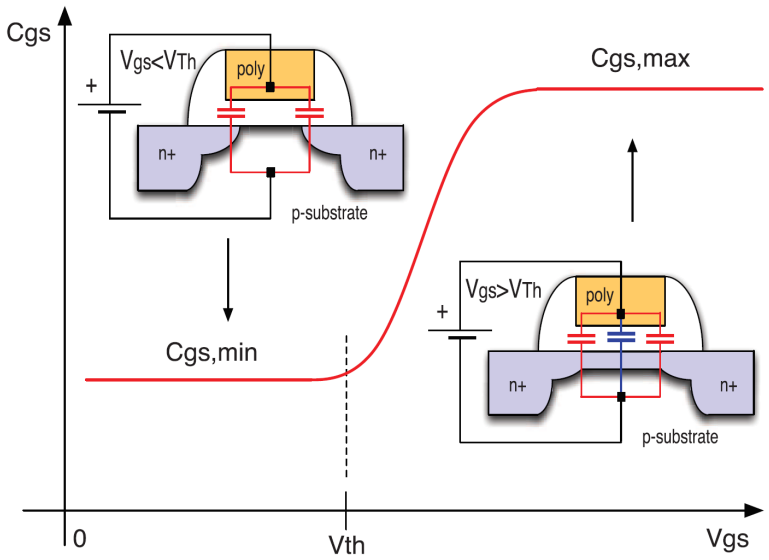


Figure 2.8: Qualitative behaviour of the C_{GS} capacitance as a function of the V_{GS} voltage for an inversion-mode NMOS capacitor with fixed gate width W. The substrate contact (not shown) is at ground.

Figure 2.9 shows the CSA sensitivity that is inversely proportional to C_{GS}. The gain of the Charge Sensitive Amplifier is not constant any more and depends on the value of the injected charge Q_{inj}, in particular in the low energy range a high gain is obtained, whereas in the high energy range the CSA has a lower gain.

Knowing the trend of the CSA sensitivity, the Transfer Function (TF) $V_{out} - Q_{inj}$ is espected to show two different slopes, higher in low energy range and lower in high energy range. An example of the expected transfer function is reported in figure 2.10. Given the very large expected energy range, a gain of $0.2\,^{\mathrm{mV}}/_{\mathrm{keV}}$ for $0 < E < 1\,\mathrm{MeV}$ and $6\,^{\mu\mathrm{V}}/_{\mathrm{keV}}$ for $1\,\mathrm{MeV} < E < 50\,\mathrm{MeV}$ has been initially hypotesized. Such conditions would lead to an output voltage in the range from 0 to 0.5 V. As will be seen in the following sections the used technology (180 nm) is characterized by showing high threshold voltage. This can be a problem, infact, if V_{Th} is too high,

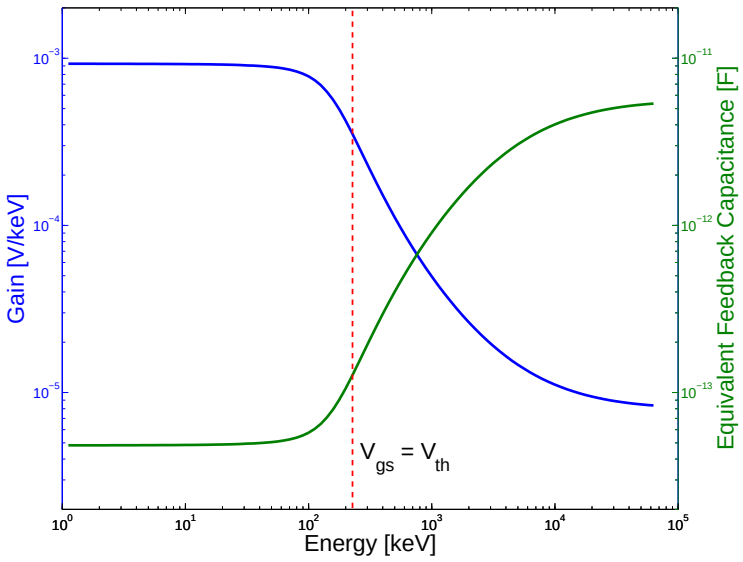


Figure 2.9: Qualitative behaviour of the CSA sensitivity and C_{GS} capacitance as a function of the V_{GS} voltage for an inversion-mode MOS capacitor.

the *kink*, i.e. the point where the change in the slope occurs, could be at a voltage value too high implying a maximum output voltage higher than 500 mV. In order to overcome such a problem, it was chosen not to connect the bulk of the feedback NMOS capacitance to the lowest voltage available in the circuit, but to the same voltage of drain and source. In this way a lower threshold voltage value is obtained.

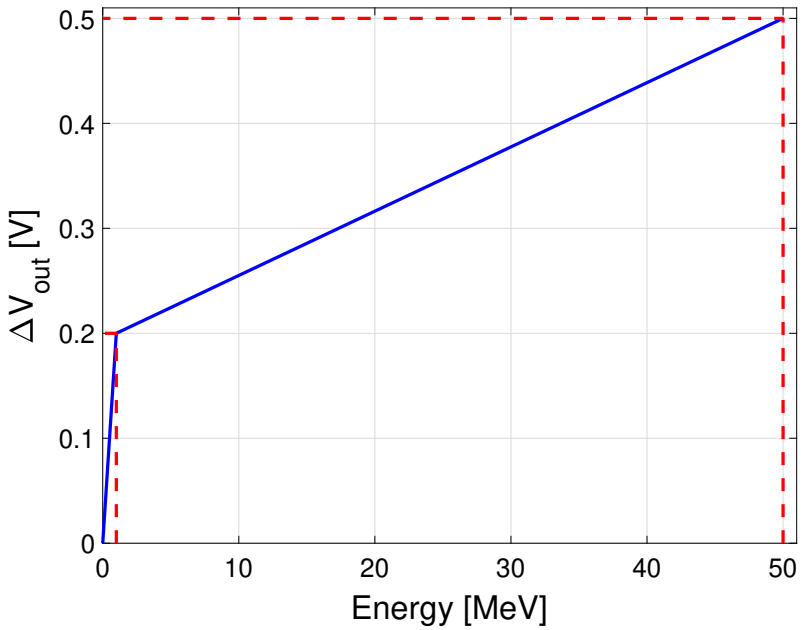


Figure 2.10: Ideal transfer function FdT of the GAPS charge-sensitive preamplifier.

In this section the CSA schematic and DC operating point will be presented. As reported in Figure 2.11, the Charge Sensitive Amplifier is comprised of by three stages:

- the forward gain stage;
- the feedback MOS capacitance;
- the transconductance feedback stage.

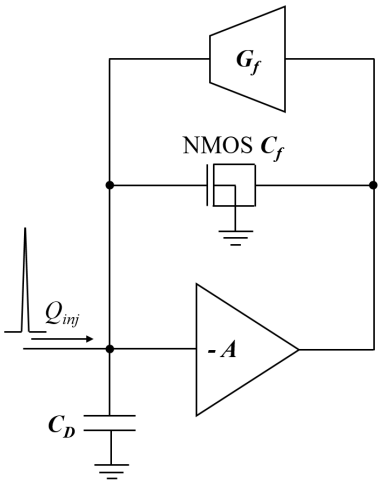


Figure 2.11: CSA block diagram.

In what follows each block will be discussed in detail.

2.2.1 CSA forward gain stage

As shown in Figure 2.12 the forward gain stage of the Charge Sensitive Amplifier is composed by an active folded cascode (composed by T_1, T_2 and T_0 as the input device) with local feedback (by means of device T_3), loaded by an active cascoded load (composed by T_5, T_6 and T_7).

The overall area of the preamplifier is $\sum(W \times L) = 2880\,\mu m^2$, with the input device T_0 dimension $(W/L)_{in} = 3\,mm/540\,nm$. The dimensioning of input device and choice of input device current value are discussed in the Equivalent Input Noise section 2.2.5.

Transistor T_0 is the input transistor, which is connected to a current buffer, represented by the PMOS T_2. This is a folded-cascode configuration with the input transistor connected to a folded PMOS, instead of being stacked over a further NMOS. This structure does not bring advantages from the point of view of the signal gain, infact the equations of such stage are the same ones of a normal cascode

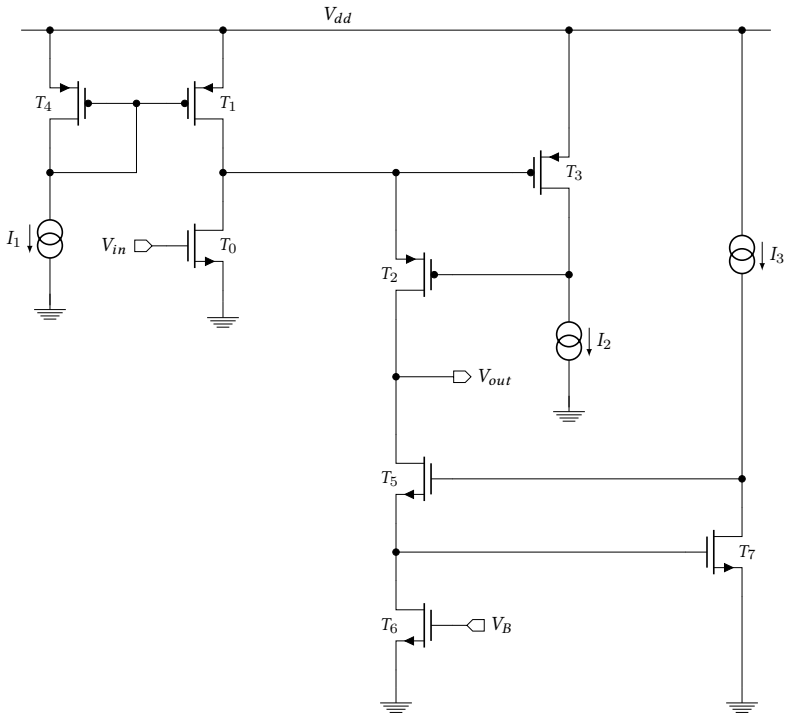


Figure 2.12: Charge Sensitive preAmplifier: folded-cascode schematic.

stage, but allows the correct dc polarization of the stage. With the MOS stack configuration there would be a problem of dynamic output, that can be too wide. On the contrary, using a folded-cascode configuration with the same bias voltage, only two transistors need to be supplied. The circuit shown in Figure 2.12also includes two local feedback composed by PMOS T_3 and NMOS T_7. Such feedbacks have basically the advantages of increasing the impedance seen by the drain of T_5 and the one seen by transistor T_2, extending both bandwidth and gain of the stage itself.

In order to proceed with a quantitative analysis for small signal, a few approximations are needed. The amplifier voltage gain can be expressed as the product between the transconductance of the input device and the impedance seen at the output node. The latter can be calculated by taking into account two parallel impedance paths:

- the resistance of T_5 drain, which includes transistors T_5, T_6 and T_7;
- the resistance of T_2 drain, which includes transistors T_2, T_0, T_1 and T_3.

The impedance seen at T_5 drain is much higher than the one seen at T_2 drain,

therefore, the gain of the stage can be calculated with the following equation:

$$\frac{V_{out}}{V_{in}} = g_{m_0} R_{DD_{out}} \tag{2.9}$$

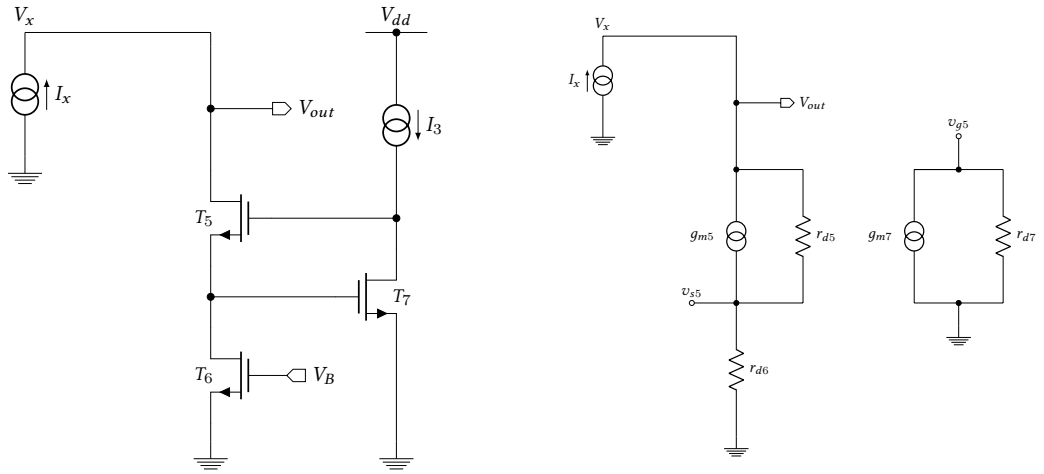
where g_{m_0} is the transconductance of the input device and $R_{DD_{out}}$ represents the impedance seen at the output node, that is the parallel of the impedance seen at T_2 drain the impedance seen at T_5 drain.

Output impedance evaluation

The impedance at the output node can be evaluated by referring to the small signal model, shown in Figure 2.13b:

$$R_{DD_5} = \frac{1}{g_{ds6}} + \frac{1}{g_{ds5}} + \frac{g_{m5}}{g_{ds5} g_{ds6}} \left(1 + \frac{g_{m7}}{g_{ds7}}\right) \tag{2.10}$$

Table 2.1 shows the MOS parameters, provided by simulation models. With these



(a) Folded-cascode active load schematic.

(b) Folded-cascode active load small signall model.

Figure 2.13: Charge Sensistive preAmplifier folded-cascode active load.

values, an output node impedance of $R_{DD_5} \approx 37\,\mathrm{M\Omega}$ is obtained.

Small Signal Analysis

From the schematic of the folded-cascode circuit, shown in figure 2.12, it is possible to obtain the small signal model, reported in figure 2.14.

	$g_m[\mu A/V]$	$g_{ds}[\mu A/V]$
T_5	3217	173
T_6	539	54
T_7	60	0.6

Table 2.1: Folded-cascode active load parameters.

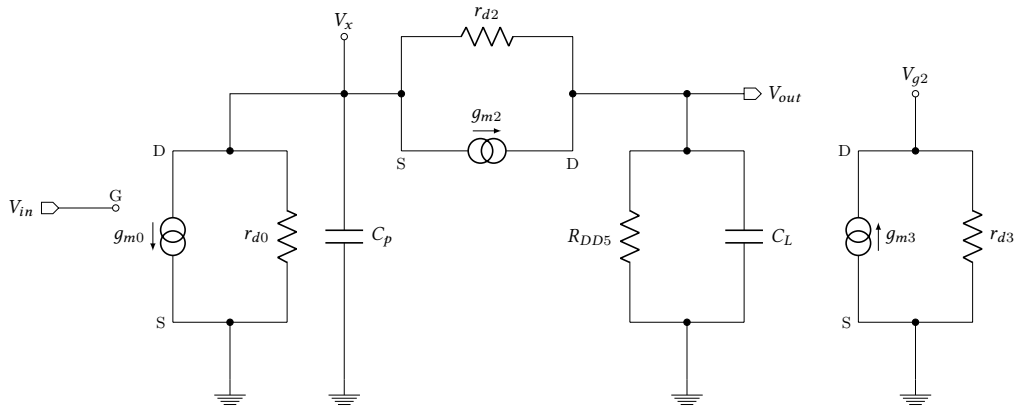


Figure 2.14: Charge Sensitive preAmplifier: model for small signal.

In order to determine the static gain of the stage a low frequency analysis is performed. Some intial hypotheses have to be set. Fisrt of all, the input device channel resistance is the result of two resistor in parallel: T_0 device r'_{d0} and T_1 device r'_{d1}, thus $r_{d0} = r'_{d0}//r'_{d1}$. The same approximation has to be adopted also for transistor T_3: in the simplified schematic reported in figure 2.12, a current source polarizes the transistor, but actually another transistor will polarize T_3. Last, but not least, all capacitances will be treated as an open circuit.

Drain voltage on transistor T_3 is:

$$v_{d3} = v_{g2} = -g_{m3} r_3 v_x = -\frac{g_{m3}}{g_{ds3}} v_x \tag{2.11}$$

Voltage drain v_x of the input device can be obtained allpying Kirchhoff's circuit laws in nodes v_x and v_{out} [28].
Node v_x:

$$g_{m2} v_{in} + \frac{v_x}{r_{d0}} = \frac{v_{out} - v_x}{r_{d2}} - g_{m2} \left(1 + \frac{g_{m3}}{g_{ds3}}\right) v_x \tag{2.12}$$

Node v_{out}:

$$g_{m2}v_{sg2} = \frac{v_{out} - v_x}{r_{d2}} + \frac{v_{out}}{R_{DD_5}}$$
$$g_{m2}\left(1 + \frac{g_{m3}}{g_{ds3}}\right)v_x = \frac{v_{out} - v_x}{r_{d2}} + \frac{v_{out}}{r_{DD_5}} \tag{2.13}$$

Calling $g_{m3}/g_{ds3} = A$, v_x can be expressed by means of the following eqaution:

$$v_x = \frac{r_{d2} + R_{DD_5}}{R_{DD_5}\left(1 + g_{m2}r_{d2}\left(1 + A\right)\right)}v_{out} \tag{2.14}$$

thus ratio between input and output of the folded-cascode will be:

$$\frac{v_{out}}{v_{in}} = -g_{m0}\left(\frac{r_{d0}\left(1 + g_{m2}r_{d2}\left(1 + A\right)\right)R_{DD_5}}{r_{d0} + r_{d2} + r_{d0}g_{m2}r_{d2}\left(1 + A\right) + R_{DD_5}}\right) \tag{2.15}$$

The impedance seen at the drain of T_5 is much larger than the other impedances, thus the equation 2.15 can be simplified in the following form:

$$v_{out} = -g_{m0} \cdot r_{d0}\left[1 + \frac{g_{m2}}{g_{ds2}}\left(1 + \frac{g_{m3}}{g_{ds3}}\right)\right]v_{in} \tag{2.16}$$

and knowing that:

$$R_{DD_2} = r_{d0}\left[1 + \frac{g_{m2}}{g_{ds2}}\left(1 + \frac{g_{m3}}{g_{ds3}}\right)\right]$$
$$R_{DD_2} \approx r_{d0}\frac{g_{m2}}{g_{ds2}}\frac{g_{m3}}{g_{ds3}} \tag{2.17}$$

From equation (2.17), the obtained R_{DD_2} is $\sim 28\,\mathrm{M\Omega}$, thus the output impedance results:

$$R_{DD_{out}} = R_{DD_5}//R_{DD_2} \approx R_{DD_2} \tag{2.18}$$

Table 2.2 shows the MOS parameters, provided by simulation models. With such values the ouput resistance is $R_{DD_{out}} \approx 15\,\mathrm{M\Omega}$. It is possible to obtain output

	$g_m[\mu A/V]$	$g_{ds}[\mu A/V]$
T_0	44610	242
T_1	6200	147
T_2	1850	70
T_3	100	00.34

Table 2.2: Folded-cascode and local feedback parameters.

voltage expression:

$$v_{out} = -g_{m0} R_{DD_o ut} v_{in} \tag{2.19}$$

Thus, the calculated the forward gain stage is equal to $A_v \approx 116\,\text{dB}$.

Source impedance T_2 Evaluation The impedance seen from the source terminal of transistor T_2 can be calculated, referring to the simplified scheme in 2.15. The gain A of the op-amp in the figure corresponds to the local feedback gain realized by the transistor T_3, i.e. $v_2 = -Av_x = g_{m3} r_{d3} v_x$. Using small signal model it is possible to express the source impedance by means of the following equation:

$$\begin{aligned} r_x = \frac{v_x}{I_x} = R_{S2} &= \frac{r_{d2} + R_{DD_5}}{1 + g_{m2} r_{d2} (1 + A)} \\ R_{S2} &= \frac{r_{d2} + R_{DD_5}}{1 + g_{m2} r_{d2} (1 + g_{m3} r_{d3})} \end{aligned} \tag{2.20}$$

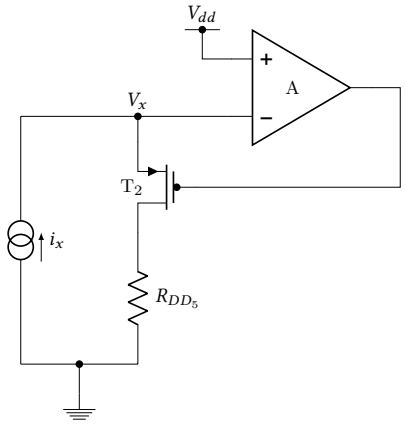


Figure 2.15: Simplified model for source resistance T_2 evaluation.

High frequency analysis The high frequency analysis is based on the evaluation of the poles of the system. At first approximation, they can be associated with the circuits nodes. The position of a pole in frequency is determined evaluating the capacitance and resistance seen in each node. In the small signal model there are two capacitances, C_L at the output node and C_p. C_L capacitance is located at a high impedance node associated with the connection between two drains, thus it corresponds to the low frequency pole. In particular, it corresponds to the dominant pole of the system, which influences the time response of the output signal when a

charge is injected into the circuit. The first pole is given by the following expression:

$$f_{p1} = \frac{1}{2\pi C_L R_{DD_{out}}} \tag{2.21}$$

where C_L capacitance is the sum of the output capacitance C_{out} and drain capacitance of transistors T_5 and T_2:

$$C_L = C_{out} + C_{GD2} + C_{GD2,ov} + C_{GD5} + C_{GD5,ov} + C_{DB2} + C_{DB2,ov} + C_{DB5} + C_{DB5,ov} \tag{2.22}$$

On the other hand, the second pole is dominated by C_p capacitance, which in part results from the Miller effect associated with the gate-drain capacitance of the local feedback transistor T_3, i.e. the fact that the value of a capacitance, connected between the input and output of an amplifier circuit, is seen from the input multiplied by a factor $(1 - A_g)$, where A_g is the voltage gain of the amplifier circuit and the capacitance is connected in parallel to the input itself. Differently, looking at the output of the amplifier, the capacitance value is multiplied by a factor around one and connected in parallel to the output itself. The impedance seen from this capacitance generates the second time constant; this impedance is the parallel between the resistance seen from the T_0 and T_1 drain and the R_{s_2} source resistance:

$$f_{p2} = \frac{1}{2\pi r_p C_p} \tag{2.23}$$

where:

$$\begin{aligned} r_p &= r_{d0} // R_{s_2} \\ C_p &= C_{GD0} + C_{GD0,ov} + C_{DB0} + C_{DD0} + C_{GD1} + \\ &\quad + C_{GD1,ov} + C_{DB1} + C_{GS2} + C_{GS3} + C_{GD3}\frac{g_{m_3}}{g_{ds_3}} \end{aligned} \tag{2.24}$$

Figure 2.16 reports the gain and phase of the forward gain stage of the Charge Sensitive Preamplifier. Values from simulations are consistent with those evaluated, with the exception of the frequency of the second pole. This discrepancy can be ascribed to the use Miller approximation at high frequency. Table 2.3 reports a comparison between evaluated and simulated values of gain and frequency parameters of the forward stage of the CSA.

Figures 2.17 and 2.18 show the obtained CSA overall schematic and DC operating point respectively.

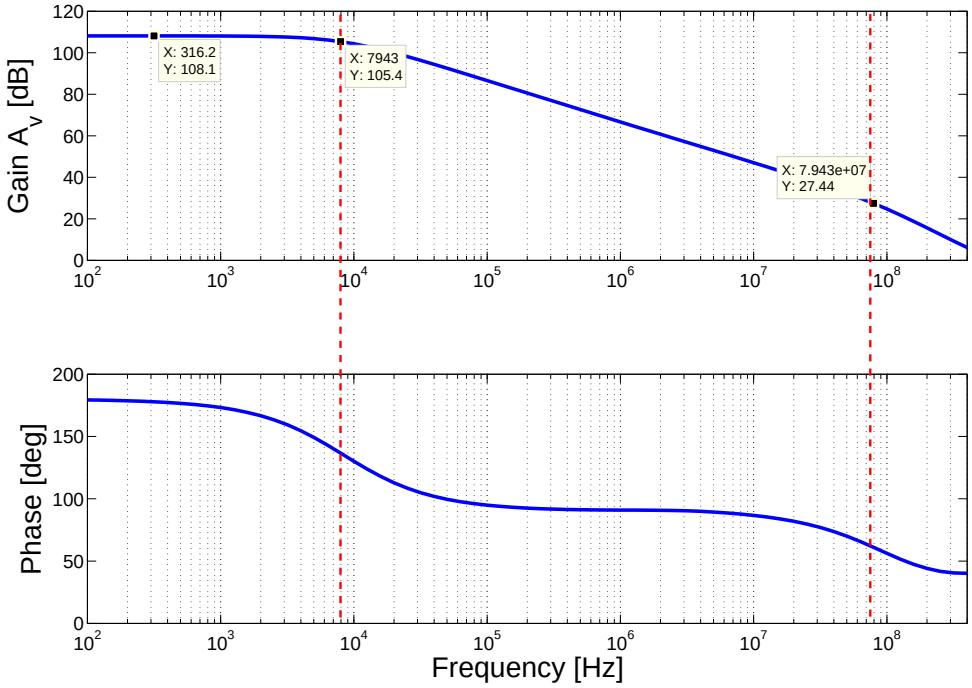


Figure 2.16: Charge Sensitive preAmplifier: overall frequency responce.

	Exctracted	**Simulated**
$A_v = g_{m0}R_{DD_{out}}$	116 dB	108 dB
f_{p1}	10.9 kHz	8 kHz
C_L	520 fF	670 fF
f_{p2}	20 MHz	79 MHz
C_p	9.5 pF	68 pF

Table 2.3: Comparison between evaluated and simulated values of the forward stage of the CSA.

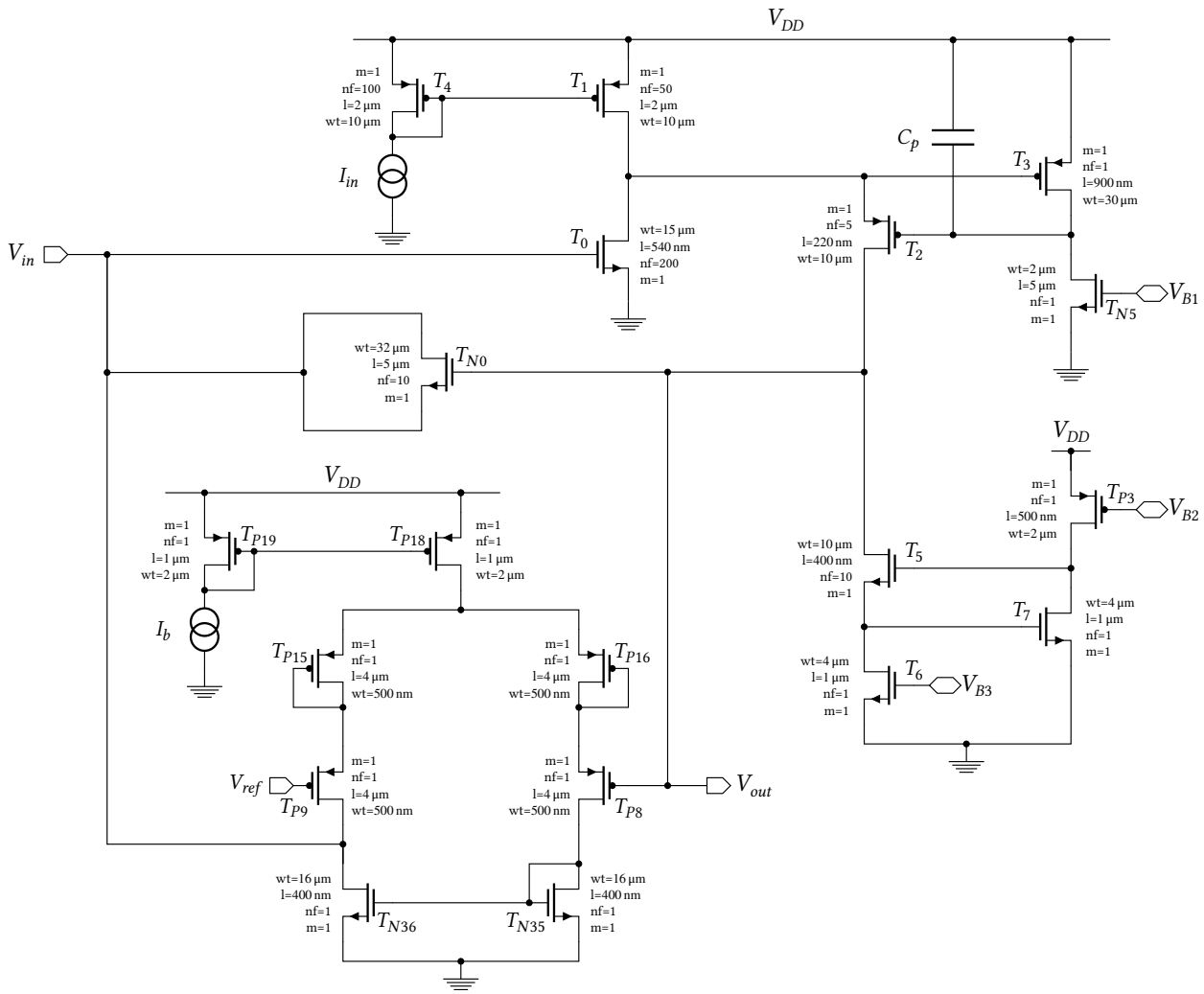


Figure 2.17: Charge Sensitive preAmplifier: overall schematic.

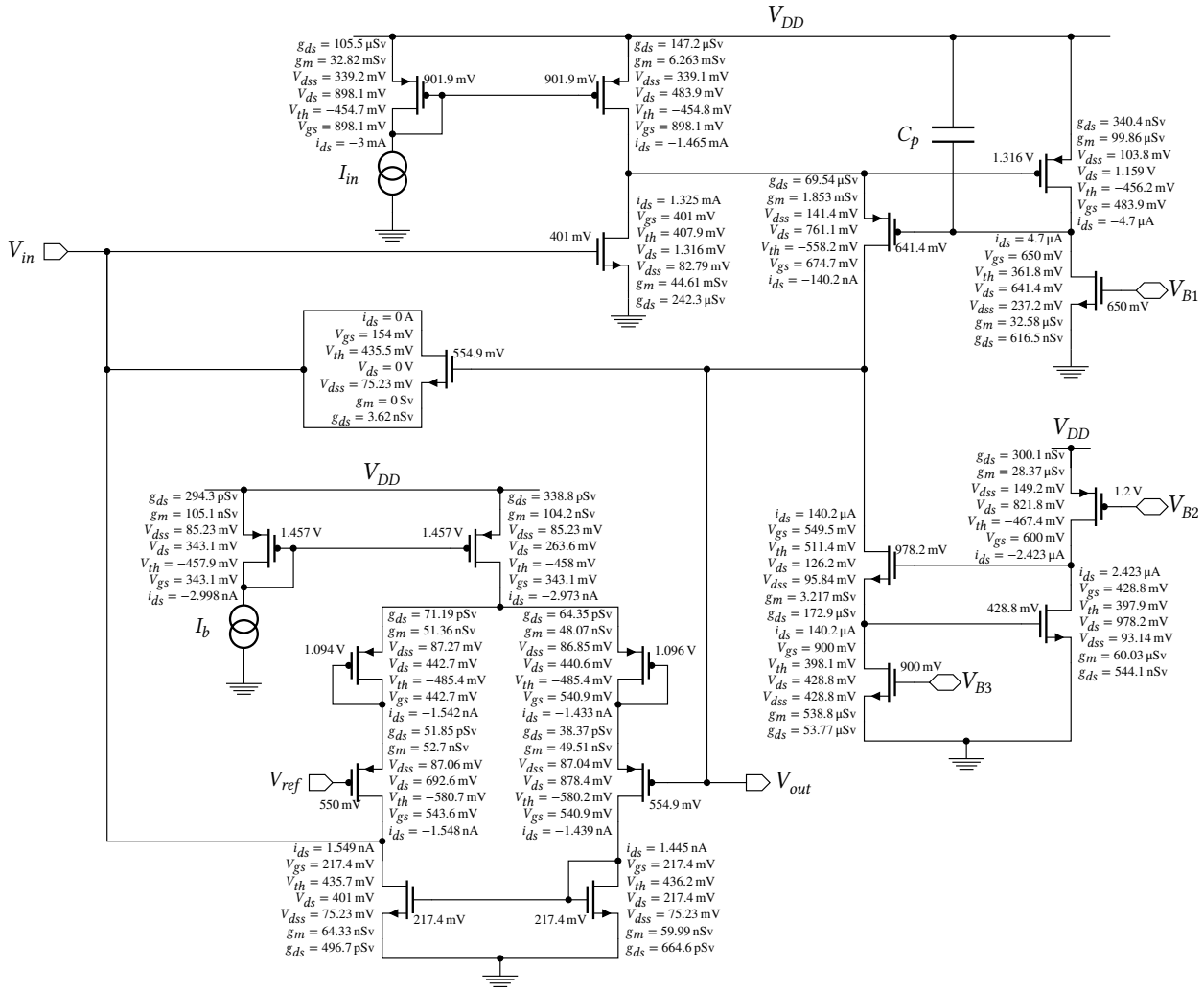


Figure 2.18: Charge Sensitive preAmplifier: DC operating point.

2.2.2 CSA Transfer Function

In this section the optimization of the CSA transfer function will be discussed. As stated in Section 2.2, a dynamic compression of the signal is mandatory to comply with the wide range of the incoming charge. The dynamic signal compression technique is characterized for having an higher gain in low energy range and a low gain in higher energy range. Figure 2.19 shows a simplified schematic of the overall charge sensitive amplifier, where G_f and V_{ref} are the current gain and the voltage reference of the transconductance stage respectively. The dimensions of the MOS

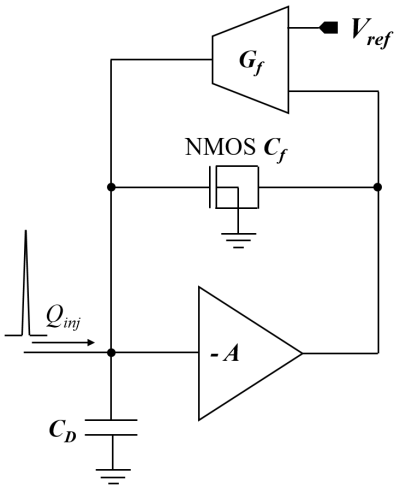


Figure 2.19: Simplified schematic of the Charge Sensitive Amplifier.

feedback device determines the slope in low and high energy. The point of the characteristic where the slope starts to change is called *kink* and it is mainly related with the device threshold voltage. Moreover, the position of the kink can also be changed by acting on the Vref voltage. An increase of the V_{ref} means a decrease of the energy of the *kink*, infact if V_{ref} is higher, the resulting V_{GS} would be closer to threshold voltage V_{Th}, see e.g. in Figure 2.20. Once the dimensions of the feedback MOS capacitance is optimized, it is possible to adjust the dynamic output voltage swing by setting V_{ref}. To optimize the amplifier transfer function, the MOS dimensions, the V_{ref} voltage and the transcondutor current gain G_f must be properly chosen.

An additional criteria is represented by the maximum output range. In the envisioned readout channel the CSA is followed by an integrator compsed by a differential pair of PMOS followed by a shaper stage. The correct operation of the integrator is guaranteed by an input dynamic range of at most 500 mV, otherwise with a higher input voltage the PMOS of the differential pair would not be in a saturation condition. This implies an output dynamic range of the CSA that has to be lower than

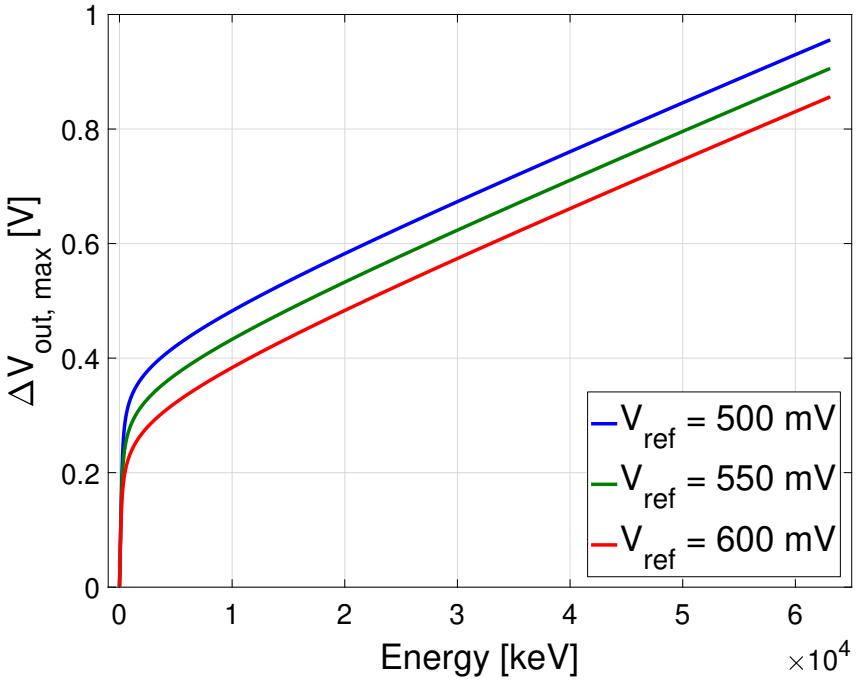


Figure 2.20: Simulation of V_{out} as a function of energy in the range from 1 keV to $\sim$ 60 MeV, for different values of voltage reference V_{ref}. The lower values of the *kinks* are a consequence of the increase of V_{ref}.

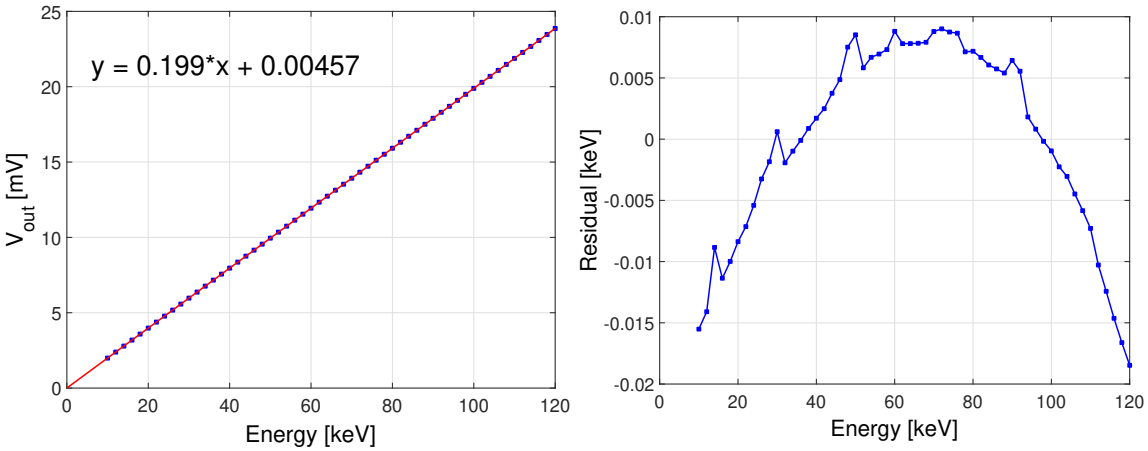
500 mV. For this reason, the gain values in low and high energy range have to be properly chosen. Using equations 2.7 and 2.8, it is possible to optimize the channel width W and length L. In the low energy range the gain is dominated by the channel width. The crucial parameters are extracted from the technology handbook. In particular, oxide capacitance per unit area $C_{ox} = 7.75\,{}^{\mathrm{fF}}/_{\mu\mathrm{m}^2}$ and effective length $L_{eff} = 130$ nm that implies an overlap of the dielectric gate with the source diffusion $\Delta L = (L_{min} - L_{eff})/2 = 25$ nm. A channel width $W = 320\,\mu$m should provide a feedback capacitance $C_f \approx 250$ fF and, consequently, a gain of $200\,{}^{\mu\mathrm{V}}/_{\mathrm{keV}}$. Once set the channel width value, only the channel length L determines the slope in the high energy range. In order to satisfy the request of an output dynamic range lower than 500 mV, the gain in high energy range was fixed to $4.5\,{}^{\mu\mathrm{V}}/_{\mathrm{keV}}$. Such value can be obtained for a channel length $L = 5\,\mu$m.

Once the dimensions of the NMOS feedback capacitance are chosen, a study of the output linearity in low range is needed. Output voltage values obtained in a simulation for detected particle energy in the range from 10 keV to 120 keV have been fitted using linear regression method with MATLAB software. Figure 2.21a shows the obtained fit curve. As already expected, the slope of the curve is $0.199\,{}^{\mathrm{mV}}/_{\mathrm{keV}}$ that is very consistent with the calculated one of $200\,{}^{\mu\mathrm{V}}/_{\mathrm{keV}}$. The offset is negligible, in fact it is around 5 µV: it has to be considered that in this energy range an

increase of 5 µV is due to a detected energy of 25 eV. The curve fit in figure 2.21a has a coefficient of determination $R^2 = 0.999$, thus the output voltage in low energy range shows a very good linearity. Figure 2.21b reports the residual values obtained subtracting to the simulated data, values espected from the curve fit and multiplying the results by the gain:

$$Res = (V_{out,sim} - V_{out,eval}) \times G \tag{2.25}$$

where $G = 0.199\,^{\mathrm{mV}}/_{\mathrm{keV}}$. The highest deviation from the ideality is lower than 20 eV: the limit of the resolution of the overall sistem is set to 4 keV and the higher residual found in low energy range is only the 0.5% of such limit. It is possible to conclude that dynamic signal compression non-linearity will not degradate the final resolution.



(a) Values from simulation (blue dots) and curve fit (red curve).

(b) Residual between ideal curve fit and actual values from simulations.

Figure 2.21: Evaluation of the linearity of the output voltage V_{out} as a function of detected particle energy E, in the range from 10 keV to 120 keV.

Figure 2.22 shows the final Transfer Function of the CSA with feedback NMOS capacitance properly dimensioned.

Figure 2.23 shows the simulated output voltage V_{out} as a function of time for different detected energies. In order to simplify such study, a constant resistance R was used as feedback resistance. For a detected energy greater than the one when the *kink* occurs, a non-exponential discharge curve is observed. The non-linearity of the feedback capacitance causes a drop down in the discharge curve. Such behavior could be misclassified by the following stages as a hole-detection event: thus, the non-exponential discharge has to be taken into account in the design of the rest of the chain, in order to properly identify actual particle detection events.

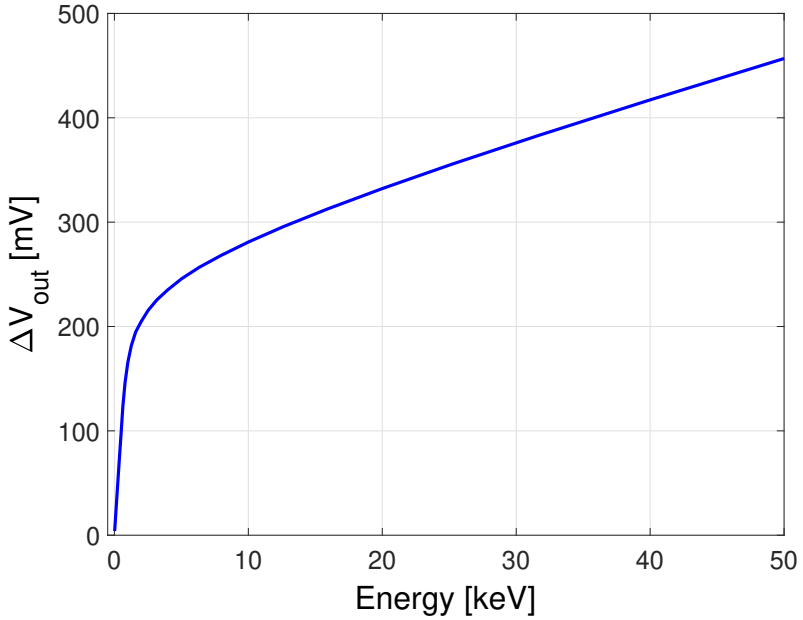


Figure 2.22: CSA final Transfer Function.

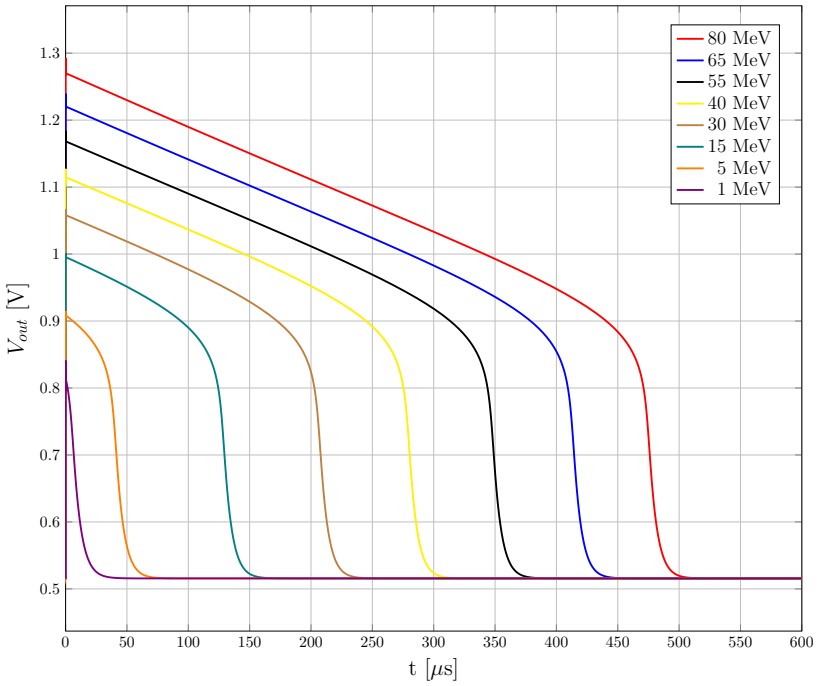


Figure 2.23: CSA output for different detected energies: since the feedback capacitance is not linear its discharge curve is not exponential.

2.2.3 CSA transconductance feedback stage

The feedback network is composed by a transconductance stage in parallel to the CMOS capacitance. The Operational Transconductance Amplifier (OTA) has the

tasks of providing a discharge path for the charge accumulated in the CMOS capacitance and, regarding the DC operating point, of fixing the otuput DC voltage. The output node without the transconductance is connected to two drains, thus it would be instable. OTA's transconductance G_f value is related to the peaking time of the stage after the CSA, because the feedback capacitance has to be discharged in a longer time than the peaking time. Indicating with t_{fall} the discharge time, the following condition has to be satisfied: $t_{fall} \gg t_p$ in order to obtain an ideal step as input signal for the shaper. As a rule of thumb it is useful to fix the discharge time at a value at least 10–20 times greater than the peaking time:

$$\begin{aligned} t_{fall} &\approx 2.2\tau \\ t_{fall} &= 20 t_p \end{aligned} \tag{2.26}$$

where $\tau = {}^{C_f}/_{G_f}$ is the OTA's time constant. In GAPS, the expected frequency of events is quite low, $f < 1\,\text{kHz}$, so another condition on the discharge time is that it has to be lower than 1 ms in order to avoid pile-up events. Using the lower value of the feedback capacitance, i.e. 250 fF, and an hypotetical peaking time $t_p = 1\,\mu\text{s}$, τ will be:

$$\tau \approx 11 \cdot t_p = 11\,\mu\text{s} \tag{2.27}$$

that means the OTA's transconductance:

$$G_f = \frac{C_f}{\tau} \approx 25\,\frac{\text{nA}}{\text{V}} \tag{2.28}$$

A transconductance stage with a low G_f is therefore needed. Figure 2.24 shows the schematic adopted for the OTA's stage. The transconductance amplifier consists in a differential pair TP_9 and TP_8, that, in the equilibrium condition, have the same voltage on the gate, so the voltage reference V_{ref} is reported as the DC output voltage of the CSA. The active load, on the other hand, is represented by transistors TN_{36} and TN_{35}. In order to obtain a transconductance stage with a low value of G_f, a source degeneration solution using a diode connected PMOS has been implemented.

When the CSA output voltage rises, the transconductance stage is unbalanced: current I_{D_x} increases due to the increase on the TP_9 gate, and consequently the current in TP_8 has to increase, because the total current in the stage has to remain constant. It is possible to describe this concept, starting from the equations that

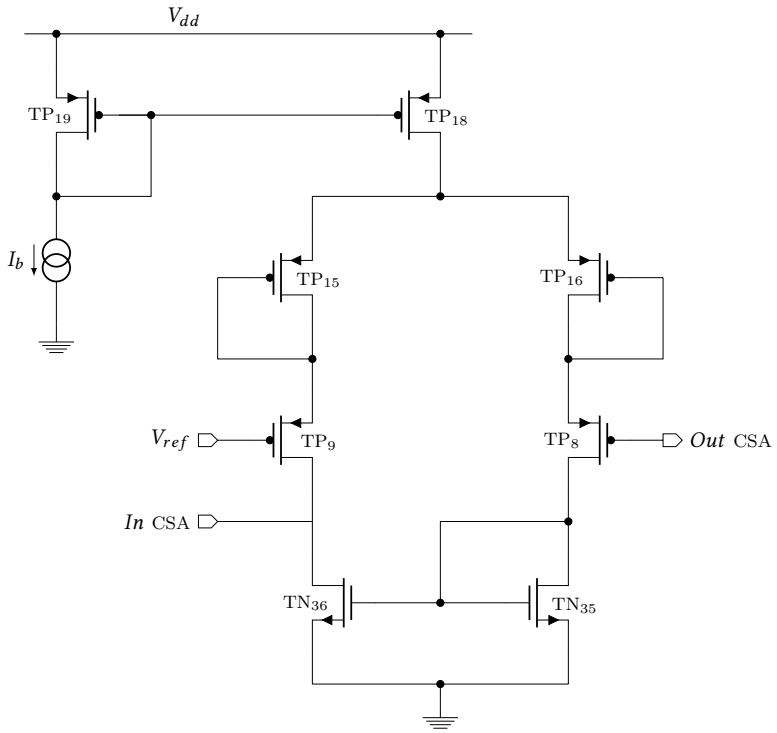


Figure 2.24: Transconductance stage schematic.

express the current in the MOSFETs:

$$I_{D_{P9}} + \Delta I_D = \beta(V_{SG} + V_{Th})^2 \tag{2.29}$$

$$I_{D_{P8}} - \Delta I_D = \beta(V_{SG} + V_{Th})^2 \tag{2.30}$$

where $\beta = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}$. The output current to the transconductor is the results of the difference of the currents between the two branches, thus:

$$\sqrt{\frac{I_{D_{P9}} + \Delta I}{\beta}} = \sqrt{\frac{I_{D_{P8}} - \Delta I}{\beta}} = V_s - V_{ref} - V_{in} + V_{Th} - (V_s - V_{ref} + V_{Th}) \tag{2.31}$$

thus:

$$\sqrt{\beta}V_{in} = \sqrt{I_{D_{P9}} - \Delta I} - \sqrt{I_{D_{P8}} - \Delta I} \tag{2.32}$$

so the output current will be:

$$I_{out} = \sqrt{\beta I_{D_{P9}}}V_{in}\sqrt{1 - \frac{\beta V_{in}^2}{4I_{D_{P9}}}} \tag{2.33}$$

and the equation expressing the gain of the transconductance will be:

$$G_f = \frac{I_{out}}{V_{in}} = \sqrt{\beta I_{D_{P9}}}\sqrt{1 - \frac{\beta V_{in}^2}{4 I_{D_{P9}}}} \tag{2.34}$$

As shown in equation 2.34 OTA's gain has non-linear behavior. Such effect can be limited using transistors with long channel and high bias current. However in this case a trade-off between linearity and correct g_m value to properly discharge the capacity has to be determined: in fact, increasing the bias current I_b, the equivalent g_m of the transconductor tends to decrease, reducing excessively the discharge time.

However, a non-linear feedback capacitance and the very large energy range makes the sizing of the transconductance stage more difficult. Figure 2.25 shows the transconductance output current I_{out} function of output voltage ΔV_{out}: the linearity of the curve is respected till an output voltage of $\approx 200\,\text{mV}$ is reached, that corresponds to a detected energy of $\approx 1\,\text{MeV}$. Such behaviour of the trasnconduc-

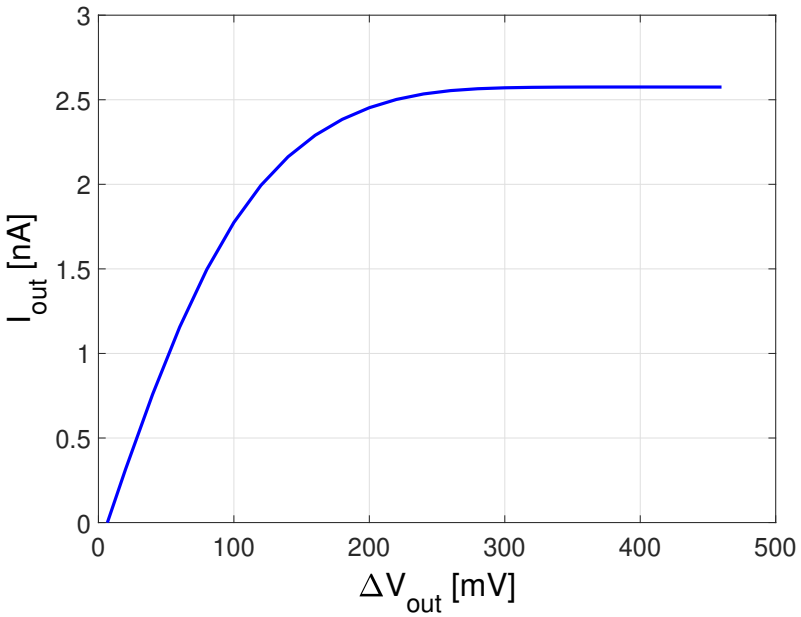
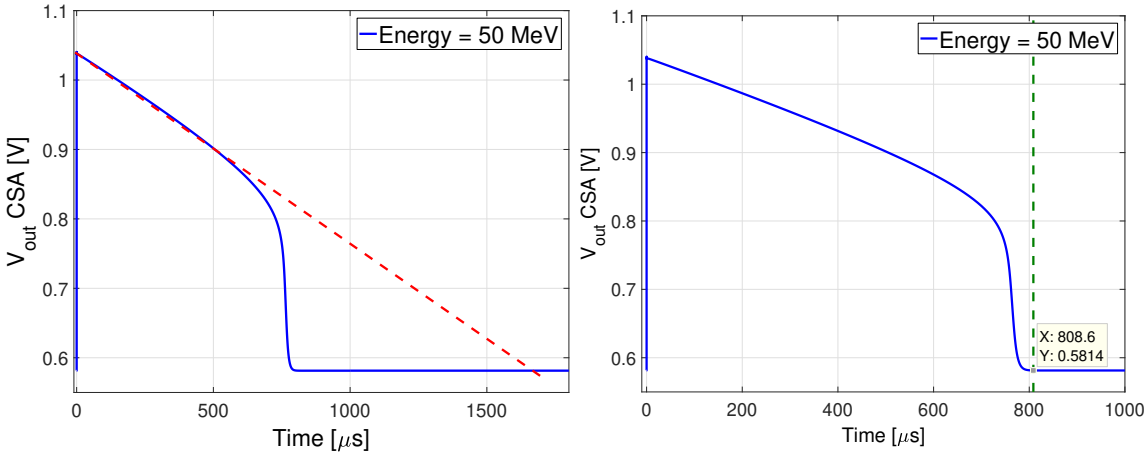


Figure 2.25: Transconductance stage output current function of output voltage ΔV_{out}.

tance stage, consistently with what observed in section 2.2.2 figure 2.23, implies that for energy greater than 1 MeV, the first part of the discharged curve is linear and not exponential. Figure 2.26a shows that for the highest expected energy and for a completely linear discharge curve, the recovery time would be greater than 1 ms, in fact it would be $\approx 1.75\,\text{ms}$(dashed red line). The solid blue line, on the contrary, represents data from simulation. It is possible to observed that when the discharged curve reaches a $\Delta V_{out} \leq 200\,\text{mV}$, the curve drops exponetially. This behavior can

be ascribed to the fact that, at some point, the transconductance stage starts to act as a constant resistor and the feedback capacitance changes to its lower constant value. Such properties lower the recovery time under 1 ms, infact, as shown in figure 2.26b, $t_{recovery} \approx 800\,\mu s$ in worst case condition, i.e. maximum expected energy $E = 50\,\text{MeV}$.



(a) Output Voltage as a function of time: solid line represents data from simulation, whereas dashed line represents a completely linear discharging curve.

(b) Output Voltage function of time: recovery time $t_p \approx 800\,\mu s$.

Figure 2.26: Transient Output Voltage analysis in the worst case condition, i.e. the highest expected energy $E = 50\,\text{MeV}$.

As previously mentioned, the drop in the discharged curve can be misinterpreted from the shaper filter. A simulation in the worst case condition, i.e. $E = 50\,\text{MeV}$, with and ideal $RC - CR^2$ shaper after CSA was performed.

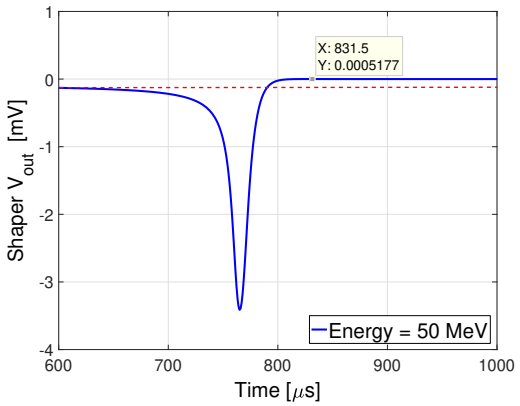


Figure 2.27: Misinterpreted elaborated signal, due to the drop in the CSA discharge curve: the overshoot is quite negligible: $\Delta V_{overshoot} \leq 520\,\text{nV}$.

Figure 2.27 shows the shaper output voltage data of such simulation that corre-

sponds to the drop in the discharged CSA output voltage curve. As expected, the shaper sees the drop as a negative step, but the overshoot connected to the filtering of this misinterpreted signal is quite negligible, in fact: $\Delta V_{overshoot} \leq 520\,\text{nV}$.

2.2.4 Open loop transfer function and closed loop gain

In this section the stability of the circuit will be analyzed by considering the open loop transfer function and closed loop gain.

In particular the effect of the capacitance C_p added in the local feedback will be discussed, as shown in figure 2.28. Such capacitance should move:

- the second pole to lower frequency;
- the right half plane zero to higher frequency.

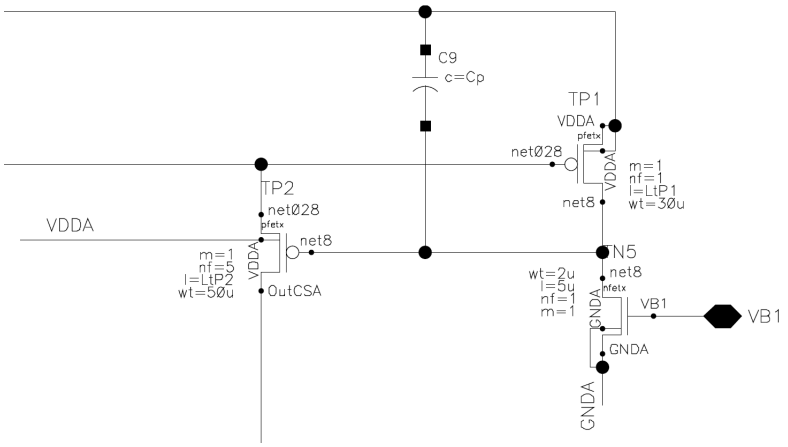


Figure 2.28: Local feedback with C_p capacitance.

As a result the phase margin in the open loop configuration increases. Figure 2.29 shows the effect of such capacitance: solid lines represents Open Loop configuration phase margin and gain curves without the use of C_p, whereas dashed lines represents Open Loop configuration phase margin and gain curves using $C_p = 2\,\text{pF}$. With capacitance $C_p = 2\,\text{pF}$, the phase margin improves with respect to $C_p = 0\,\text{pF}$. Closed loop gain has been simulated with `iprobe` tool in the configuration reported in figure 2.30. By varying the voltage reference V_{ref} (from $\approx 0.5\,\text{V}$ to $1.0\,\text{V}$) it is possible to simulate closed loop gain for different values of the incoming signal. Figures 2.31a, 2.32a and 2.33a show close loop gain and phase for detector capacitance $C_d = 0\,\text{pF}$, $40\,\text{pF}$ and $80\,\text{pF}$ respectively without compensation capacitance C_p. As expected, close loop gain functions present phase margin far better than open loop phase margin. On the other hand, figures 2.31b, 2.32b and 2.33b show close loop gain and

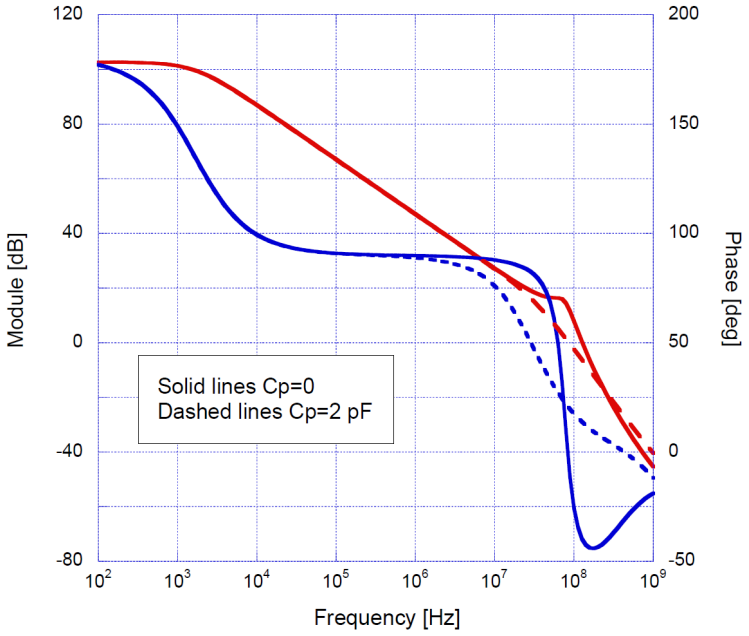


Figure 2.29: Open Loop configuration phase and gain: solid lines for $C_p = 0\,\mathrm{pF}$, whereas dashed lines are for $C_p = 2\,\mathrm{pF}$.

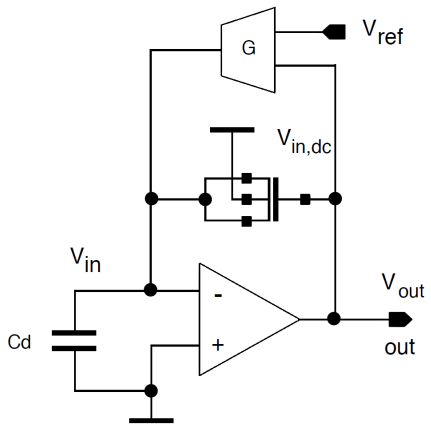
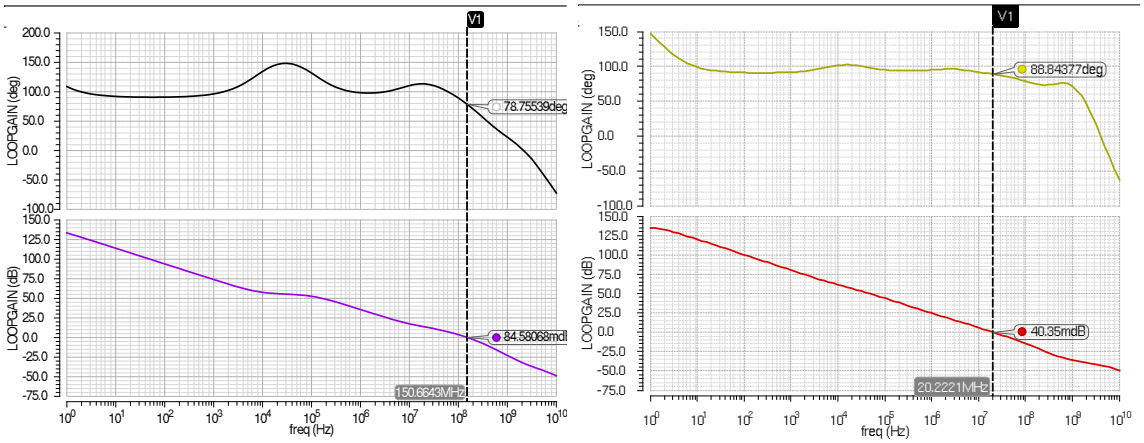


Figure 2.30: Configuration for close loop gain simulation with `iprobe` tool.

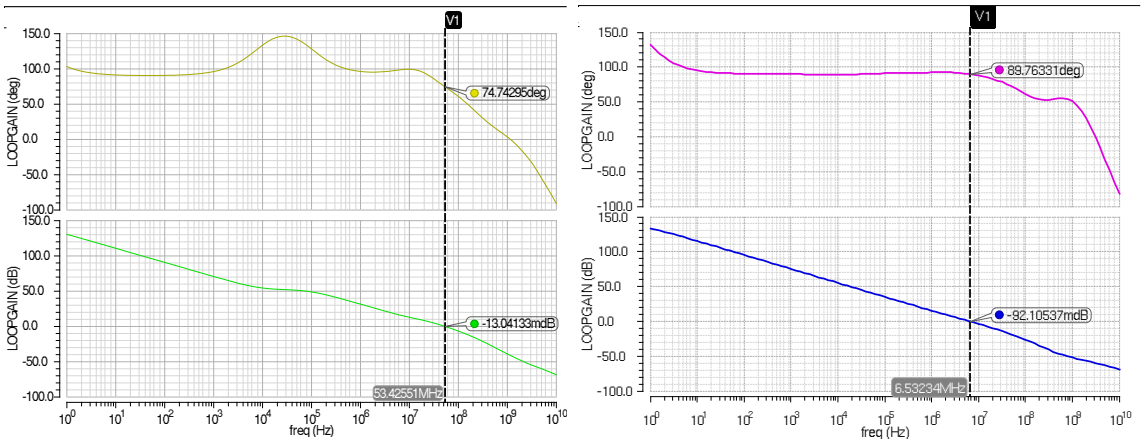
phase for detector capacitance $C_d = 0\,\mathrm{pF}$, $40\,\mathrm{pF}$ and $80\,\mathrm{pF}$ respectively with the compensation capacitance C_p. The latter graphics show a slight improvement of the already acceptable obtained phase margin.



(a) Simulation without compensation capacitance C_p.

(b) Simulation with compensation capacitance $C_p = 4\,\mathrm{pF}$.

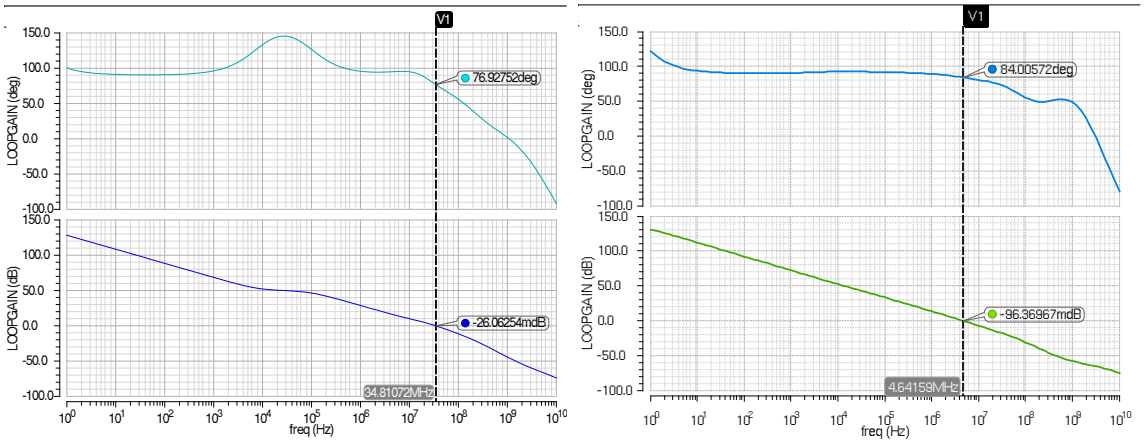
Figure 2.31: Closed loop gain simulations with `iprobe` tool with a detector capacitance $C_d = 0\,\mathrm{pF}$.



(a) Simulation without compensation capacitance C_p.

(b) Simulation with compensation capacitance $C_p = 4\,\mathrm{pF}$.

Figure 2.32: Closed loop gain simulations with `iprobe` tool with a detector capacitance $C_d = 40\,\mathrm{pF}$.



(a) Simulation without compensation capacitance C_p.

(b) Simulation with compensation capacitance $C_p = 1\,\text{pF}$.

Figure 2.33: Closed loop gain simulations with `iprobe` tool with a detector capacitance $C_d = 80\,\text{pF}$.

2.2.5 CSA Equivalent input noise and noise performance

The design of the CSA has to satisfy fundamental requirements: the equivalent input noise must be minimized and the input transistor must be the one that contributes at least 50% to the overall noise level of the circuit. These two constraints can be translated into sizing criteria, such as geometry and bias current, for the input device (T_0 in figure 2.12).

In order to properly choose the input device geometry, different criteria for channel length and channel width must be followed.

First of all, length L must be minimized in order to lower white noise. White noise can be modeled by means of the following equation:

$$S_W(f) = 4KT\frac{\Gamma}{g_m} \tag{2.35}$$

In strong inversion, g_m is proportional to $\sqrt{W/L}$. Such behavior is the reason why, normally, the input device channel length is given by the minimum dimension allowed by the technology, in this case 180 nm. Flicker noise presents the opposite behavior. As reported in equation 1.19, flicker noise is inversely proportional both to channel width W and channel length L. The chosen 180 nm technology shows higher flicker noise values with respect to the discrete version of the preamplifier with a JFET at the input as shown in figure 2.34. For this reason a higher values of L has been chosen. Previous studies [27] show that the value of the flicker noise

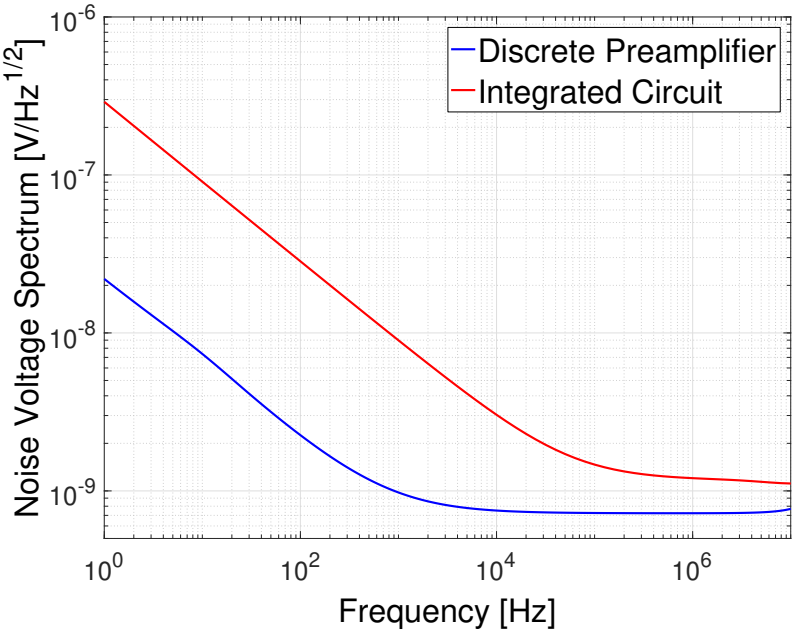


Figure 2.34: Comparison of the Equivalent Input Noise betweeen the integrated charge sensitive preamplifier and the discrete preamplifier with a NJFET at the input.

coefficient, K_f, is asymptotic at a minimum value for channel length $L \geq 3L_{min}$, so the input device channel length was fixed at $3 \times L_{min} = 540\,\text{nm}$.

However, it has to be taken into account that the channel width and lenght also determine the value of the input capacitance of the MOS:

$$C_{GS} = \frac{2}{3} C_{OX} W L \tag{2.36}$$

The value of this capacitance must be chosen in order to obtain the best coupling, in terms of contribution of noise, betweeen the input and the detector capacitance. Channel width was fixed at $W = 3\,\text{mm}$ which corresponds to in input capacitance of 2.57 pF.

Moreover, the drain current of the input device sets the value of the transconductance and consequently of the white noise. Thus it is advisable to fix a relatively high current in the input device, e.g. $I_D = 1.5\,\text{mA}$. Table 2.4 reports the top 5 noise sources of the CSA. As expected, the input device contributes for the 40 %. Another great contribution to the equivalent input noise comes from the two NMOS of the transconductance, i.e. $T_{N36} = 16\,\%$ and $T_{N35}13\,\%$.

Once the equivalent input noise has been optimized, it is possible to obtain an extimation of the expected energy resolution. In particular, white and flicker noise

Device	Parameter	Noise Contribution	% Of Total
T_0	thermal	$2.75 \cdot 10^{-5}$	19
T_0	flicker	$2.75 \cdot 10^{-5}$	19
T_{N36}	thermal	$2.52 \cdot 10^{-5}$	16
T_{N35}	thermal	$2.27 \cdot 10^{-5}$	13
T_1	thermal	$1.43 \cdot 10^{-5}$	5

Table 2.4: Noise contribution of the CSA.

parameters are used to evaluate the Equivalent Noise Charge:

$$ENC^2 = C_D^* \left(A_1 \frac{S_W}{\tau} + A_2 2\pi A_f \right) + \left(2qI_D + \frac{4kT}{R_f} \right) A_3 \tau \tag{2.37}$$

where ${C_D^*}^2$ is the detector capacitace, S_W the white noise, A_f the voltage noise spectrum at 1 Hz, I_D the detector leakage current and R_f the equivalent feedback resistance. A_1, A_2 and A_3 are three coefficients that depend on the signal shaping [12]. Implementing an RC^2-CR semigaussian shaping stage following the CSA, the three coefficient assumes the following values: $A_1 = 0.85$, $A_2 = 0.54$ and $A_3 = 0.61$. The resolution of the detector is represented by the **Full Width at Half Maximum FWHM** that is the width of a spectrum curve measured between those points on the y-axis which are half the maximum amplitude, see figure 2.35. Energy spectrum is expected to show a gaussian distribution, so to equivalent noise charge can be related to the FWHM by the following relation:

$$FWHM = F\varepsilon \frac{ENC}{q} \tag{2.38}$$

where F is the Fano factor equal to $F = 2\sqrt{ln2} \approx 2.355$ and $\varepsilon = 3.6\,\text{eV}$ is the energy required for the production of an electron-hole pair in the Silicon. The final

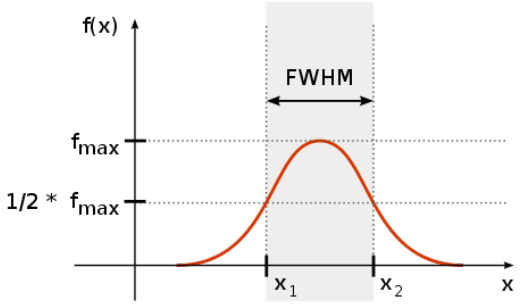


Figure 2.35: Rapresentation of the Full Width at Half Maximum in a gaussian distribution.

resolution strongly depends on the detector capacitance and the leakage current, as

shown in equation 2.37. Thus, the charge sensitive preamplifier has been studied/optimized for detector capacitance values from 38 pF to 85 pF and leakage current from 1 nA to 10 nA that are, respectively, the best and the worst case expected. The detector capacitance values can be evaluated considering the detector as a capacitor constructed of two parallel plates, thus:

$$C_{Si} = 1.05\frac{A}{t} \tag{2.39}$$

where A is the detector area expressed in cm^2 and t is the detector thickness expressed in cm. Detector thickness is 0.25 cm, whereas detector diameter is still not fixed and the values taken into account goes from 7.62 cm to 10.16 cm. The detector will be divided in slices of equal diameter, but the number of slices is not decided yet. Table 2.5 reports a comparison between the evaluated values of FWHM for integrated CSA (using equations 2.37 and 2.38) and discrete preamplifier within the condition obtained in the first pGAPS launch. Such values are quite promising because in spite of the fact that the integrated CSA shows a higher flicker noise than discrete components, the overall FWHM is comparable with results obtained with the discrete preamplifier. The reason of this behavior might be ascribed to the choice of the peaking time in the IC design, that was fixed at $t_p = 700$ ns instead $t_p = 1$ µs, that is the value used for the discrete preamplifier. Simulations show that a peaking time 0.6 µs $\leq t_p \leq 1$ µs minimize the ENC.

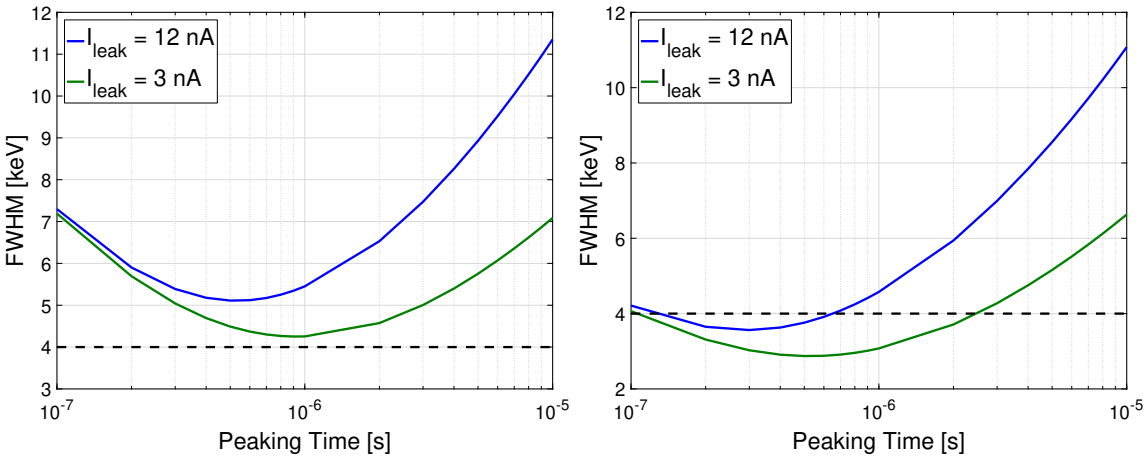
Right now the detector design group is confident that the next generation of Si-Li detector will present values of leakage current for each strip from 1 nA to 10 nA [19]. Figures 2.36a and 2.36b show the FWHM as a function of the peaking time t_p in the case of a 3 nA and 12 nA of leakage current for a detector capacitance of 80 pF and 40 pF respectively. It is possible deduce that for an 80 pF detector capacitance is no possible to reach the required specification of a $FWHM \leq 4$ keV neither for $I_{leak} = 3$ nA nor for $I_{leak} = 12$ nA. On the contrary, for a 40 pF detector capacitance it is possible reach values below 4 keV even in the worst case of leakage current. In order to satisfy the request of $FWHM \leq 4$ keV, a detector capacitance $C_D \leq 50$ pF is needed. Such results are consistent with those obtained in table 2.5.

2.3 Discussion

The first block of the analog readout channel, i.e. the Charge Sensitive preAmplifier, for a novel cosmic antideuteron detector in the GAPS project has been designed and simulated. The preamplifier is composed by three stages: forward gain stage,

Diam [in]	Strips #	I_{tot} [nA]	I_{strip} [nA]	C_d [pF]	R_s [Ω]	δE_{PA} [keV]	δE_{ASIC} [keV]
4	8	100	1.25	42	0	3.6	3.7
4	6	100	16.7	57	0	4.2	4.3
					1	3.7	4.3
					10	3.8	4.4
					20	4.0	4.6
4	4	50	12.5	85	0	4.9	5.0
					1	4.2	5.0
					10	4.5	5.3
					20	4.7	5.6
3	4	55	13.8	48	0	3.8	3.9
3	5	55	11.0	38	0	3.2	3.6

Table 2.5: Comparison between estimated FWHM for IC and discrete preamplifier (PA). The peaking time for the IC circuit is $t_p = 700\,\text{ns}$, whereas for the PA is $t_p = 1\,\mu\text{s}$.



(a) Detector capacitance $C_D = 80\,\text{pF}$. **(b)** Detector capacitance $C_D = 40\,\text{pF}$.

Figure 2.36: Evaluation of the FWHM as a function of peaking time t_p for different values of detector capacitance C_D and leakage current I_{leak} at a temperature $T = -50\,°\text{C}$.

transconductance stage and feedback MOS capacitace. Each block was studied in detail. The preamplifier presents a non-linear output typical of the dynamic signal compression technique adopted here. Such technique was implemented both to satisfy the double gain requirements set by the experiment and to cover the wide

energy range expected in an integrated circuit operating at a relatively low voltage bias (1.8 V). A gain of 200 $\mu V/keV$ in low energy range and 4.5 $\mu V/keV$ in high energy range has been obtained, which yields an otuput dynamic range lower than 500 mV. Another key characteristic of the CSA is that, assuming a detector capacitance of 40 pF, a simulated energy resolution lesser than 4 keV can be achieved: the limit of 4 keV was a strict requirement set by the experiment.

A protopyte chip will be submitted by the end of the year 2017. The final chip have to be ready and tested by the June 2019 in order to make possible the first launch by the end of year 2020.

3 DSSC Bare Module Testing Activity

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Nanotechnology is based on the ability to perform measurements and manipulate objects at a molecular scale. For example the smallest molecule is the diatomic hydrogen (H_2), with a bond length of 0.74 Å and the water molecule (H_2O) presents a bond length of 20 Å = 2 nm. The time scale of the dynamic processes in this field is of the order of femtoseconds. Investigating such small scale and fast phenomena is of utmost importance in understanding the states of matter, phenomena during molecules reaction processes and the further development of advanced materials with innovative functionalities.

X-ray Free Electron Lasers (XFEL) are bound to become the predominant tools for investigating natural phenomena taking place at nanometer scale and the complex structure of organic and inorganic materials. These facilities, capable of producing photon pulses with outstanding brightness and ultra-short duration, are a promise to revolutionize a number of research fields, e.g. structural biology, chemistry, material science and molecular physics. The class of laser known as XFEL (X-rays Free Electron Laser) is a type of free electron laser where the electron beam producing radiation has such an energy to emit radiation in the X-ray spectral zone. Since the emission frequency is proportional to the square of the energy of the electrons, the

energies needed to reach the X-ray wavelength are very high, i.e. of the order of the gigaelectronvolts.

In Free Electron Lasers (FEL) a beam of relativistic electrons, i.e. with a velocity close to the speed of light, is made to wiggle through an undulator (a periodic magnet array) producing a coherent and collimated X-ray beam as shown in Figure 3.1. Self-amplified spontaneous emission (SASE) is used to start the light ampli-

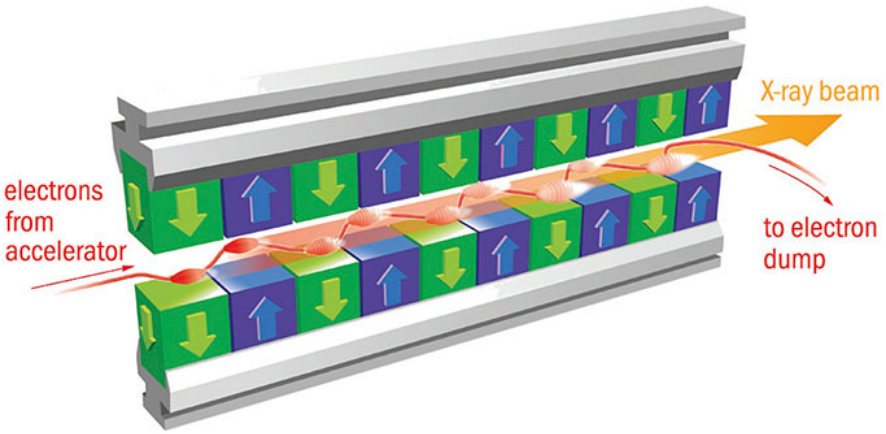


Figure 3.1: Undulator.

fication process. In the undulator, the electrons acquire an undulatory motion in the plane orthogonal to the magnetic field and emit light characteristic of the undulator strength, within a certain energy bandwidth. [30] The wavelength λ of the emitted radiation depends on the undulator geometry (the period λ_q of the wiggler), the magnetic field intensity B and the electron energy E by means of the following equation:

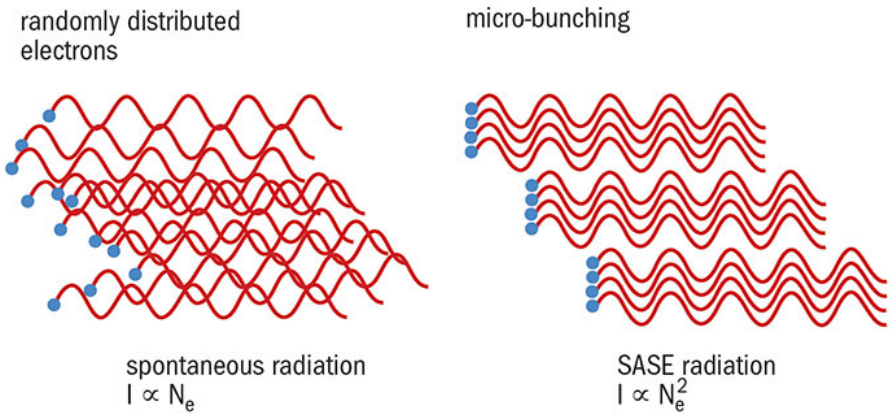
$$\lambda = \frac{\lambda_q}{2}\left(\frac{m_0 c^2}{E}\right)^2 \left(1 + K^2\right) \tag{3.1}$$

where K is the undulator paramenter:

$$K = \frac{q\lambda_q\sqrt{\langle B^2\rangle}}{2\pi m_0 c^2}. \tag{3.2}$$

As a bunch of electrons start their travel through the undulator, low intensity, incoherent (out of phase) radiation is emitted, see Figure 3.2a. The emitted photons travel slightly faster than the electrons, thus interact with the beam each undulator period. Depending on the phase to each other, electrons gain or lose energy, i.e. faster electrons catch up with slower ones [29]. Thereby the electron bunch density is periodically modulated by the radiation which is called *microbunching*. Microbunched electrons behave as a single charged particle, emitting a beam of

quasi-coherent photons, thus extremely short and intense flashes of laser-like light is obtained, see Figure 3.2b. The minimum wavelength, of the order of one Angstrom,



(a) Incoherent emission. **(b)** Quasi-coherent emission.

Figure 3.2: SASE radiation.

and the intensity of the laser beam available in FEL systems, make possible to see objects with nanometer feature size. The science base accessible at FELs is quite broad, including structural biology, chemistry and molecular science.

Experiments in such facilities involve very severe requirements on each building block of the overall system, including the readout electronics and the detector. The electronic instrumentation must be able to cope not only with an input dynamic range that can goes from 0.3 keV up to $\sim$ 10 keV and from 4000 ph to 100 000 ph, but also with the requirement of single photon resolution for small input signals. The detector must feature a small pixel pitch, of the orders of tens of a µm, and a quite large sensing area. The readout of the full detector must occur at very high speed, approaching 5 Mfps. Last but not least, both the detector and the readout electronics must be able to withstand high radiation environments, with a total ionizing dose ranging from 1 Grad up to 100 Grad. Active edge pixel sensors represent an interesting solution to minimize the dead area of the detector. The 3D approach of layering tiers of active circuitry, besides increasing the overall circuit density, reduces the overall length of the device interconnections, increases the speed and reduces the power consumption.

At the European XFEL the foreseen X-ray pulses will be generated with a repetition rate of 4.5 MHz and with a time interval of about 100 ms between two subsequent bursts, each one composed of a train of 3000 X-ray pulses with a temporal distance of 200 ns, as reported in Figure 3.3. European XFEL presents 5 different beam lines that allowing for an X-ray energy range from $1 - 10$ keV.

The DSSC collaboration is developing a detector for X-ray FEL applications able

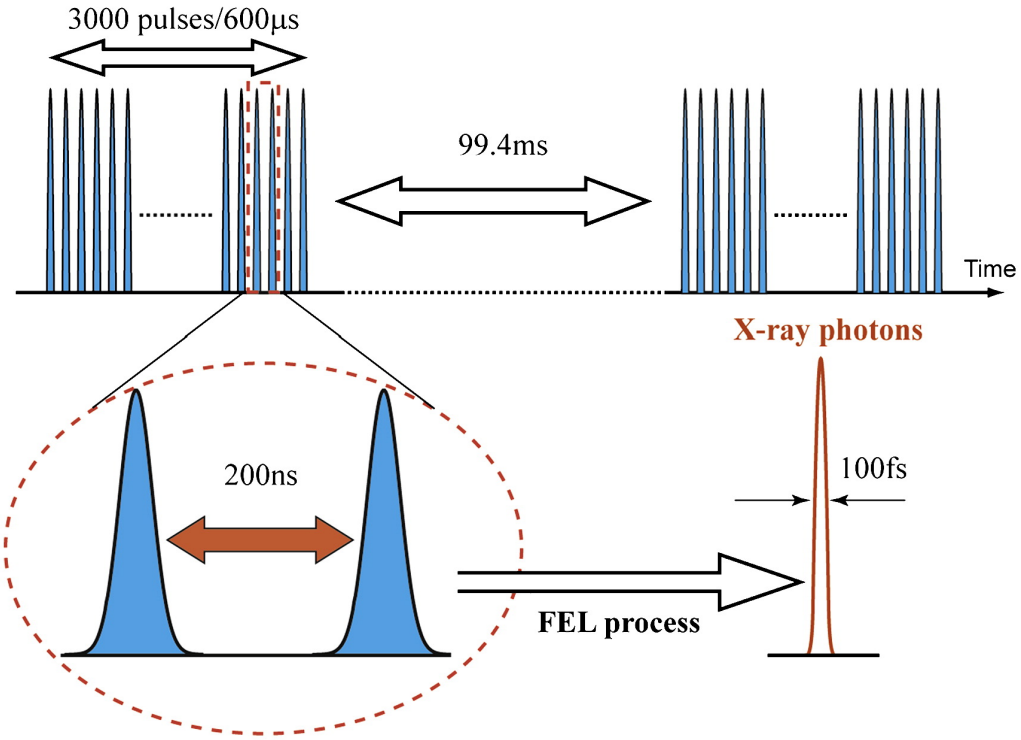


Figure 3.3: X-ray bunch structure at the European XFEL [31].

to cope with the demanding requirements set by the European XFEL [32]. The DSSC project (DEPMOS Sensor with Signal Compression) has the goal to develop a silicon detector for XFEL with $\sim 40\,000\,\mu m^2$ hexagonal pixels by means of non-linear gain DEPFET sensor for the energy range $0.5 - 6\,keV$ capable of taking up to 600 frames at 4.5 MHz. To pursue such a goal, the project is developing a system with a pixellated silicon sensor based on a new DEPFET device, connected via bump-bonding to an ASIC for the parallel readout of the full matrix. As depicted in Figure 3.4, each quadrant of the focal plane consists of 4 ladders and 8 monolithic sensors of 128×256 pixels, with an overall sensing area of $21\,cm \times 21\,cm$. Each ASIC integrates 64×64 readout channels, with an array of 2×4 ASICs bump bonded to one sensor. The final 1 Mpixel camera will be composed by $256 \times 64 \times 64$ pixels.

In the framework of the DSSC collaboration, a characterization activity has been carried out on the first protoype of the bare module, i.e. the pixel sensor matrix connected to the readout ASIC via bump bond. This chapter presents the characterization of the readout ASIC functionality and the backside current of the first bare module production (a.k.a. F1): it presents a validation activity of a prototype of the DSSC Chip, aimed to check the proper operation of the single ladders. In order to monitor the yield of various production steps of the module (wafer dicing, shipping, flip chip mounting, wire bonding), it must be guaranteed that functioning

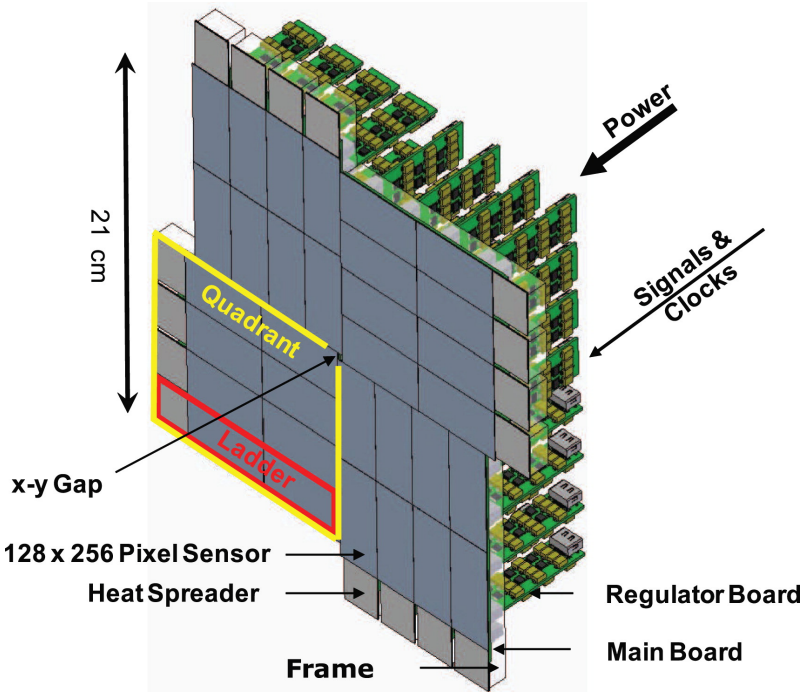


Figure 3.4: 3D view of the DSSC focal plane.

chips are used for specific assembly. After the Known Good Dies (i.e. functioning ASIC) have been identified, the flip chip and bumpbonding to the sensor has been performed by AEMTech foundry. This activity was carried out in order to verify that such operations don't damage neither the ASIC Chip nor the DSSC sensor. A second, and final, mass production, F2, is scheduled for the end of year 2017.

3.1 Overview of the DSSC project

As already mentioned, the DSSC collaboration is developing a detector for X-ray FEL applications able to deal with the requirements of the European XFEL. The main specifications of the DSSC detector are summarized in Table 3.1.

3.1.1 The DEPFET Sensor with Signal Compression

The radiation sensible element of the DSSC detector is a new type of DEPFET device, the so called DEPFET Sensor with Signal Compression (DSSC). The DEPFET device is a Field Effect Transistor (FET) with an electrode on the bottom surface acting as radiation entrance window [33]. As shown in Figure 3.5, Bulk contact is n-doped and reverse biased with respect to the p-doped source, drain and back contact. Using the correct doping concentration and bias voltage, a potential maximum

Parameters	Value
Energy Range	$1\,\text{keV} \div 10\,\text{keV}$
Number of Pixels	1024×1024
Pixel Size	$204 \times 236\,\mu\text{m}$
Input Dynamic Range	$\geq 10\,000\,\text{ph}$ for $E \geq 1\,\text{keV}$ $\geq 4000\,\text{ph}$ for $E = 0.5\,\text{keV}$
Resolution	1 ph
Frame Rate	$0.9 \div 4.5\,\text{MHz}$
Average Power Consumption	400 W in vacuum
Operating Temperature	253 K

Table 3.1: Summary of the DSSC main specifications.

below the channel of the transistor is created. Such region is called *internal gate* and collects signal electrons generated within the depleted bulk [34]. The collected charge can be read-out with one of the two following solutions:

- **Sorce Follower:** the current is imposed by means of an external current source, and the device is operated in source follower configuration.
- **Drain Read-Out:** the terminals of the device are kept to a external fixed potential and the drain current, which is proportional to the collected signal charge, is read out.

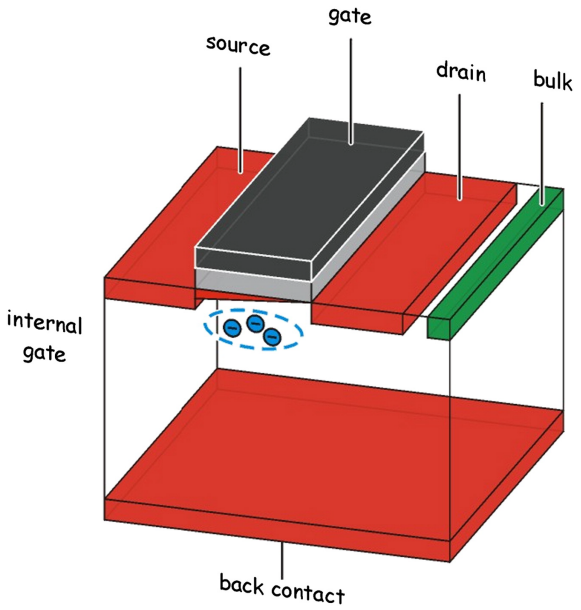


Figure 3.5: Simplified view of a DEPFET device.

The charge collected in the internal gate can be removed by applying a positive voltage pulse to the bulk contact.

In order to cover the wide input dynamic range and simultaneously the single photon detection expected at European XFEL, a non-linear response of the system front-end is needed. The DEPFET pixels provide signal compression at the sensor level. Such feature has been obtained extending the internal gate into the region below the large area source region, as reported in Figure 3.6. Adopting this solution, the small signal charges are collected below the channel and fully contribute to increasing the transistor current, whereas if the charge collected is large and consequently spilled a bit underneath the source region, the increase in the transistor current is less effective. Such beahvior results in the non-linear response of

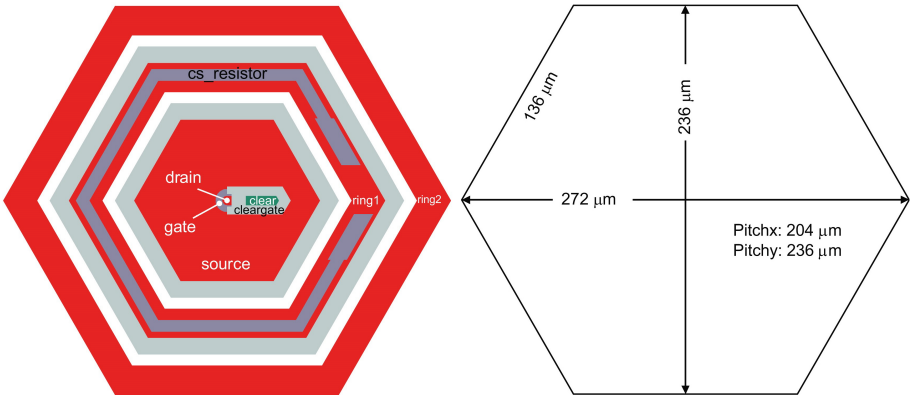


Figure 3.6: Top view of the DSSC pixel cell.

the charge-current characteristic shown in Figure 3.7. The pixel shape of a regular hexagon has been chosen in order to optimize the signal collection time. An hexagon, with a side length of 136 µm, a pitch of 204 µm along the x direction and a pitch of 136 µm along y direction, minimizes the distance from the center to the edge with respect to the more classical square shape. The device is enclosed by two drift rings that are biased in such a way that signal electrons are guided towards the centre of the pixel, providing a more homogeneous drift field.

There is also a simplified Mini-SDD array that will be used to build the first mega-pixel camera for the day-zero of the European XFEL operation, where the dynamic range compression will be not provided by the sensor itself, but by ASIC front-end, using dynamic signal compression explained in Chapetr 2.

3.1.2 The DSSC Chip

The readout ASIC for DSSC project is designed in 130 nm CMOS technology manufactured by IBM foundry. The maximum power supply voltage is 1.2 V. ASIC readout, a.k.a. DSSC Chip, is constituted by a 64×64 pixels matrix characterized

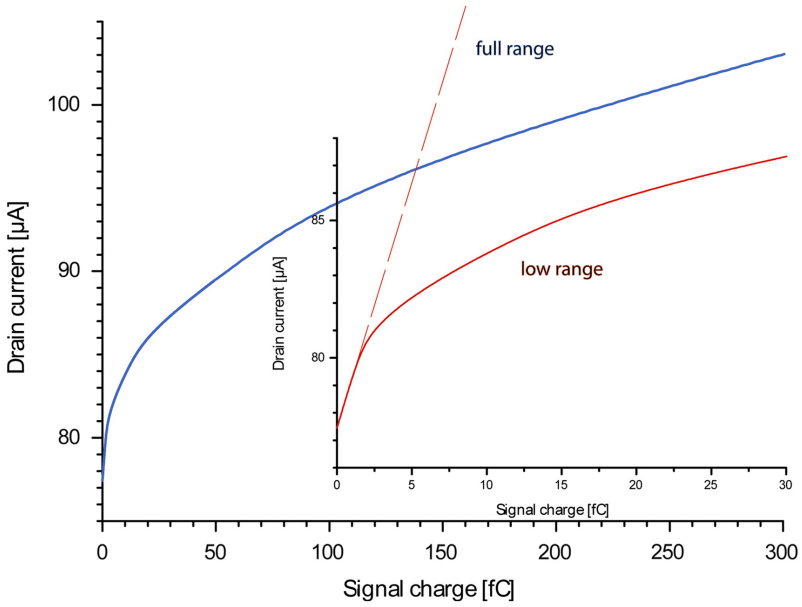
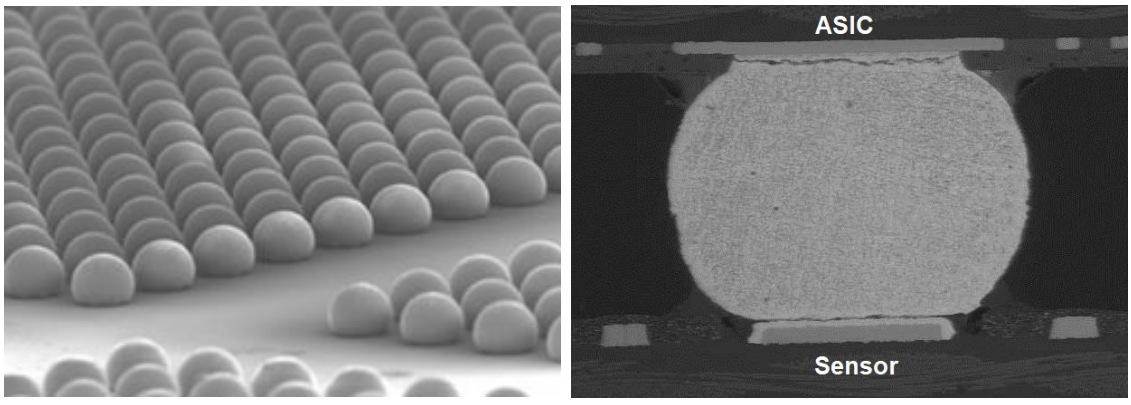


Figure 3.7: Non-linear response of the DSSC sensor.

by a low-noise readout channel. All pixels have integrated the digitization of the DSSC output current at a rate between 0.9 MHz and 4.5 MHz. Each pixel has a form factor of 204 µm × 236 µm and is directly connected to one pixel sensor with the *bump-bond* technique, i.e. small spheres of solder (with the diameter of approximately 100 µm) that guarantee mechanical and electrical connections 3.8a and 3.8b.

Figure 3.9 shows a single readout channel, composed by the following building



(a) Overall view of solder bumps on a matrix.

(b) Side view of a single bump connected to both ASIC and sensor.

Figure 3.8: Bump bonding: small solder spheres ensuring mechanical and electrical connections.

blocks:

- An input cascode stage has the task of keeping the drain of the DSSC at

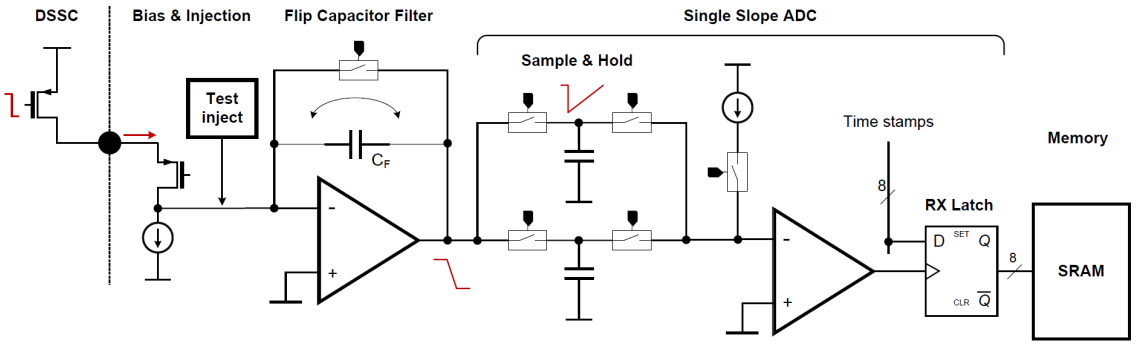


Figure 3.9: Conceptual schematic of one DEPFET Sensor with Signal Compression readout channel.

constant potential, thus enabling the drain current mode operation. The drain of the input cascode is connected to the virtual ground of the front-end filter, and is set to a potential of 950 mV.

- A pixel-level adjustable current source for the DSSC bias current cancellation [35]. This circuit is based on a 5-bit DAC (with pixel-wise settings) and an additional continuous regulation which is operated in a closed loop before the arrival of the X-ray macro bunch.

- A time variant filter, also known as the Flip Capacitor Filter (FCF), acting as gated integrator and performing correlated double sampling with a trapezoidal weighting function. In order to compensate the signal measurement for the bias current contribution, both the baseline and the signal are integrated in a single stage by flipping the feedback capacitance [36] of the amplifier. The gain of the stage can be adjusted by changing the feedback capacitance, depending on the input photon energy. The reference voltage of the FCF is 950 mV.

- An injection circuit for pixel-level calibration of the readout channel and for functional test purposes (*Bergamo injection circuit* [37] [38]). The circuit is based on an 8-bit binary weighted current steering DAC topology, and integrates a coarse current DAC for the emulation of the bias current from the DSSC.

- A pair of Sample-and-Hold (S&H) capacitors for an interleaved readout operation.

- An 8-bit Wilkinson type (single slope) ADC [39], based on a ramp current,

started with a precise strobe, which charges the S&H capacitors and latches 8 gray coded differentially distributed time stamps once the threshold voltage is reached. A fast 800 MHz external clock is used to toggle the counter on both edges, resulting in a time resolution of 625 ps. The ramp current is pixel-level adjustable for a fine tuning of the gain of the readout channel. Moreover, a programmable time delay on the ramp signal makes possible to individually adjust the ADC offset with a granularity equal to $^1/_{10}$ of the bin size. An additional bit can be used with operation at frequencies lower than 4.5 MHz. The ADC covers an input voltage ranging from 0.2 V to 1 V, respectively for high and low signals at the input of the front-end.

- A SRAM to store 640 words of 9 bits during the X-ray pulse train period. The size of the memory makes possible to store all the events occurring in a 600 µs bunch train period with a 0.9 MHz burst mode operation. At higher frequencies, further events can be stored thanks to a vetoing mechanism which discriminates whether a successfull hit has occured or not.

- Additional auxiliary blocks, like static control registers, a large switchable decoupling capacitor, monitoring lines and a debug readout circuit.

DSSC Chip has a global digital control block able to manage the operation of the ASIC. It contains the Master Finite State Machine (FSM), Sequencer, SRAM Controller, Sequencer Controller and a JTAG interface for slow control. JTAG (Joint Test Action Group) is a consortium of 200 integrated circuit manufacturers and print circuits with the purpose of defining a standard protocol for functional testing of such devices. Each module has its own configuration register. The pixel control registers are accessed throughout JTAG.

3.2 Bare Module test bench

A series of tests was performed principally on two different type of devices:

- MiniSDD 64 × 64 modules: provided in a Gel-Pak container, Figure 3.10;

- Large sensor: and 128 × 64 and 128 × 256 PXD8 sensors, provided in a storage container Figures 3.11a and 3.11b.

The tests on the bare modules include the validation of each ASIC, with standard measurements on the single microelectronic building block, and the measurement of the I/V characteristic of the sensor. ASIC's tests are divided in 5 different type, more in details:

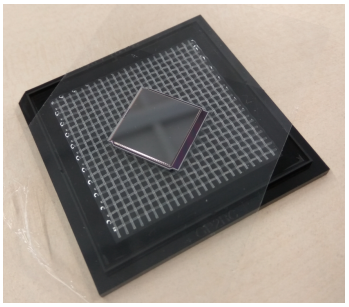
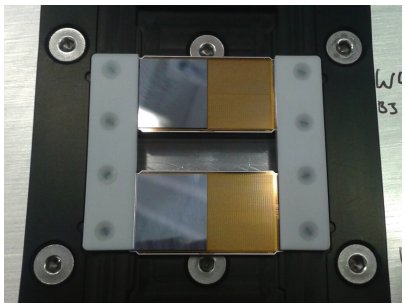
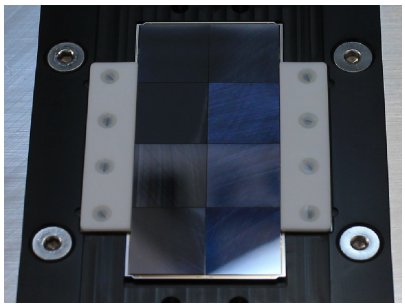


Figure 3.10: MiniSDD 64 × 64 in the Gel-Pak container.



(a) 128 × 64 pixels.



(b) 128 × 256 pixels.

Figure 3.11: PXD8 sensors in the storage container.

- digital;
- power consumption;
- perifery;
- Analog to Digital Converter;
- Front-End.

The tests setup includes a 150 mm probe station (EPS150FA provided by Semiprobe), a 3 Megapixel digital videocamera and a vibration isolation table.

Figure 3.12 shows how the ASICs are arranged in one bare module. Each ASIC has 80 wire bonding pads, with an area of 130 × 256 μm^2 each and a pitch of 150 µm. The bare module is hosted in a storage container (Figure 3.13a) which is vacuum clamped to the chuck of the probe station. Each ASIC of the bare module is clamped with a holder mechanism, as depicted in Figure 3.13b.

The pads on the ASIC are contacted according to the diagrams of Figure 3.14a and Figure 3.14b, with 80 tungsten-rhenium probe tips descending for about 3.65 mm from the probe card (PC). The contact with each ASIC is achieved by finely shifting the chuck, along the x and y axes.

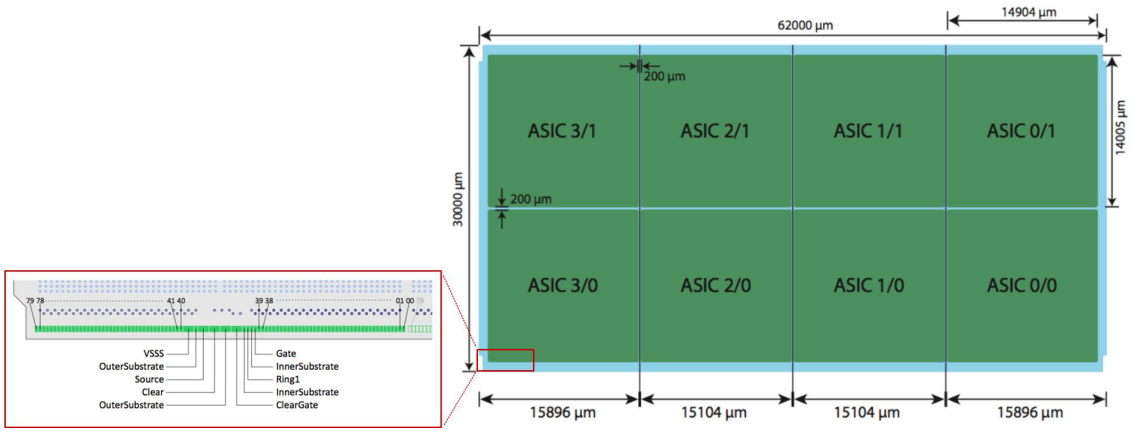
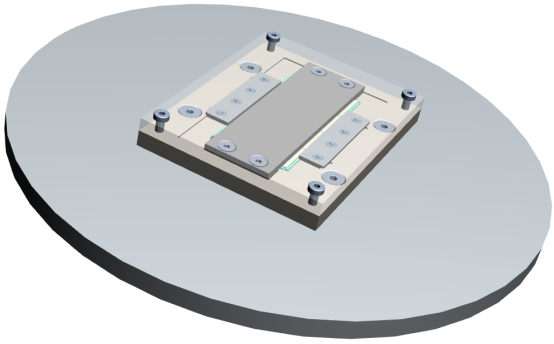
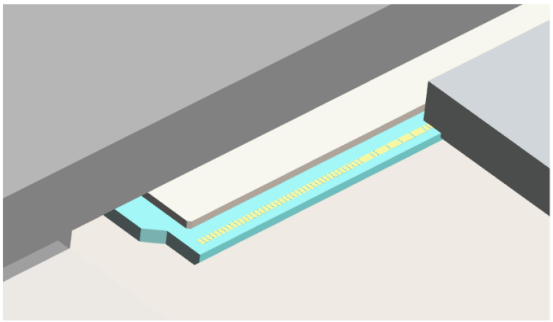


Figure 3.12: Block diagram of a bare module, with the row of 80 contacts on the ASIC.



(a) Storage container for a bare module.

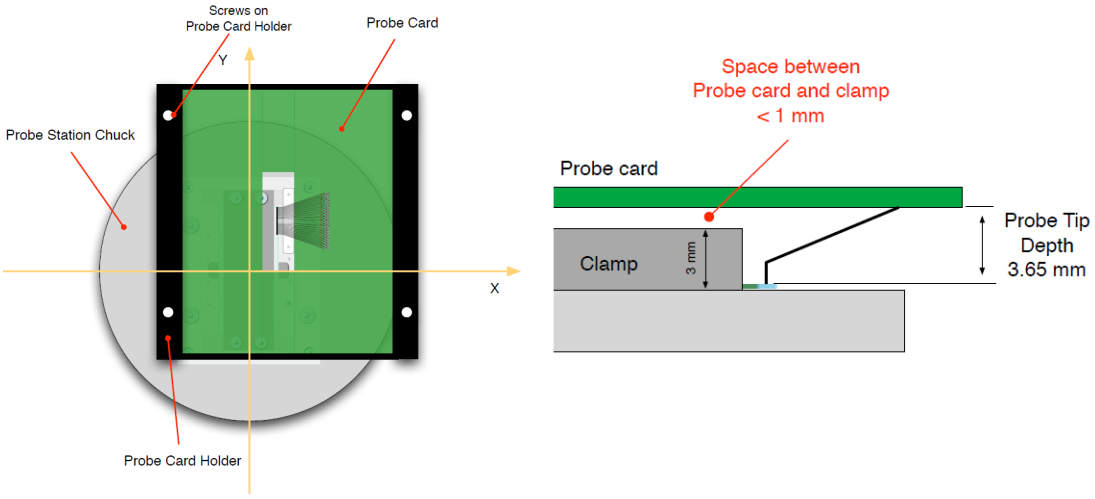


(b) Clamping of the bare module within the storage container.

Figure 3.13: Bare module holding setup.

The probe card designed for the bare module test activity features an array of 80 vias, with a diameter of 0.9 mm and a through hole diameter of 0.5 mm, which is used for the connection of the 80 tips to the ASIC through a rectangular aperture in the middle of the PCB (see Figure 3.14a). The probe card is connected, by means of a high speed edge card connector, to an FPGA board both for the control of the ASIC and for data acquisition. A regulator replacement board (RRB), connected on-top of the FPGA board, provides the digital, analog and ADC supply voltages. Thus for the ASIC tests a probe card holder, a Probe Card, one High Speed Cable, one Patch Board, one FPGA board, one Regulator Replacement Board, three power supplies, a multimeter, one Pulser Oscilloscope one oscilloscope and one laptop were used (see Figures 3.15a and 3.15b).

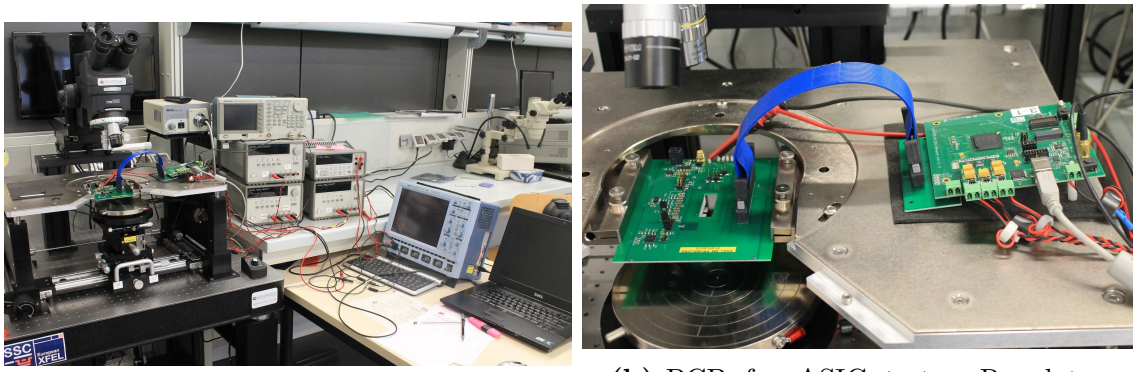
For what concerns tests on the sensor, back side current measurements were performed. The set-up of such tests is composed by three MA-8000 Manipulator In-



(a) Connection of the ASIC to the probe-card with an orientation along the y-axis of the probe station.

(b) Side view of the connection between the ASIC and the probe-card.

Figure 3.14: Connection between ASIC and probe-card.

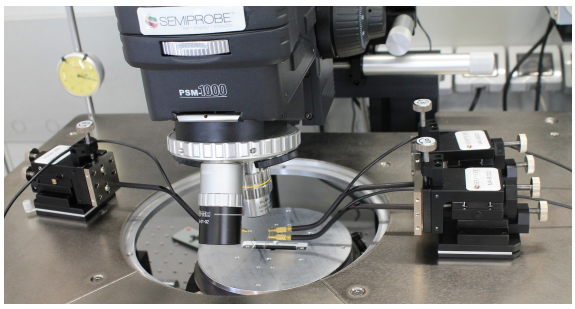


(a) ASIC tests intrumentations setup: three power supplies, one multimeter, one pulse generator, one oscilloscope and one laptop.

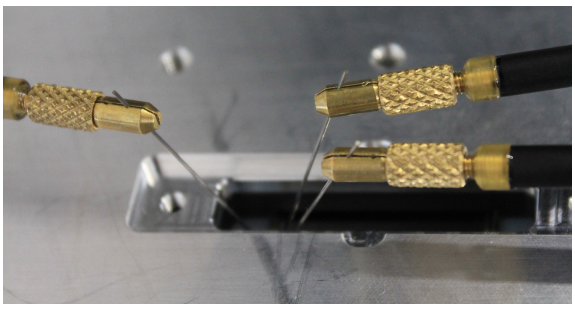
(b) PCB for ASIC tests: Regulator Board mounted on FPGA board, connected to Probe Card Board by means of high frequency cable (blue cable).

Figure 3.15: Overall setup for ASIC tests.

strumentation (Figures 3.16a and 3.16b), one SMU and two Multimeters.



(a) Three MA-8000 Manipulator Instrumentation on the platen of the Probe Station.



(b) View of the needles contacting the bare module in the storage container.

Figure 3.16: Setup for Back side current measurements: view of the instrumentations on the Probe Station.

3.3 Activity description

3.3.1 ASIC's Tests

When commissioning a new chip, some recommended basic functionality tests are indicated in the following:

- *Power Consumption*: it should be around 120 mA for the whole chip (combined on `VDDA`, `VDDD_ADC`, `VDDD_GL`).
- *Output Link*: the Master FSM can be put into `sSEND_TEST_PATTERN` in which the chip will permanently send a 10 bit test pattern. The test pattern can be configured via slow control and must have its MSB set.
- *JTAG*: putting the JTAG TAP controller into `sSHIFT_IR`, and injecting a known pattern at TDI, the pattern should appear after 5 (length of IR) clock cycles. After writing an instruction to the JTAG IR and moving to `sSHIFT_DR` afterwards, a pattern injected at TDI should appear at TDO after the length of the selected register in TCK clock cycles.
- *Pixel Control Shift Register*: if the Pixel Control register is selected through the JTAG IR, the Pixel Select register contains all zeroes, and the JTAG Tap controller is put into `sSHIFT_DR` a known pattern injected at TDI should appear at TDO after $8 \times 16 \times 34 = 4352$ clock cycles. If the last pixel is

selected through the Pixel Select register, the pattern should be visible afer 34 clock cycles (only the last pixel is then traversed).

- *Pixel Control Shift Register*: The XOR chain can be tested by flipping the `SC_GlXorIn` (located in the Global Control register). The `SC_XorOut` bits are sent within the trailor to the data when the chip is read out.

- *Bias Current*: connecting n pixels to the inject bus while the front end is not powered, n × the bias current can be sunk from the inject bus.

- *VHold*: When `DDYN_Iprog` is active (it is possible make it permanently active through the Master FSM config. register), the voltage on the VHold capacitor should change when the bias current is changed (if VHold is not saturated). VHold can be seen at the filter output during the bias current programming phase.

- *ADC Data Valid*: There are two ADC Data Valid (MeasOK) output signals connected to pads. When operating the `DDYN_ADC_RMP` signal correctly, this signal should change in time when the input signal to the ADC is varied. It should also vary if the ramp current is changed, which can be done through the control register (×2 and fine trim).

For some measurements, the pass/fail criterium is obvious (digital tests), for other tests, the typical measurement value must be determined iteratively by analyzing the scans of a larger number of chips (e.g. power supply currents). The tests can be divided in two groups:

- *Systematic Tests* checking one by one a certain feature, like configuration bit,SRAM cells, decouplig caps.

- *Overall Tests* run the chip in typical modes and check the correct operation like generation of test patterns or ADC sweep.

Table 3.2 shows the list of performed tests with a short description. When tests are repeated with different test patterns (mainly digital tests) the sub-tests are labelled A and B. If a crucial test fails significantly (e.g. supply current being way out of limit), further testing makes no sense and testing is aborted. The corrisponding 'stop' criterion is listed in the last column.

In order to performe all the tests 2 operative systems (with 32 and 64 bits) and 2 testing softwares (for IC2KAH-1C2LSH and VTBZLLH-VRBZM5H wafers) were used.

Test	Function	Details	Prel. Pass Criterion	Stop if
DIG1 A/B	JTAG	All register, only $VDDD\_GL$ on	all ok	≥ 1 error
DIG2 A/B	Pixel Register	Write in xy mode, read serially via JTAG, only $VDDD\_GL$ on	all ok	≥ 1 error
DIG3 A/B	SEU Chain	Toggle XOR input, read XOR output from JTAG register	all ok	≥ 1 error
DIG4 A/B	Output link & state machine	Send test pattern, enable via telegram	correct	error
DIG5 A/B	Matrix SRAM	Write/read 010/1010 pattern (or 0000/1111)	< 1000 errors	-
DIG6	Sequencer Holder	Hit two ExtLatch points with hold functionality	all ok	≥ 1 error
PW1	Supply current reset	Decoupling caps must first be programmed to harmless ststes	< 50 mA	-
PW2	Supply current idle state	All supplies and clock active but all pixels off	< 50 mA	-
PW3	Supply current operation	All pixels on, 1% duty cycle	< 100 mA ($VDDD\_GL$)	-
PW4	Decoupling caps	Use decoupling caps self test feature	-	-
P1	Perifery DAC	Check few points with multimeter. Static analog power, pixels off	-	-
ADC1 A/B	GCC start values	Use instant ExtLatch for all bits	all ok	≥ 1 error
ADC2	ExtLatch scan	Use ExtLatch via XDATA to latch every timestamp in one burst	-	-
ADC4	ADC ramp current	Measure ADC value at 2–4 fixed periphery DAC values for all current, all pixels	-	-
FE1	Basic compensation DAC	Check correct BG DC current compensation for all DAC bits, digitize VHold with pixel ADC	-	-
FE2	Basic FCF function, injection	Check linear BG current injection for each bit	-	-
FE3	Gain settings	Check gain with all four filter feedback caps	-	-
FE4	Day 0	Basic functionality - bias with periphery DAC and check few points with BG injection	-	-

Table 3.2: Performed Chip Tests.

As already mentioned, a Regulator Replacement Board was used in order to correctly bias the DSSC Chip. Such RRB presents three different supplies voltages called Analog, Global and ADC. Each line has a Sense and Force terminals, used in order to deliver significant current at accurate voltage, i.e. 1.3 V. Each lines has its own ground, thus resulting in 12 different nets going from RRB to PC board, then on the chip. One of the faced challanges was the effect of ASIC biases sensed at chip or at probe card level. The chip has been designed in order to have Force and Sense terminals shorted at chip level, when the chip is biased correctly, but in the bare module tests setup such terminals can be shorted also at Probe Card level (by means of 6 jumpers on the probe card). If Force and Sense were shorted at Probe Card level, good digital tests results (i.e. well reproducible) were obtained but poor analog tests resuts could be achieved. On the contrary, with Force and Sense shorted at ASIC level, poor digital tests results (i.e. not reproducible) and acceptable analog tests results were obtained, if and only if the digital part worked properly. After some attempts a good compromise with the following configuration was found:

- VDDA, VSSA, VDDD_ADC and VSSD_ADC sensed at ASIC level;
- VDDD_GL and VSSD_GL sensed at Probe Card level.

It is possible deduce that the different behavior observed with the different configurations is likely to be ascribed to the series parasitic resistance on the force lines and that VDDD_GL and VSSD_GL seem to be the most critical.

In order to investigate this phenomena, simulations of the RRB channel have been performed with LTSpice software. Each channel of the RRB has been simulated in two different conditions:

- original schematic of the single biasing line (see Figure 3.17),
- improved schematic with parasitic resistances in addiction (3.18).

The channel has been operated in static current around $25 - 30\,\mathrm{mA}$ and $100\,\mathrm{mA}$ in $4.5\,\mathrm{MHz}$. After simulations, the effective voltage across the ASIC has been monitored. Figures 3.19a and 3.19b show respectively the two different simulations compared with an actual measurement of VDDA during ADC1 test. This comparison highlights that there is an actual variation of $\sim 100\,\mathrm{mV}$ on the bias line, that implies the presence of a $0.5\,\Omega$ series parasitic resistance.

It is clear that the correct sensing of the applied voltage is a critical issue, in fact if the sense terminal is not well connected, the ASIC can experiment very high voltage

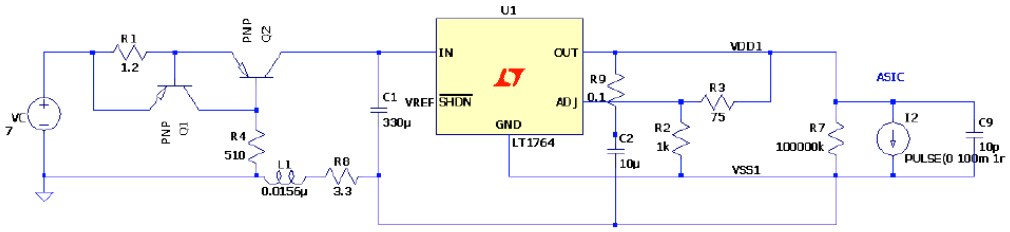


Figure 3.17: Channel without series parasitic resistances.

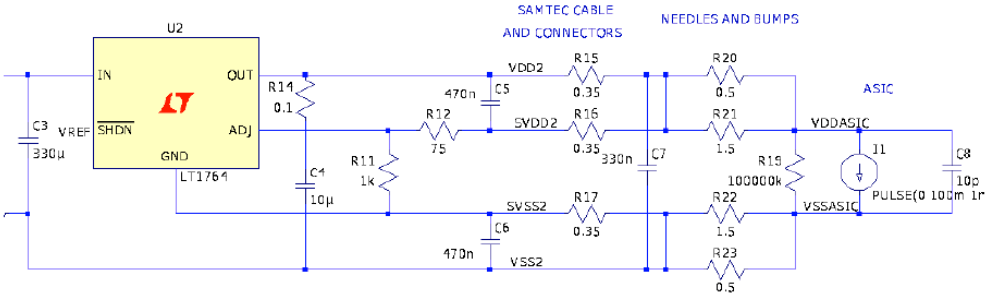
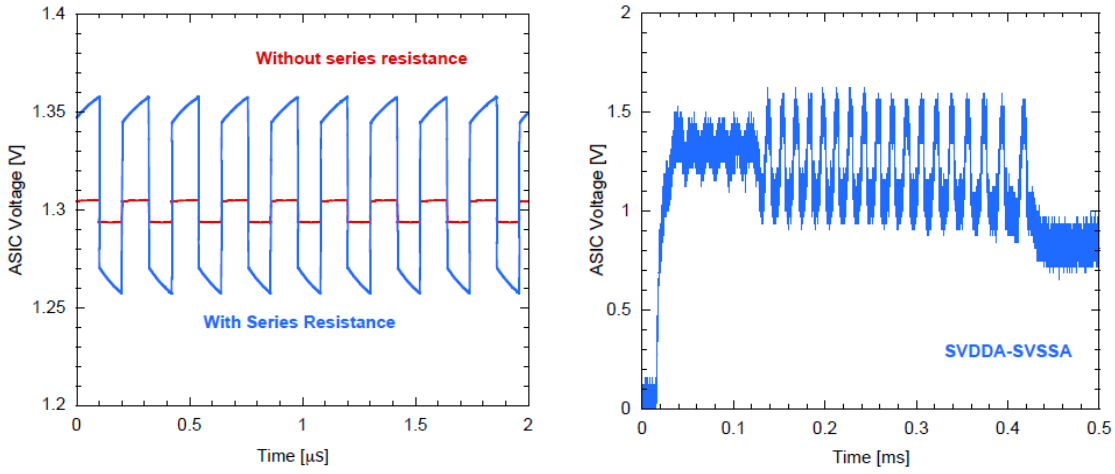


Figure 3.18: Channel with series parasitic resistances (improved model).



(a) Data from simulations.

(b) Actual measurements.

Figure 3.19: ADC1 test: comparison between simulations and actual measurements.

variations. In order to avoid damages (while keeping the advantages of sensing at ASIC) it is proposed to place two resistances ($R_7 = R_{18} = 10\,\Omega$) in parallel to the two capacitances of 470 nF, Figure 3.20, for the F2 mass production.

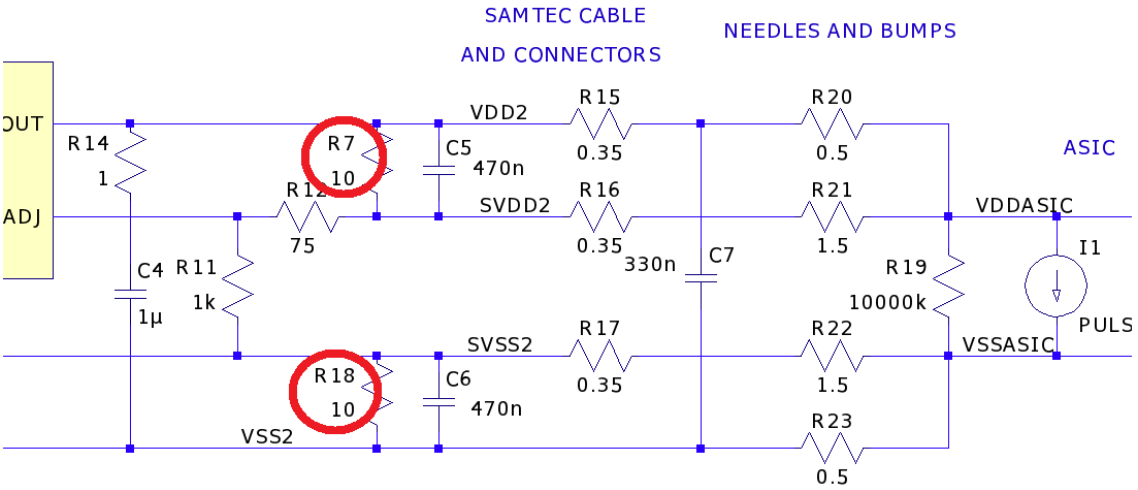


Figure 3.20: Possible solution for the correct sensing of the applied voltage issue

3.3.2 MiniSDD and PXD8 ASIC's test results

The digital and power tests can be evalutated very easily, whereas the evaluation of the more complex ADC and FE tests show no ASIC with perfect performance.

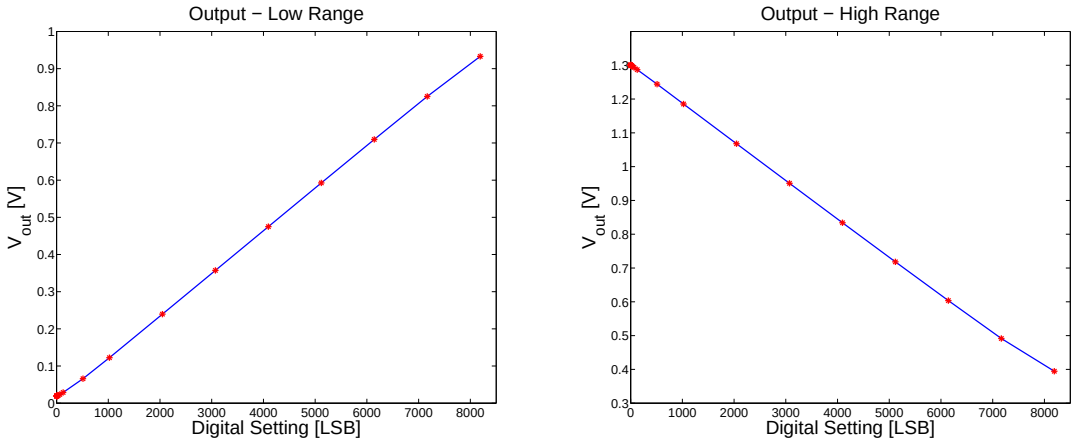
Tests have shown that out of the 37 ASICs tested, 9 failed during the overall digital tests. In most cases, when the pixel register or the JTAG register could not be written and read back correctly, the overall digital tests failed. Different considerations have to be taken into account regarding DIG5 SRAM test. On a single F1 die, there can be $4096 \times 800 = 3276800$ SRAM words of 9 bit width. Corrupt memory cells can be marked as invalid in the readout chain. The success of the test, in this case, is considered when the chip presents less than 1000 or 0.03% defect SRAM words.

The periphery DAC is supposed to show a linear relationship between applied digital setting and output voltage in two output voltage ranges, called low and high range (see Figures 3.21a and 3.21b), according to Table 3.3.

In the ADC2 test, the digital part of the ADC is tested by applying an extlatch signal from an external pulser. By shifting the extlatch signal for each cycle, it is possible to try to latch each of the 256 gray counter timestamps. Ideally, we expect that every pixel is able to latch every timestamp, so $4096 \times 256 = 1048576$

Parameters	Lower Limit	Upper Limit
High Range Offset	1.25 V	1.35 V
Low Range Offset	0 V	0.1 V
Slope (high range)	−0.12 mV/LSB	−0.1 mV/LSB
Slope (low range)	0.1 mV/LSB	0.12 mV/LSB

Table 3.3: Periphery DAC evaluation parameters.



(a) Low Range. **(b)** High Range.

Figure 3.21: Example characteristics of the periphery DAC (Example characteristics of the periphery DAC (Wafer 1C2KAH, Reticle G2)).

timestamps are checked. The success of the test, in this case, is considered when the chip presents less than 1000 missed timestamps.

In order to check each pixel delay bit, in ADC3 test, the output voltage of the on-chip DAC has been digitized for each delay setting. From theory a small shift of the mean digitized value to higher values for each delay step is expected, covering approximately 1 ADU (fine) and 2.5 ADU (coarse).

For the ramp current test, ADC4, several settings of the on-chip DAC are digitized by the in-pixel ADCs. A binary sweep of the ramp currents is done by activating each of the 6 control bits once. Increasing the ramp current by activating a higher-order control bit should result in dropping ADC counts. In total, $4096 \times 6 = 24576$ ramp current settings are checked. The main problem of this test is that, unlikely all other tests, it requires a 64 bit operative system, thus it was not always possible to perform it.

In bias compensation test (FE1), for each DC bias current from the BG injection circuit, a suitable bias compensation DAC setting is searched. The resulting VHold voltage is digitized and checked to be in the valid range of 30 to 200 ADU. This range is very broad to cope with the uncalibrated ADCs.

In basic function, injection test, FE2, each Depfet frontend is checked by applying a bias current and a varying signal current from the pixel injection circuit.

In gain settings test, FE3, each feedback capacitor is checked independently. Smaller capacitor values are expected to result in a higher frontend gain.

The day-0 frontend is tested by applying a bias voltage from the DAC at the nominal bias point, FE4 test. Using the *Bergamo charge injection circuit* in high gain mode, the nonlinear characteristic of each pixel is scanned. Each pixel frontend is using all four feedback capacitors available. The *Bergamo charge injected circuit*, designed by Microelectronic group of the University of Bergamo, is a network able to simulate the large input dynamic range expected at European XFEL [40] [41].

The following two tables (Tab 3.4 and Tab 3.5) show the two test results summaries of MiniSDD and PXD8 ASIC's tests, respectively. In green there are the positive results, in red the negative results and in gray the not performed tests. It is possible to conclude that for digital, power consumption and perifery tests no big problems were observed, whereas for the Front End and ADC tests the issue is more critical. PXD8 tests were performed with an improved version of the software, in fact more Front Ened and ADC tests are positive.

Sensor ID	DIG1	DIG2	DIG3	DIG4	DIG5	DIG6	PW1	PW2	PW3	PW4	ADC1	ADC2	ADC3	ADC4	P1	FE1	FE2	FE3	FE4
IC2KAH-G2																			
IC2KAH-G3																			
IC2KAH-D6																			
IC2KAH-D7																			
IC2KAH-C7																			
IC2KAH-D5																			
IC2KAH-D4																			
IC2LSH-D5																			
VTBZLLH-B1																			
IC2LSH-E4																			
IC2LSH-E3																			

Table 3.4: MiniSDD test results.

Despite this improvement of the software, ADC3 test ("Shift of the pixel delay circuit measurements for all pixels") results always negative. In fact a possible explanation is that probably there is some loss of the ADC supply voltage, infact F1 bias voltages are generated by the RRB (blue circle in Figure 3.22) mounted on

	Sensor ID	DIG1	DIG2	DIG3	DIG4	DIG5	DIG6	PW1	PW2	PW3	PW4	ADC1	ADC2	ADC3	ADC4	P1	FE1	FE2	FE3	FE4
W44-F12	IC2LSH-H4																			
	IC2LSH-H5																			
	IC2LSH-H6																			
	IC2LSH-H7																			
	IC2LSH-H3																			
	IC2LSH-H1																			
	IC2LSH-G2																			
	IC2LSH-G3																			
W50-H13	IC2KAH-G6																			
	IC2KAH-G5																			
	IC2KAH-G6																			
	IC2KAH-F8																			
	IC2KAH-F6																			
	IC2KAH-F5																			
	IC2KAH-F1																			
	IC2KAH-E9																			
W50-F12	IC2KAH-D0																			
	IC2KAH-E5																			
	IC2KAH-E4																			
	IC2KAH-E3																			
	IC2KAH-E1																			
	IC2KAH-D1																			
	IC2KAH-C1																			
	IC2KAH-B1																			
	VTBZLLH-B5																			
	VTBZLLH-B3																			

Table 3.5: PXD8 test results.

the FPGA board. Thus force and sense lines propagate throughout 4 connectors, the patch board, the 25 cm-long high-speed cable, the probe card and the tips. In order to introduce a minor loss in the signal, the Regulator Replacment Board was moved closer to the Probe Card, as shown in Figure 3.23.

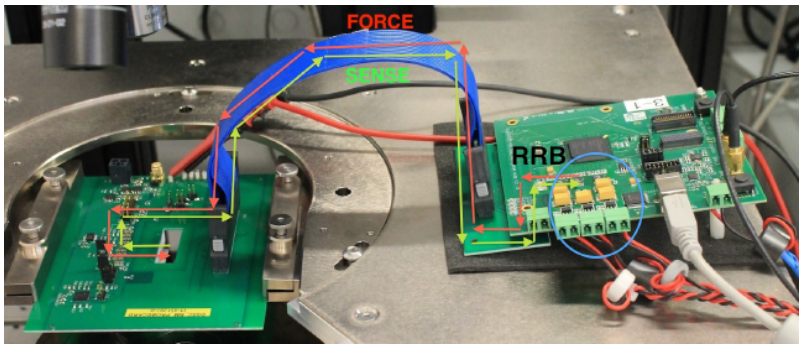


Figure 3.22: Old ASIC's tests set-up.

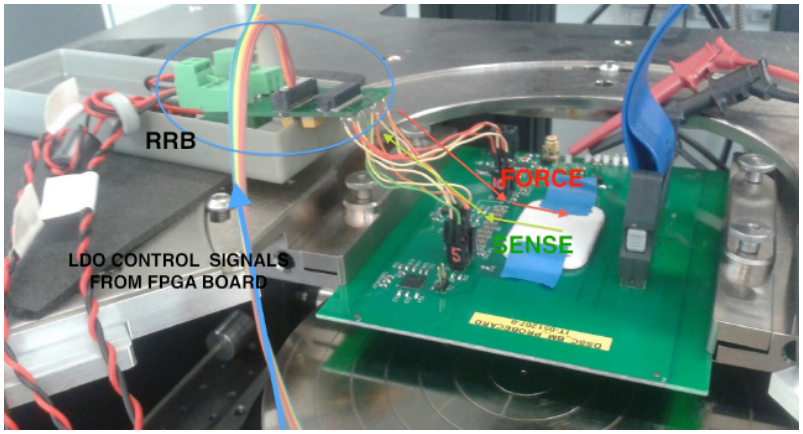
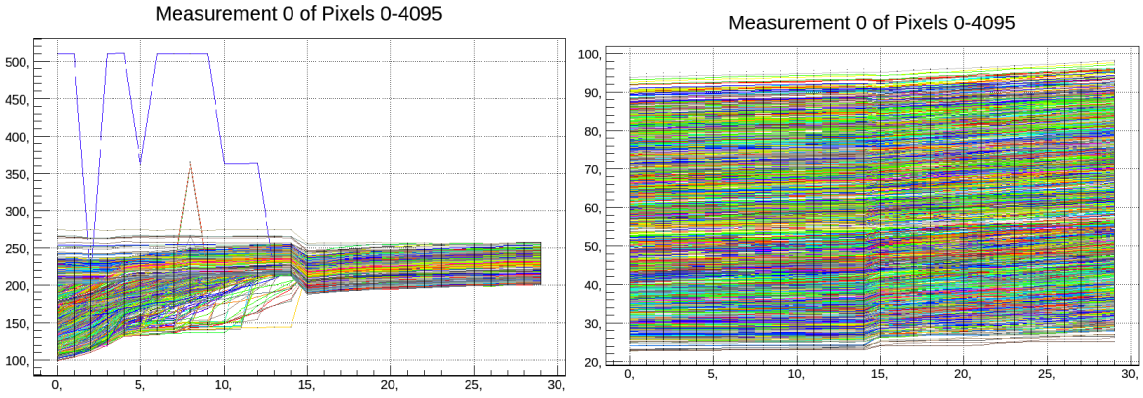


Figure 3.23: New ASIC's tests set-up.

After this adjustment, all tests were performed again on some devices. Digital, power consumption and perifery tests still worked correctly, whereas ADC3 test and Front End tests showed a remarkable improvement as depicted in Figures 3.24a, 3.24b, 3.25a, 3.25b, 3.26a, 3.26b, 3.27a and 3.27b.

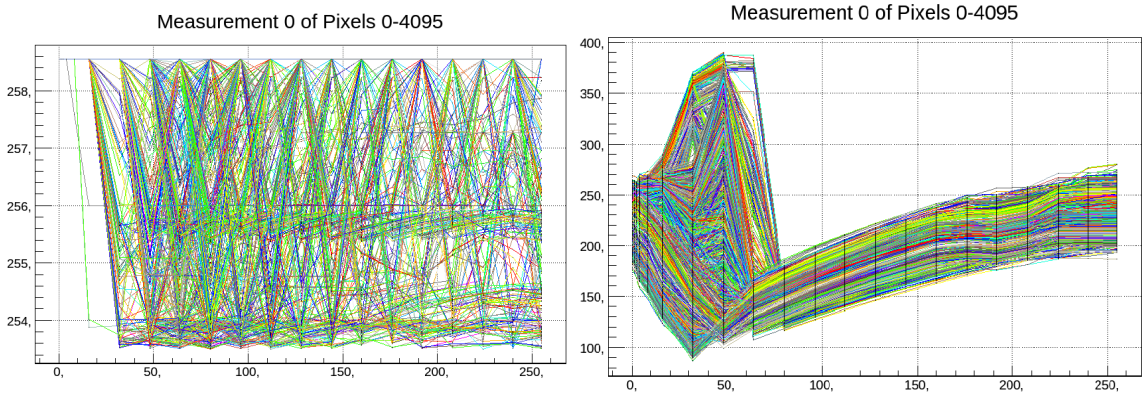
Clearly the results obtained are promising, thus we conclude that it could have been helpful to produce a new Probe Card with connectors to directly mount the Replacement Regulator Board and take advantage of the unused lines on the high-speed cable in order to propagate the LDO control signals.

A new Probe Card, with connectors for the Regulator Board (Figure 3.28), has already been designed ,by means of the software Eagle, and produced for the testing of F2 mass production bare modules.



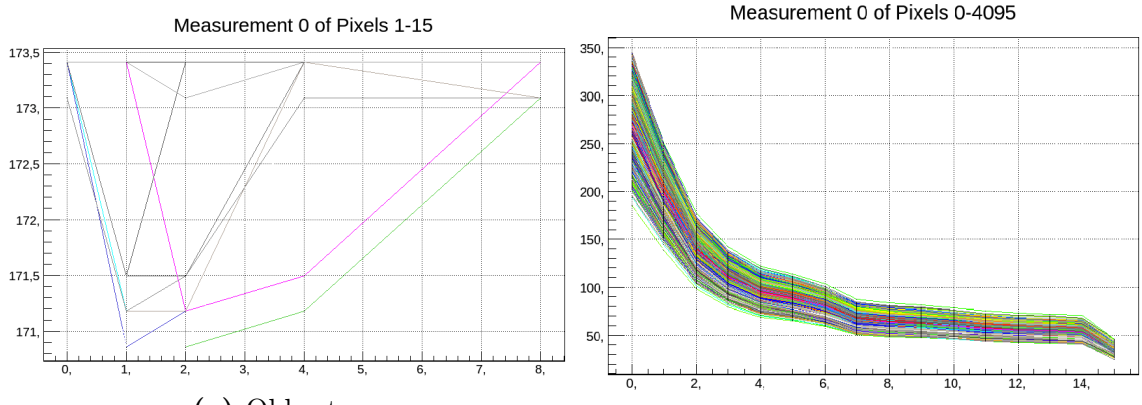
(a) Old setup. **(b)** New setup.

Figure 3.24: ADC3: shift of the pixel delay circuit measurement for all pixels.



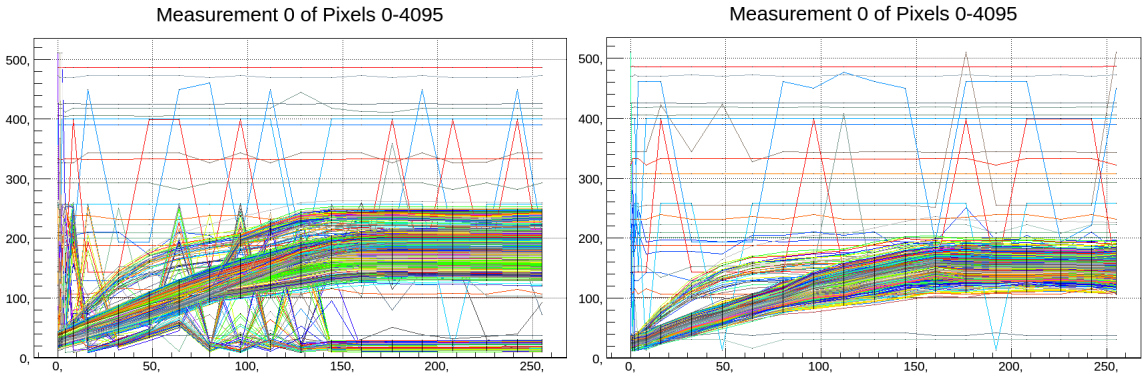
(a) Old setup. **(b)** New setup.

Figure 3.25: FE2: signal injection in DEPFET mode, checked using the BG injection circuit.



(a) Old setup. **(b)** New setup.

Figure 3.26: FE3: frontend gain variation due to different filter feedback capacitors.



(a) Old setup. **(b)** New setup.

Figure 3.27: FE4: Day 0 FE is checked with one bias setting, nonlinear mode, high gain injection.

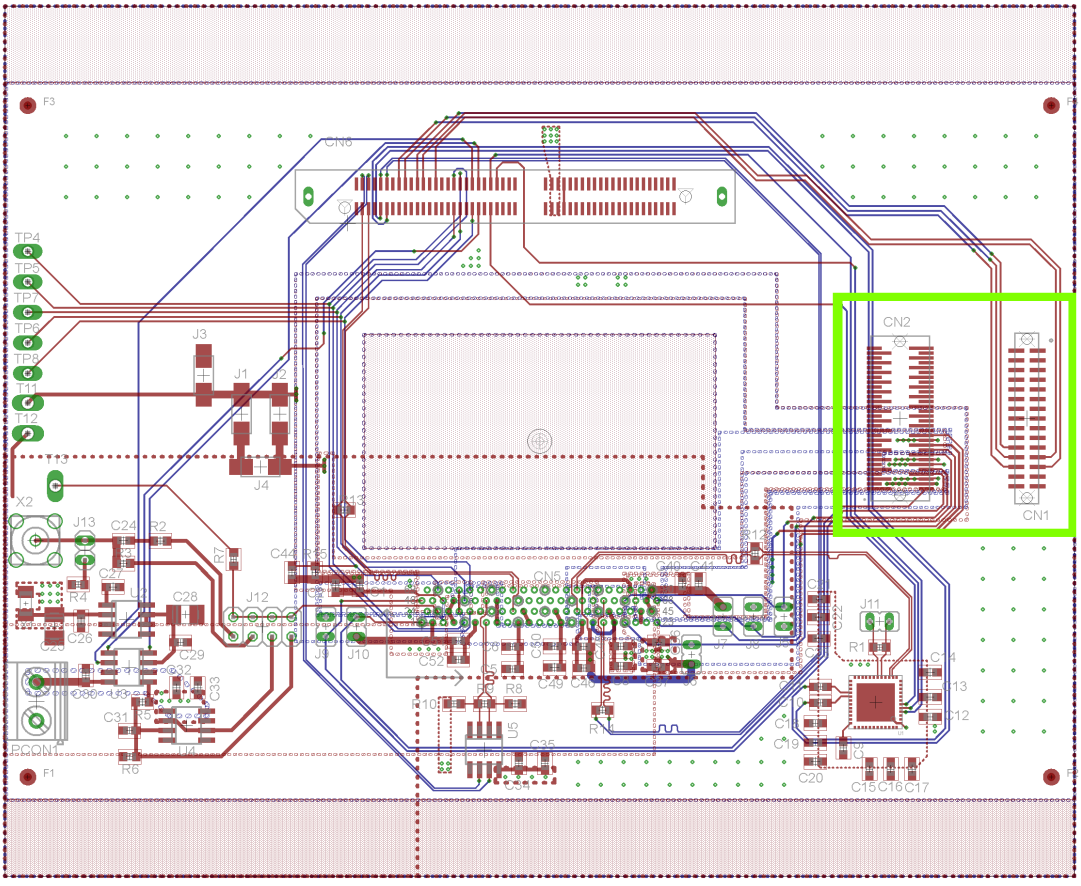


Figure 3.28: PC new layout: in the green box the two connectors addeded in order to mount directly the RRB on the PC.

3.3.3 I/V Tests - Dark Current

Dark current given by the relatively small amount of charge carriers that flows through an insulating region of photosensitive devices even though no outside radia-

tion is entering the detector. This current loss rises exponentially when the insulating region thickness decreases. Ideally, within the depletion region all free charges should be removed from the junction. However crystallographic defects within the depletion region make a random generation of electrons and holes possible. Also thermal excitation could enhance the passage of electrons. Depending on the nature of the detector, the magnitude of the back side current can goes from the order of nanoAmpere to microAmpere. The reverse biasing of the DSSC increases the dark current without much change in the photocurrent, thus a study of backside current as a function of the reverse bias voltage is needed. As already said in section 3.2, three MA-8000 Manipulator Instrumentation, one SMU, two Multimeters and one laptop were used in order to perform I/V measurements. All those instruments were used, adopting the configuration scheme reported in Figure 3.29:

- Agilent B2961 SMU: biases Cutting Edge net (substrate) troughout one of three needles and reads the erogated current;

- Two Agilent 34401 DMM: read the voltage drop trough two resistances ($R = 1\,\mathrm{M}\Omega$) connected respectively to Back Contact net and Back Frame net troughout the other two needles.

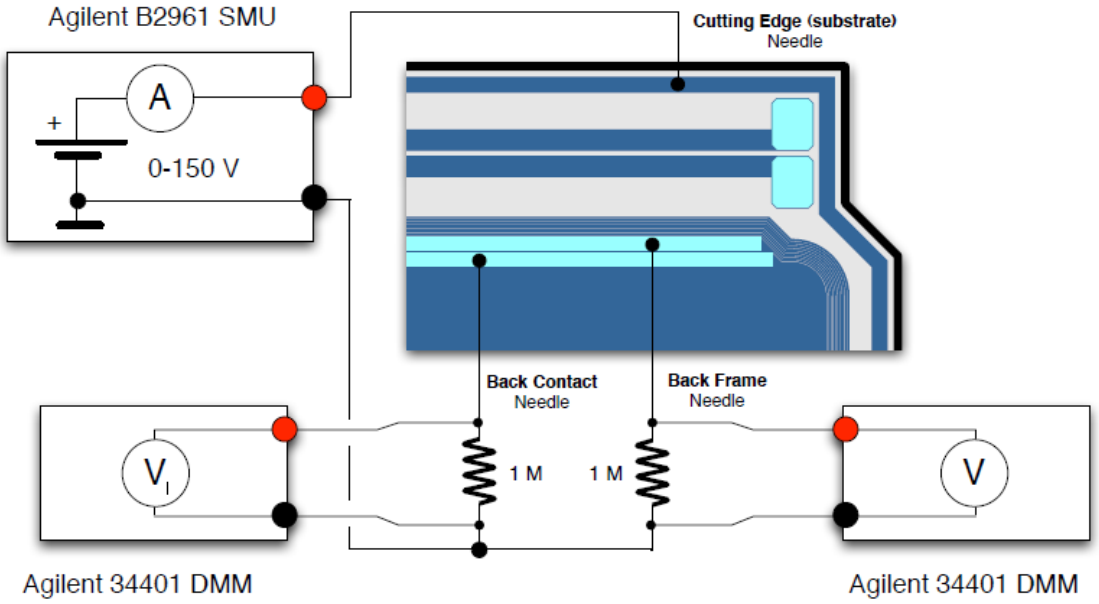


Figure 3.29: Scheme of the connections for the back side current measurements.

3.3.4 MiniSDD and PXD8 I/V Tests

Figure 3.30 shows the connection directly on the sensor net seen with the 3-Megapixel camera of the Probe Station. Measurements were performed biasing the sensor from

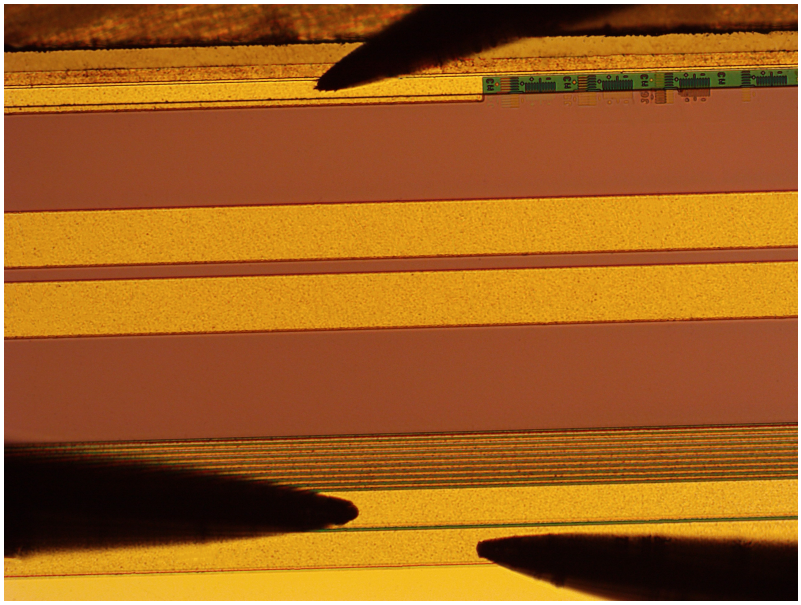


Figure 3.30: Scheme of the connections for the back side current measurements.

0 V to 150 V. Figure 3.31 shows Back Contact Current measurements results as a function of Reverse Bias Voltage. It is possible observe an exponential increase of this current for a reverse bias voltage greater than 120 V. Such behavior can be ascribed to the bump bonding process, infact before bumpbonding, the sensor showed a backside current of approximately x. All measurements were performed in a dark box in order to minimize external noise due to the light. Table 3.6 shows mean values of Back Contact Current over all MiniSDD sensor.

Voltage Bias	**Mean Value [nA]**
100 V	0.41 ± 0.07
150 V	16.88 ± 3.55

Table 3.6: Mean Values of Back Contact Current of all MiniSDD sensors.

On the other hand measurements on PXD8 bare module were not performed in a dark box, but only in a almost dark enviroment. Figure 3.32 shows Back Side Current measurement function of reverse bias voltage for three different bare module (W44-S03, W44-S13 and W44-F12). Even though these measurements are expected to be at least 8 times higher than MiniSDD backside current, a comparison with MiniSDD measurements highlights that the pixels sensor are detecting some

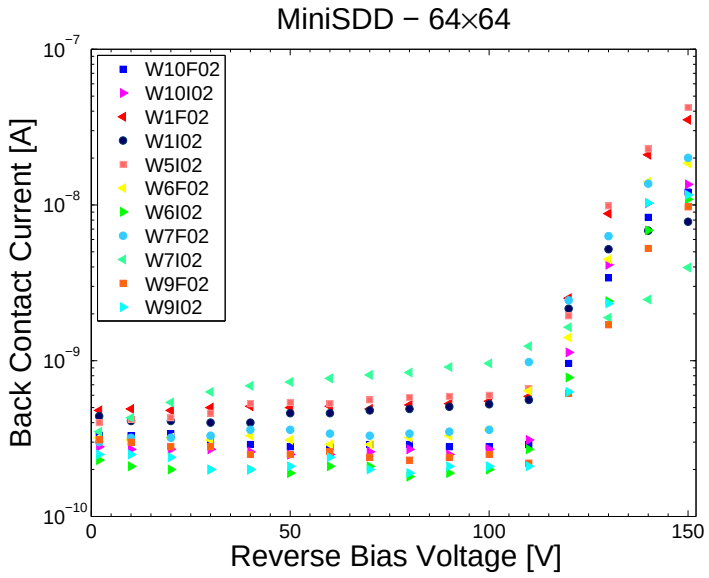


Figure 3.31: Back Contact Current measurements results function of Reverse Bias Voltage.

light. Table 3.7 reports the comparison between back side current before and after the bumpbondign procedure. At this point it is not possible to conclude that the increase of the back side current is striclty due to the bumpbonding for PXD8 sensors. For F2 mass production a dark box for 4×2 chip sensors back side current measurements is needed.

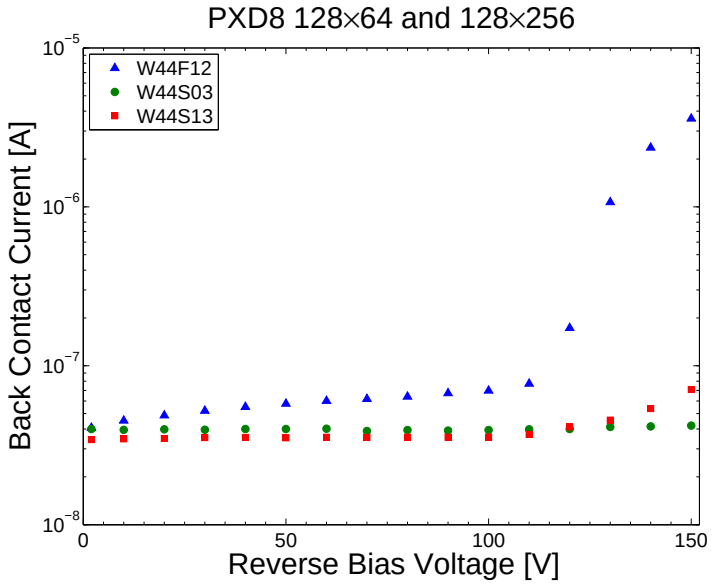


Figure 3.32: Back Contact Current measurements results function of Reverse Bias Voltage.

	Reverse Bias Voltage [V]	Back Contact Current [nA] Before bumpbonding	After bumpbonding
W44-S03	100	0.45	34.9
	150	2.26	49.0
W44-S13	100	1.5	35.6
	150	24.8	70.9
W44-F12	100	37.0	69.7
	150	6300	3590

Table 3.7: Back Contact Current Values before and after bumpbonding process.

3.4 Discussion

A detailed characterization of silicon pixel detectors for DSSC project at European XFEL has been performed. The chapter reports the study of the readout ASIC functionality, in terms of Digital functionality, PoWer consumption, Periferal logic, ADC and Front-End test, and the backside current of the first prototype of the DSSC bare modules. This activity led to the optimization of the complex setup that will be used for the characterization of the next generation mass production bare modules F2. In fact a substantial change have been implemented to the ASIC test setup. With the Regulator Replacement Board on the Probe Card PCB, the voltage bias is much more stable and faling ASIC test are now much more stable. Another key requirement for a good characterization of the final chip is the presence of a dark box for the backside current measurements.

Conclusions

In this thesis work all the fundamental steps for realization of an analog readout channel of a radiation detector were carried out in detail:

- characterization of a CMOS nanoscale technology that are today used for the design of analog channels in state-of-the-art pixel detector readout chips;
- desing and simulation of the semiconductor detector low-noise analog readout channel;
- characterization and validation of of a full mixed-signal readout chip bonded to a pixel sensor.

First of all a deep analysis of ionizing radiation tolerance of 65 nm and 110 nm CMOS technology was carried out. A set of test devices 110 nm UMC technology and 65 nm TSMC technology were irradiated up to 5 Mrad and 600 Mrad and studied.

It is possible conclude that for what concernes 110 nm UMC technology a large degree of tolerance up to Total Ionizing Dose of 5 Mrad is observed. This behaviour might be ascribed to the thin gate oxide typical of transistors in modern CMOS technologies. Little threshold voltage shift and negligible transconductance decrease were detected either for Core, Enclosed Layout and I/O devices. Despite there was almost no change in static characteristics, it is possible to observe a degradation of the low-frequency noise. In particular at 5 Mrad, PMOSFET devices show a Lorentzian noise term, instead NMOSFETs exhibit a moderate increase of 1/f noise at low current density. Overall, these result lead to the conclusion that this technology is suitable for the design of analog circuits with a good degree of radiation tolerance up to first step of 5 Mrad total dose. Further irradiation steps are programmed in order to study effects up to 10 and 50 Mrad TID. It is useful to remind that this technology is being used for readout chips in X-ray imaging [42] and in particle detection, where the capability of tolerating doses of several tens of Mrad is an essential requirement.

The 65 nm CMOS process is presently used by the international collaboration RD53 for the design of a new integrated circuit for the readout of the innermost

layer of pixel sensors in the ATLAS and CMS experiments at the High Luminosity LHC. Among other demanding requirements, this chip will have to stand extremely high doses of ionizing radiation, up to 1 Grad. 65 nm TSMC devices show a good degree of tolerance to ionizing radiation up to a total dose of 600 Mrad. Negligible transconductance increase was detected for all devices. A threshold voltage shift lesser than 40 mV is detected. With increasing TID, NMOS devices show an inversion of the $I_D - V_{GS}$ characteristic. This effect can be ascribed to the fact that at low TID, positive charge in STI oxides switches on lateral devices, increasing I_D for the same V_{GS} and reducing threshold voltage value. At higher doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge, switching off lateral parasitic transistors and reducing I_D for the same V_{GS}, increasing threshold voltage value. For both NMOSFET and PMOSFET no effect is detected in the white noise region. Despite of good results in white noise region, the effect of 1/f noise increase can be nonnegligible both for N-channel and P-channel devices. In particular, for what concerns NMOS devices, at 600 Mrad the 1/f noise coefficient increases by a factor 3 at low currents. Regarding PMOS devices, at 600 Mrad the 1/f noise coefficient increases by about a factor 2. Unlike 110 nm UMC technology no Lorentzian component is visible after irradiations. One further irradiation step is programmed in order to study effects up to 1 Grad TID.

During the second part of the thesis, the first block of the analog readout channel, i.e. the Charge Sensitive preAmplifier, for a novel cosmic antideuteron detector for GAPS project has been designed and simulated. The preamplifier is composed by three stages: forward gain stage, transconductance stage and feedback MOS capacitance. Each block were studied in detail. The preamplifier presents a non-linearity transfer characteristic due to the dynamic signal compression technique. Such technique was implemented both to satisfy the double gain requirements imposed by the experiment and to cover wide energy range expected in a relatively low voltage bias (1.8 V). A gain of 200 $\mu V/keV$ in low energy range and 4.5 $\mu V/keV$ in high energy range has been obtained, that implies an otuput dynamic range lower than 500 mV. Another key characteristic of the CSA is that, assuming a detector capacitance of 40 pF, a simulated energy resolution lesser than 4 keV: the limit of 4 keV was a strict requirement setted by the experiment.

Last but not least, a detailed characterization of silicon pixel detectors for DSSC project at European XFEL has been performed. Chapter 3 reports the study of the readout ASIC functionality, in terms of Digital, PoWer consumption, Perifery, ADC and Front-End test, and the backside current of the first prototype of the DSSC bare modules. This activity led to the optimization of the complex setup that will be

used for the characterization of the next generation mass production bare modules F2. In fact a substantial change have been implemented to the ASIC test setup. With the Regulator Replacement Board on the Probe Card PCB, the voltage bias is much more stable and faling ASIC test are now much more stable. Another key requirement for a good characterization of the final chip is the presence of a dark box for the backside current measurements.

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