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Total Ionizing Dose effects on a 28 nm Hi-K metal-gate CMOS technology up to 1 Grad

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Abstract: This paper presents the results of an irradiation study on single transistors manufactured in a 28 nm high-k commercial CMOS technology up to 1 Grad. Both nMOSFET and pMOSFET transistors have been irradiated and electrical parameters have been measured. For nMOSFETs, the leakage current shows an increase of 2–3 orders of magnitude, while only moderate degradation for other parameters has been observed. For pMOSFETs, a more severe degradation of parameters has been measured, especially in the drain current. This work is relevant as the evaluation of a new generation of CMOS technologies to be used in future HEP experiments.

Keywords: Radiation-hard electronics; Front-end electronics for detector readout

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Contents

1 Introduction

Microelectronic readout integrated circuits (IC) and advanced micro-systems are key parts for successful high energy physics (HEP) experiments, as well as for many other scientific applications (space experiments, medical instrumentation, etc). For this reason, an optimal IC design, depending on the application, is required for high performance, low power and low system cost.

The present paper will present the results of an irradiation study up to 1Grad on single transistor test structures on a 28 nm high-k (high dielectric constant k) commercial CMOS technology which is being investigated in terms of signal process quality, power consumption and radiation hardness for applications in instrumentation electronics for particle physics. As a matter of fact, the HEP community could benefit from the intrinsic low power consumption and large scale integration potentiality offered by this technology node.

The paper is organized as follows: after the description of the test structures and of the setup in section 2, a review of measurements on MOSFETs is presented (section 3 for nMOSFETs and section 4 for pMOSFETs), with a discussion on the presented results.

2 Test setup

2.1 Test structure description

A test chip with different kinds of test structures has been designed and produced. It contains six sets of different structures:

- 10 core nMOSFET, standard V_{th};
- 10 core nMOSFET, high V_{th};
- 10 core pMOSFET, standard V_{th};

- 10 core pMOSFET, high V_{th};
- few more core nMOSFETs, standard V_{th} (for analysis of device to device matching, multi-finger MOSFETs, and to study different Electrostatic Discharge (ESD) protection approaches);
- I/O nMOSFET and pMOSFET, diodes, capacitors.

Core transistors are those implemented in the core of chips (as the name suggests), while I/O interface transistors are used at the periphery of chips and are more robust (the gate oxide is thicker), since they are in direct contact with the external world.

Most of structures have ESD protection structures made of diodes; only a few have no ESD protection at all or ESD protection implemented by MOS structures.

I/O pads are arranged in 6 rows of 24 pads each. All designed transistors have a linear layout since the design rules of 28 nm technology do not allow Enclosed Layout Transistors (ELT) [1–3].

The first four sets contain single core transistors (both n-channel and p-channel, in standard and high V_{th}), with different geometries and diode-based ESD protection; transistors belonging to the same set share the same substrate, source and n-well contacts, while drain and gate contacts are accessible for each individual device. The different geometries available (W is the width, L the length of the gate channel) are listed in table 1.

Table 1. Geometries implemented for single transistor test structures.

	Tr#1	**Tr#2**	**Tr#3**	**Tr#4**	**Tr#5**	**Tr#6**	**Tr#7**	**Tr#8**	**Tr#9**	**Tr#10**
W	3 μm	3 μm	100 nm	1 μm	1 μm	1 μm	400 nm	200 nm	300 nm	100 nm
L	1 μm	30 nm	1 μm	30 nm	60 nm	90 nm	1 μm	1 μm	30 nm	30 nm

The two sets of standard V_{th} devices (nMOSFET and pMOSFET) have been irradiated and characterized up to 1 Grad.

2.2 Measurement setup

The Total Ionizing Dose (TID) tests have been carried out at the X-ray facility installed at the Physics and Astronomy Department of the University of Padova [4]. The X-ray source is the RP-149 Semiconductor Irradiation System from Seifert, with the tube biased at 40 kV. The naked chip was mounted on a semi-automatic 4-inch wafer probe station within the X-ray irradiation cabinet and contacted by a custom probe card. The probe card features 32 probe tips (two columns of 16). A Keithley 707 switching matrix connects the four Single-Measuring-Units (SMUs) of the semiconductor device analyzer (HP4156) and the voltage supply to specific probe tips. In this way, the selected set of structures could be properly biased during irradiation and measurements. Given the limitation in the number of connections available in the switching matrix, only one set of transistors could be biased and irradiated at a time. This meant that we performed the irradiation study on different dies for nMOSFETs and pMOSFETs.

The chip was placed as close as possible to the tube exit in order to maximize the dose rate, which could be set at 8Mrad/h in SiO_2. During irradiations the devices were kept in the worst case bias conditions found for the 65 nm technology [5], i.e. with both drain and gate biased, while source and bulk were shorted to ground. For nMOSFETs the conditions were $V_{ds} = V_{gs} = 1.1$ V; for

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nMOSFET $V_{ds} = V_{gs} = -1.1$ V. The value 1.1 V is 10% more than the technology nominal supply voltage and has been chosen since it maximizes the damage (+10% is the maximum tolerable value guaranteed by the foundry). Irradiations were performed at room temperature up to 1 Grad, in steps. Measurements were taken before irradiation and after each dose step. The whole setup was remotely controlled, so that the sequence of irradiation and measurements could be performed automatically. No annealing was performed afterwards, given limitations to the available setup.

3 nMOSFET irradiations

In figure 1 the I_d-V_{gs} curve in the linear region ($V_{ds} = 0.1$ V) are shown for two transistors with contrasting geometries. On the left, the characteristics is shown for a transistor with minimum gate length ($L = 30$ nm) but with a large width ($W = 3\ \mu$m); on the right, the same curve for a transistor with a long channel ($L = 1\ \mu$m), but narrow ($W = 100$ nm). The two devices behave very differently. V_{th} value was extracted with the maximum transconductance method in the linear region [7]. The first transistor ($W = 3\ \mu$m, $L = 30$ nm) shows a limited shift of V_{th} towards lower values ($\Delta V_{th} = -20$ mV at 1 Grad) as a function of TID. The second ($W = 100$ nm, $L = 1\ \mu$m), on the contrary, has a more complex evolution. The decrease of V_{th} is more pronounced and reaches $\Delta V_{th} = -70$ mV at 130 Mrad and then increases again with increasing accumulated dose ($\Delta V_{th} = -25$ mV at 1 Grad). Figure 2 (b) shows the V_{th} evolution with respect to TID for the whole set of transistors. It can be noted that, with the exception of the narrowest transistors, the V_{th} decrease is limited to <30mV (and it is basically within the device-to-device variability); for transistors with a small W, the decrease in V_{th} is more marked.

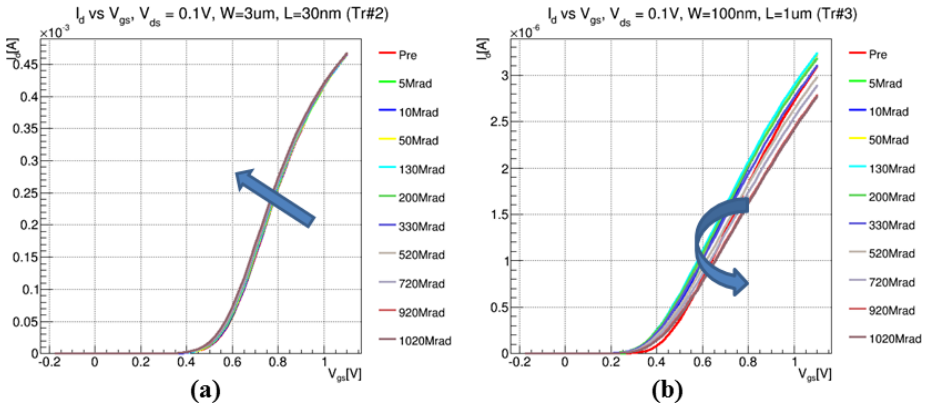

Figure 1. $I_d - V_{gs}$ characteristics in linear regime for two transistors: (a) $W = 3\ \mu$m, $L = 30$ nm, (b) $W = 100$ nm, $L = 1\ \mu$m.

A behavior similar to the one shown by the long and wide transistor ($W = 100$ nm, $L = 1\ \mu$m) has been observed both in 130 nm and 65 nm technology nodes [5, 6]. For the other technologies the effect was essentially always present but strongly dependent on the transistor width (more pronounced for narrow devices, only marginal on wide ones). For the technology under study on this paper the "rebound" has been shown only for one transistor. This so-called "rebound" effect originates from the compensation between positive charge trapped in the bulk of Shallow Trench Isolation (STI) oxides and the negative (for nMOSFETs) charge accumulated in the interface states.

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Radiation-induced positive charges are quickly trapped in the STI oxides at the transistor edge, causing a decrease of V_{th}. The negative charge trapped in the interface states starts to compete with positive gate oxide charge only with some delay, compensating the electrical field.

Linear-layout nMOSFETs are affected by positive charge trapped in STI oxides, which opens a lateral conductive path where current can flow between source and drain. This current, flowing in the lateral parasitic transistor, appears as an increase of the leakage current in the main transistor. In figure 2 (a) the evolution of the leakage current is shown, as a function of TID, for all the transistors tested; leakage current increases of 2–3 orders of magnitude for all the transistors, regardless of the geometry. Saturation current (not shown here) does not display any appreciable degradation, so that the $I_{\text{on}}/I_{\text{off}}$ ratio is always greater than 10^4. Therefore the degradation of leakage current should not affect the overall device functionality, even though it would cause a large increase of power consumption in very complex circuits.

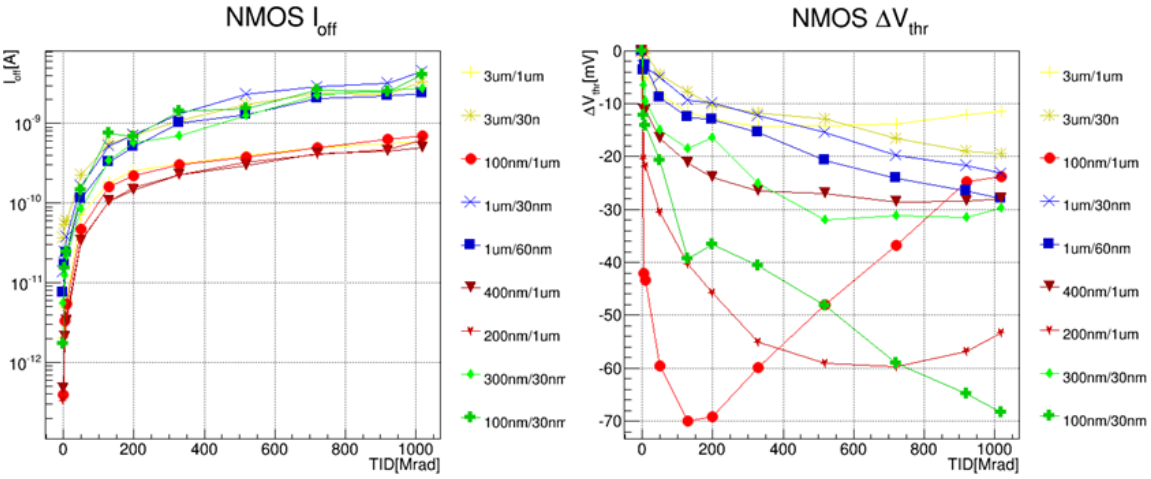

Figure 2. (a) I_{leak} progression as a function of TID. (b) ΔV_{th} evolution with TID.

4 pMOSFET irradiations

For pMOSFETs there is no degradation in the off-state leakage current, since they are not subject to sidewall leakage current. The subthreshold slope evolution with TID has been calculated, since it is related to the accumulation of interface traps [8]. The degradation is not noticeable ($\Delta ss < 10$ mV/dec for all the transistors), which might be an indication of a negligible accumulation of interface traps in the oxide. In order to perform a more in-depth analysis of the interface, the charge pumping technique, a more reliable and precise method [9], might also be applied; however this study would require some ad-hoc test structures and could not be performed on the available devices.

Figure 3 (a) shows the $I_d - V_{\text{gs}}$ curve for the transistor with the minimum gate width and maximum gate length ($W = 100$ nm, $L = 1\ \mu$m). The threshold voltage increases as expected (in absolute value). For pMOSFET, in fact, both the charge trapped in the bulk of STI oxides and the charge trapped at the interface are positive and the two effects sum up. In figure 3 (b) the $I_d - V_{\text{ds}}$ curves in saturation region ($V_{\text{gs}} = 1.1$ V) are shown. The degradation of the saturation current (I_{on}),

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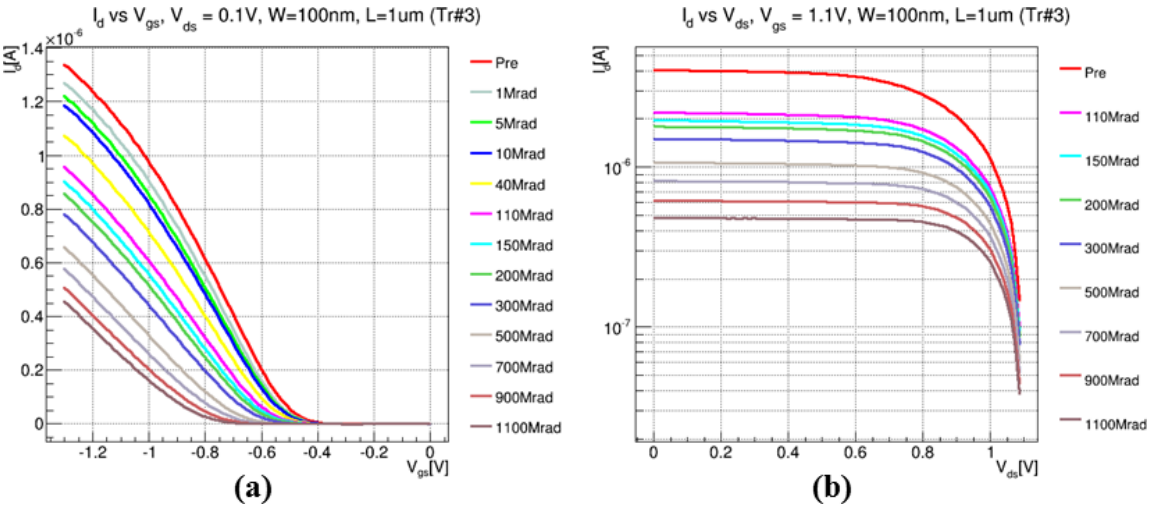

Figure 3. (a) $I_d - V_{gs}$ curves in the linear region ($V_{ds} = 0.1$ V). (b) $I_d - V_{ds}$ curves in the saturation region ($V_{gs} = 1.1$ V).

i.e. the drain current for $V_{gs} = V_{ds} = 1.1$ V, is dramatic. At 200 Mrad the current is already halved, and at 1Grad it drops to one order of magnitude below the initial value.

Figure 4 (a) plots the variation of the saturation current with the dose (expressed in percent variation with respect to the value before irradiation), for the complete set of devices tested. From the picture it is clear that I_{on} decreases for all the devices, but the degradation is limited for some of them, while it is more severe for others. In order to better understand the dependence on the transistor geometry, in figure 4 (b) the behavior of four transistors sharing a moderate channel length ($L = 1$ μm, the maximum available, so reasonably no short channel effects should be present), but with W ranging from 3 μm down to 100 nm, is shown. The strong impact of the channel width is clear: for $W = 3$ μm the drain current loss is limited to 20% at the maximum dose, while for the minimum width device at the same dose there is a loss of about 90%.

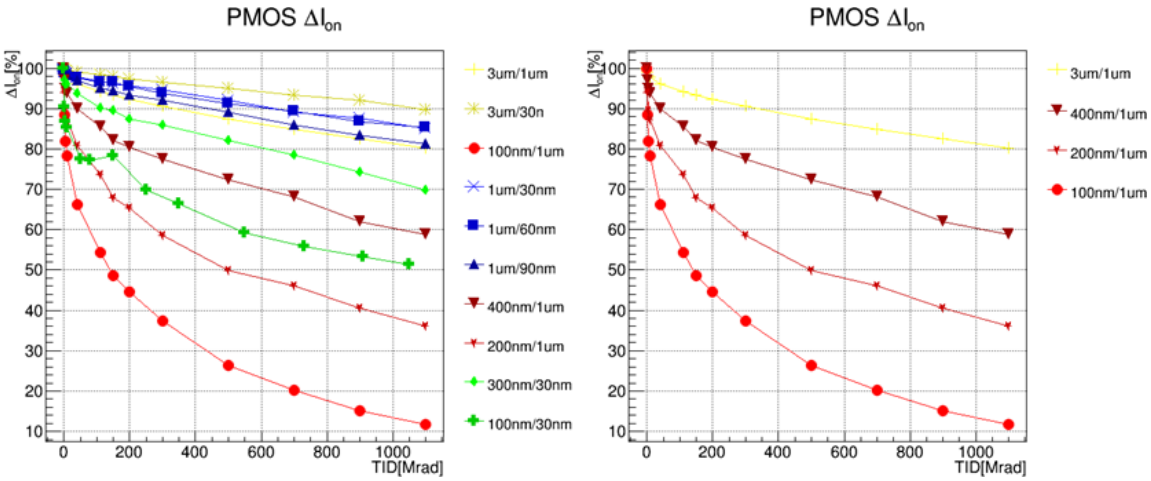

Figure 4. (a) Variation in the saturation current (I_{on}) for the whole set of structures. (b) Trend for I_{on} for an array of transistors with the same L (1 μm) but different W (100 nm, 200 nm, 400 nm, 3 μm).

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The degradation of the maximum drive current for narrow transistors is attributed to Radiation Induced Narrow Channel Effect (RINCE) [5, 6]. For these devices the radiation-induced positive charge trapped in the lateral STI influences the main transistor; it prevents the channel inversion, with the consequence of reducing the available channel width.

Interestingly there seems to be no (or very small) effect related to the channel length. In figure 5 the I_{on} variation loss is shown for two subsets of transistors with the same channel width and different length ($W = 1\ \mu$m, $L = 30$ nm, 60 nm, 90 nm in (a) and $W = 3\ \mu$m, $L = 1\ \mu$m and 30 nm in (b)). In all cases the current loss is below 20% at 1 Grad. This is different from what has been measured for other technology nodes (like 65 nm [3]) and might have a strong impact on the design of digital circuits, where designers might have more flexibility in the choice of the device geometry (especially minimum L transistors).

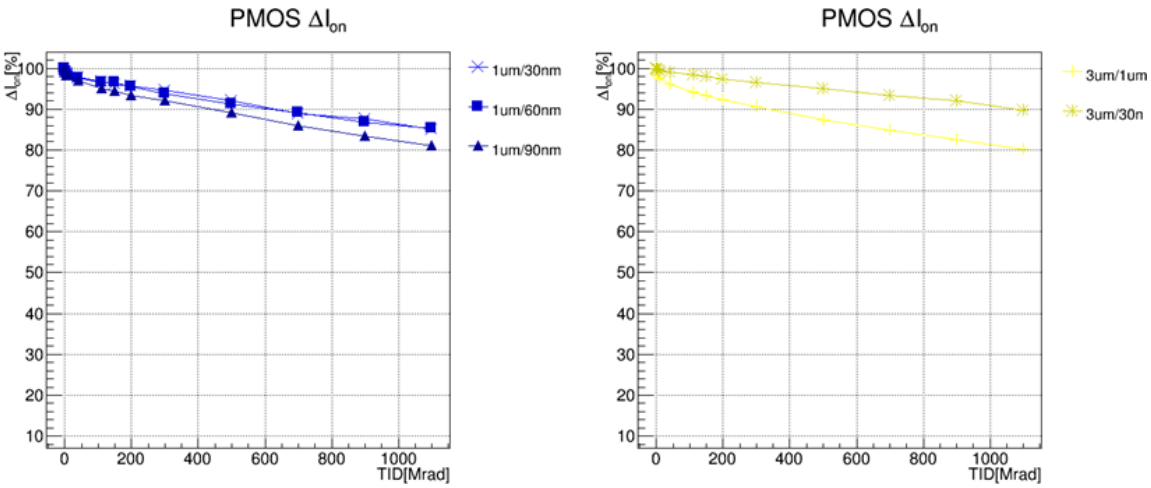

Figure 5. I_{on} for two subsets of transistors with the same W ($W = 1\ \mu$m in (a), $W = 3\ \mu$m in (b)) but different L.

The loss in the drain current can only partially be explained by a decrease of mobility. In figure 6 (a) the variation of g_m with respect to the initial value is shown; even in the worst case (minimum W device), the degradation of transconductance is of 50%; another contribution comes from the shift in the threshold voltage (figure 6 (b)), which is limited to few tens of mV for wide devices, while it reaches hundreds of mV for narrower transistors.

It is also worth noticing that for pMOSFETs, in the g_m curves, not only the g_m peak decreases with TID, but it also shifts in V_{gs} (this effect being more pronounced for narrow devices), as shown in figure 7. The figure also shows how the parameter extraction becomes very difficult for the narrowest transistor at the highest doses, since the curves are very degraded.

5 Conclusions

A 28 nm high-k commercial CMOS technology has been tested for Total Ionizing Dose damage at 1Grad with X-ray irradiation, for possible applications at future HEP experiments. Both nMOSFETs and pMOSFETs have been tested. For nMOSFETs, parameter degradation is limited except for drain to source leakage current, which increases by a few orders of magnitude, but without compromising the device functionality. pMOSFETs show a more severe degradation of parameters, especially in

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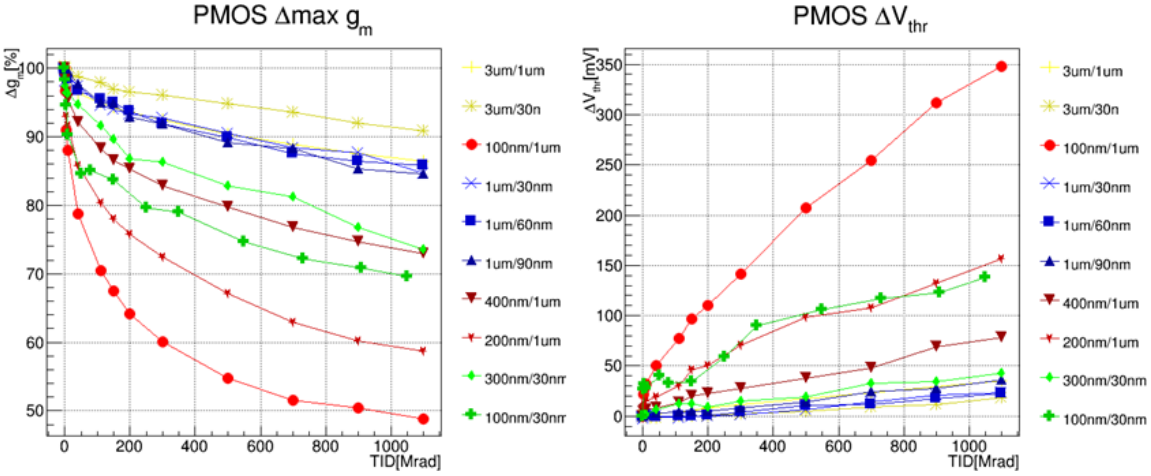

Figure 6. (a) Variation of the peak of transconductance with TID. (b) Variation of V_{th} with TID.

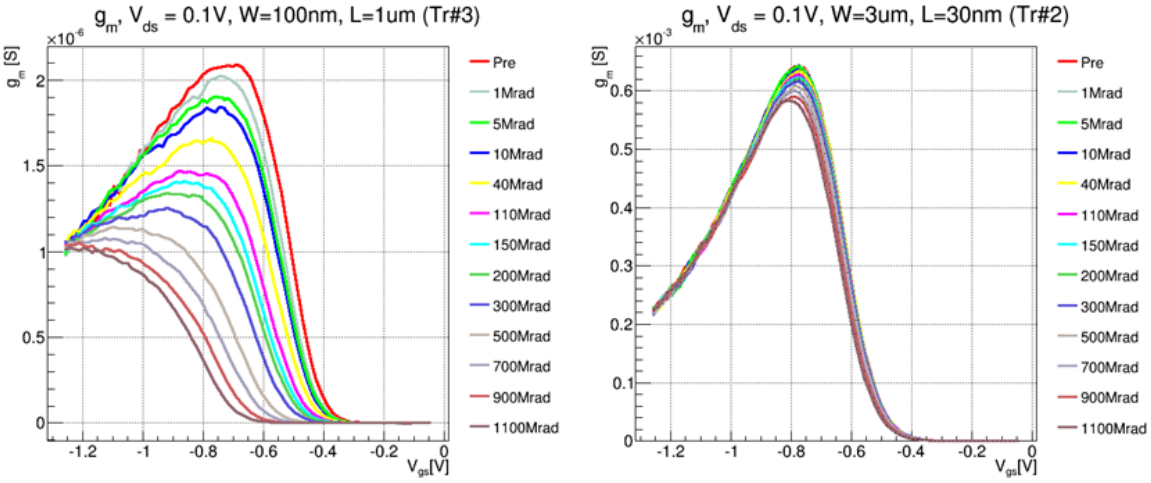

Figure 7. Transconductance for two transistors: (a) $W = 3\,\mu$m, $L = 30\,$nm, (b) $W = 100\,$nm, $L = 1\,\mu$m.

the saturation drain current, which has a strong dependence on the width of the transistor and is worst for devices featuring narrow channels.

Some design techniques, such as the implementation of wide transistors, might be adopted to reduce the impact of the irradiation damage, without limiting the circuit performance. HEP designers may be able to use it and profit from the intrinsic low-power advantages which accompany this technology.

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