University of Bergamo

SCHOOL OF DOCTORAL STUDIES
Doctoral Degree in Engineering and Applied Science
XXXIII Cycle - SSD: ING-INF/01 - Elettronica

Design and characterization of a 32 channels mixed-signal processor for the Si(Li) tracker of the GAPS experiment

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Academic year 2019–2020

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Introduction

One of the towering problems of early 21th century physics is the identification and discovery of the nature of dark matter which, according to different studies, is expected to account for about the 86% of the universe mass. The dark matter is an hypothetical component of matter not directly observable, because, with respect to the known matter, it does not emit electromagnetic radiation and it manifests itself only by gravitational effects. The existence of non-relativistic particles, which weakly interact with the known matter by gravitational force and weak nuclear force, has been hypothesized: they are called WIMPs (Weakly Interacting Massive Particles).

In this scope, the GAPS (General AntiParticle Spectometer) experiment arises as a modern approach to the indirect search of the dark matter, leading to a complementary type of research. In fact, GAPS aim is not to directly detect the WIMPs, but, instead, the anti-deuteron that is produced by the WIMPs auto-annihilations. Cosmic rays rarely produce anti-deuteron particles with energies below 0.25 GeV whereas the dark matter models predict a higher number of anti-deuterons produced even at these low energies. In the physics experiments, the anti-deuteron was never revealed, so its non-ambiguous detection will be very significant. In physics theories, anti-deuteron would be produced in high concentration zones of dark matter with a high rate of annihilations. The anti-particles produced by the dark matter are captured by a target material with the consequent formation of an exotic excited atom. This exotic atom quickly decays, producing X-rays at uniquely defined energies and after the subsequent nuclear annihilation, other particles as pions and protons. The GAPS detection method consists of a Time-Of-Flight (TOF) system, for a first selection of the particles of interest, and a solid state tracker based on Lithium-Drifted Silicon (Si(Li)) detectors, which reconstruct the particle traces and velocities. From this data it is possible to obtain information about the particle energy and its type. The research project discussed in this thesis work is focused on the design of the front-end electronics for the GAPS Si(Li) tracker.

The thesis work is organized as follows. In the Chapter 1 the design of three IP blocks for the detector readout channel is described. The first designed IP block is a bandgap voltage reference. This block's main task is to generate a PVT (P: manufacturing process variations, V: supply voltage, T: temperature) independent, stable voltage which will be used in other channel blocks. In particular, the generated voltage is used by the second IP block: a current generator. This generates a fixed current of 5 μA, made process independent by the design of a specific 3-bit DAC, included in the current generator design. The currents are then mirrored in other branches of the channel with a gain factor dependent on the required current. The last designed IP block is an 8-bit DAC used to generate two threshold voltages needed by a channel comparator.

The Chapter 2 is focused on the characterization of the two first designed ASIC prototypes: SiLI DEtector Readout 4 (SLIDER4) and SiLI DEtector Readout 8 (SLIDER8). SLIDER4 is a 4-channels simplified version of the final ASIC which has been used to validate the functionality of all the main blocks included in the readout channel. SLIDER8 is a simplified

version of the final ASIC, too. Beside 8 analog readout channels it also includes an 11-bit SAR ADC and a digital back-end section.

In Chapter 3 the results obtained from the characterization of the first prototype of the flight ASIC, pSLIDER32, are described. The ASIC has been tested as a standalone device and also once mounted on the front-end board designed for the final experiment. Moreover, since the assembly of the tracker requires the connection of 6 front-end boards in a chain, 6 front-end boards (with the mounted ASIC) connected with each other have been tested. Measurement results of this chain executed with pSLIDER32 ASICs are reported in this chapter, too.

1 Design of IP blocks in a 180 nm CMOS technology

All ASICs need IP blocks to work properly. In particular three IP blocks, needed by the GAPS ASIC, will be described in this chapter: a bandgap voltage reference, which generates a PVT (P: manufacturing process variations, V: supply voltage, T: temperature) independent, stable voltage, a current generator (and a 3-bit DAC for its fine trimming) used to bias all the blocks of the analog readout channel of the GAPS ASIC by means of current mirrors, and a 8-bit DAC used to generate two threshold voltages needed by the readout channel comparator.

1.1 Voltage and current reference

The analog front-end channel designed for the readout of the Si(Li) detector of the GAPS experiment (appendix A) is comprised of several blocks, as discussed in detail in appendix B. Each element of the channel requires one or more current references to be properly biased. These references should remain constant regardless of the external conditions like temperature, variations in the ASIC supply voltage and process parameter mismatch in fabrication. To comply with this requirement, a solution where the reference currents are generated starting from a precise voltage reference has been adopted, as shown in fig. 1.1. Starting from this voltage (Voltage Reference: BGR), a 3-bit adjustable current can be obtained and then the final reference currents can be derived. Each of these blocks will be discussed in detail in this section.

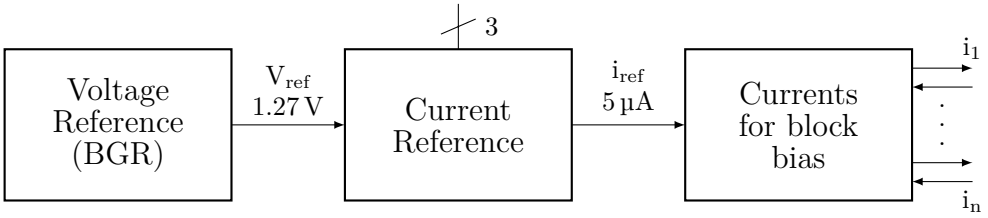


Figure 1.1: block diagram of GAPS voltage and current references.

1.1.1 Bandgap Voltage Reference

A voltage reference is an essential block in the design of any integrated circuit. The goal of a bandgap voltage reference is to generate a PVT independent stable voltage. In order to achieve this goal, the following basic principle is usually adopted, i.e. the reference voltage is obtained as the sum of two voltages [1]:

- V_1 with positive temperature coefficient (TC), $\frac{\partial V_1}{\partial T} = k_1$, where $k_1 > 0$;

- V_2 with negative temperature coefficient (NC), $\frac{\partial V_2}{\partial T} = k_2$, where $k_2 < 0$.

Moreover, the derivative of the sum of these two voltages, with respect to the temperature, must be equal to 0:

$$\frac{\partial V_{out}}{\partial T} = \frac{\partial V_1}{\partial T} + \frac{\partial V_2}{\partial T} = k_1 + k_2 = 0. \tag{1.1}$$

The schematic of the bandgap designed for the the GAPS current generator, is one of the most widely used in commercial applications and is depicted in fig. 1.2 [2]. Because of the negative feedback network of the operational amplifier, the voltage at its non-inverting input, V^-, is equal to the voltage at its inverting input, V^+. PMOS M12, M13 and M14 are in current mirror configuration. The current which flows in the drain terminal of a PMOS operating in saturation mode can be defined as [3]:

$$I_D = \frac{1}{2}\mu_p C_{ox} \cdot \left(\frac{W}{L}\right) \cdot \left(V_{SG} - \left|V_{tp}\right|\right)^2 \cdot (1 + |\lambda| V_{SD}) \tag{1.2}$$

where λ is a device parameter whose units are reciprocal volts $\left[\mathrm{V}^{-1}\right]$, C_{ox} is the gate oxide capacitance per unit area $\left[\mathrm{F/m}^2\right]$, μ_p is the charge-carrier effective mobility while W and L are respectively the width and length of the MOS channel. PMOS M12 and M13 have the same dimensions, so $V_{tp,M12} = V_{tp,M13}$, $W_{M12} = W_{M13}$, $L_{M12} = L_{M13}$ and $\lambda_{M12} = \lambda_{M13}$. Moreover, by design, they have the same V_{SG}. Resistors $R_0 = R_1$ are inserted to guarantee $V_{SD,M12} = V_{SD,M13}$, suppressing current mismatch due to channel-length modulation. PMOS M14 is used to provide the bias current to the operational amplifier described in detail in section 1.1.2. After all these considerations, the two currents I_1 and I_2 can be considered as equal ($I_1 = I_2$). The constant voltage V_{ref} can be extracted from the following equivalence:

$$\frac{V_{ref} - V^-}{R_1} = \frac{V^+ - V_{E2}}{R_2}, \tag{1.3}$$

where $V^- = V^+ = V_{EB1}$ and $V_{E2} = V_{EB2}$. So:

$$V_{ref} = V_{EB1} + \frac{R_1}{R_2} \cdot (V_{EB1} - V_{EB2}) = V_{EB1} + \frac{R_1}{R_2} \cdot \Delta V_{EB}. \tag{1.4}$$

By differentiating V_{ref} with respect to the absolute temperature we obtain two terms: one proportional to the absolute temperature (PTAT) the other proportional to the complementary absolute temperature (CTAT), as shown in the following equation:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{EB1}}{\partial T} + \frac{\partial \Delta V_{EB}}{\partial T} \cdot \frac{R_1}{R_2}. \tag{1.5}$$

Negative TC voltage

The pnp BJT consists of three semiconductor regions: the emitter region E (p-type), the base region B (n-type) and the collector region C (p-type). These regions form two pn junctions, the emitter-base junction (EBJ) and the collector-base junction (CBJ). In this project, the pnp has been used as a diode-connected transistor, namely $V_E > V_B$ (forward biased EBJ junction) and $V_B = V_C$ (reverse biased CBJ junction). A characteristic of diode-connected

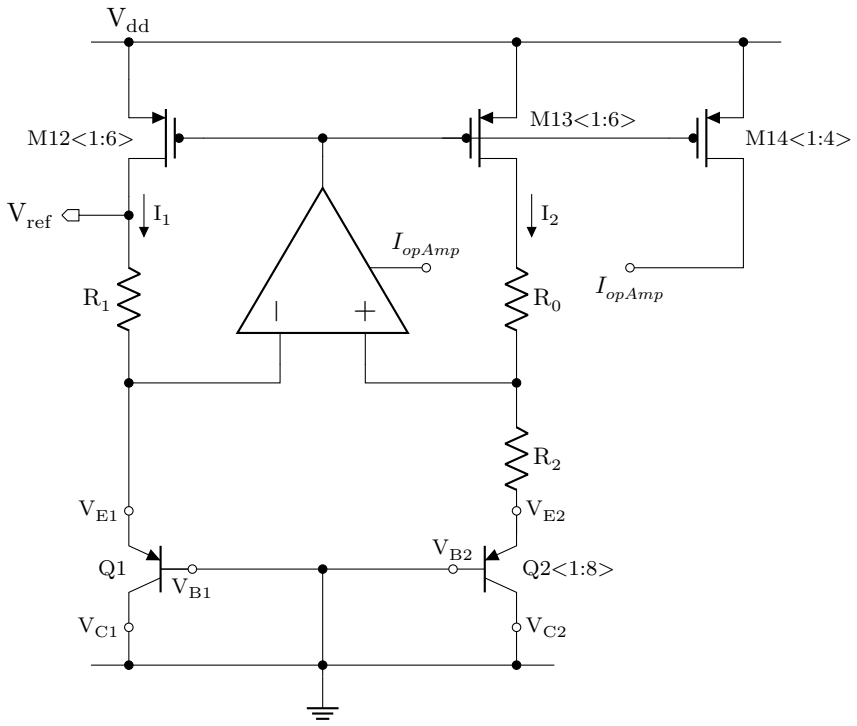


Figure 1.2: bandgap voltage reference schematic.

BJTs is that they are always in the forward active region. The emitter current of a pnp in diode-connected configuration can be defined using the Shockley diode equation [3]:

$$I_E = I_S \left[\exp\left(\frac{V_{EB}}{V_T} \right) - 1 \right], \tag{1.6}$$

where $V_T = (k_B \cdot T)/q$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge and I_S is the saturation current (which is an intrinsic transistor parameter). Even for small V_{EB}, the exponential is very large, since the thermal voltage is very small in comparison (at 300 K, $V_T = 25.85\,\mathrm{mV}$), so that the diode equation can be approximated by [3]:

$$I_E \approx I_S \cdot \exp\left(\frac{V_{EB}}{V_\mathrm{T}} \right). \tag{1.7}$$

The saturation current of a BJT, can be defined as [3]:

$$I_S = \frac{A_\varepsilon q D_p p_{n0}}{W} \tag{1.8}$$

where p_{n0} is the thermal-equilibrium value of the minority-carrier (hole) concentration in the base region, A_ε is the cross-sectional area of the base-emitter junction, D_p is the hole diffusion coefficient in the base, W is the effective width of the base. By expressing $p_{n0} = p_i^2/N_A$, where p_i is the intrinsic carrier density and N_A is the doping concentration in the base, I_S can be expressed as [3]:

$$I_S = \frac{A_\varepsilon q D_p p_i^2}{N_A W} \tag{1.9}$$

Typically I_S is in the range from 10^{-12} A to 10^{-18} A and is a strong function of temperature, approximately doubling every 5 °C rise in temperature. In fact:

- $p_i = BT^{3/2} \exp\left(-E_g/2k_BT\right)$. B is a material-dependent parameter that is $7.3 \cdot 10^{15}\ \mathrm{cm^{-3}K^{-3/2}}$ for silicon [3].
- E_g is the bandgap energy of silicon. The relationship between band gap energy and temperature can be described by Varshni's empirical expression [4]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}. \tag{1.10}$$

  In silicon: $\alpha = 4.73 \cdot 10^{-4}$ eV/K, $\beta = 636$ K and $E_g(0) = 1.17$ eV [5]. In the range of temperature of interest (from −40 °C up to 30 °C) the bandgap energy of silicon can be considered constant, and its value is 1.14 eV. So, from here on, $E_g = 1.14$ eV will be considered.

- $D_p = \mu_p V_T$. This is the electrical mobility equation coming from the Einstein – Smoluchowski diffusion relation, where μ_p is the hole mobility in silicon.
- Regarding the temperature dependence of μ_p in silicon, the function $\mu_p(T)$ is often approximated as

$$\mu_p(T) = \mu_{p0} \left(\frac{T}{300\,\mathrm{K}}\right)^m. \tag{1.11}$$

  where $\mu_{p0} = 470.5\ \mathrm{cm^2/(V \cdot s)}$ (it is the maximum mobility, with no doping) and $m = -2.2$ [6, 7].

From these equations, it can be found that I_S is proportional to $\mu_p k_B T p_i^2$ [1]. Thus,

$$I_S = b \cdot T^{4+m} \cdot \exp\left(\frac{-E_g}{kT}\right) \tag{1.12}$$

where b is a proportionality factor, which contains all the temperature independent terms. Writing $V_{EB} = V_T \cdot \ln(I_E/I_s)$, the TC of the base-emitter voltage can be computed. Given the derivative of V_{EB} with respect to T, the behavior of I_E as a function of the temperature is known. To simplify the analysis, the current I_E is held constant. Thus,

$$\frac{\partial V_{EB}}{\partial T} = \frac{\partial V_T}{\partial T} \cdot \ln\frac{I_E}{I_S} - \frac{V_T}{I_S} \cdot \frac{\partial I_S}{\partial T}. \tag{1.13}$$

From eq. (1.12):

$$\frac{\partial I_S}{\partial T} = b \cdot (4+m) \cdot T^{3+m} \cdot \exp\left(\frac{-E_g}{kT}\right) + b \cdot T^{4+m} \cdot \exp\left(\frac{-E_g}{kT}\right) \cdot \frac{E_g}{kT^2}. \tag{1.14}$$

Therefore,

$$\frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2} \cdot V_T. \tag{1.15}$$

By combining eq. (1.13) and eq. (1.15) [1]:

$$\frac{\partial V_{EB}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2} \cdot V_T \tag{1.16}$$

$$= \frac{V_{EB} - (4+m) \cdot V_T - E_g/q}{T} \tag{1.17}$$

The eq. (1.17) gives the temperature coefficient of the base-emitter voltage at a given temperature T, revealing dependence on the magnitude of V_{EB} itself. With $V_{EB} \approx 780\,\text{mV}$ and $T = 233\,\text{K}$, $\partial V_{EB}/\partial T = -1.7\,\text{mV/K}$. From the eq. (1.17), it can be noted that the temperature coefficient of V_{EB} itself depends on the temperature, creating a small error in constant reference generation.

From the simulations, the CTAT (Complementary to Absolute Temperature) voltage at 233 K is:

$$\frac{\partial V_{EB1}}{\partial T} \simeq -1.72\,\frac{\text{mV}}{\text{K}}, \tag{1.18}$$

which is a very similar value to the one obtained from theory.

Positive TC voltage

From eq. (1.7)

$$V_{EB} = V_T \cdot \ln\left(\frac{I_C}{I_S}\right). \tag{1.19}$$

Using eq. (1.19), ΔV_{EB} can be found as

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = \tag{1.20}$$

$$= V_T \cdot \ln\frac{I_{E1}}{I_{S1}} - V_T \cdot \ln\frac{I_{E2}}{I_{S2}} = \tag{1.21}$$

$$= V_T \cdot \ln\left(\frac{I_{E1} \cdot I_{S2}}{I_{E2} \cdot I_{S1}}\right). \tag{1.22}$$

Since all the BJT fingers of Q1 and Q2 have the same dimensions, the current saturation of these are equal ($I_{S1} = I_{S2}$). Moreover, their collector currents are:

- $I_{E1} = I_1$, because Q1 has only 1 finger.
- $I_{E2} = \frac{I_2}{N} = \frac{I_1}{8}$, since Q2 is composed of 8 fingers (N is the number of fingers).

From these assertions, the derivative of ΔV_{EB} can be easily found:

$$\Delta V_{EB} = V_T \cdot \ln(\text{N}) = V_T \cdot \ln(8), \tag{1.23}$$

$$\frac{\partial \Delta V_{EB}}{\partial T} = \frac{k}{q} \cdot \ln(8) \simeq 0.179\,\frac{\text{mV}}{\text{K}} \tag{1.24}$$

which is the required PTAT (Proportional to Absolute Temperature) coefficient.

Voltage reference

The numerical values found in the eq. (1.18) and (1.24) can be used in the eq. (1.5):

$$\frac{\partial V_{ref}}{\partial T} = -1.72\,\frac{\text{mV}}{\text{K}} + 0.179\,\frac{\text{mV}}{\text{K}} \cdot \frac{R_1}{R_2} = 0, \tag{1.25}$$

and hence

$$\frac{R_1}{R_2} = \frac{1.72}{0.179} = 9.6. \tag{1.26}$$

In Section 1.1.4 the solution adopted to select the resistors is carefully explained.

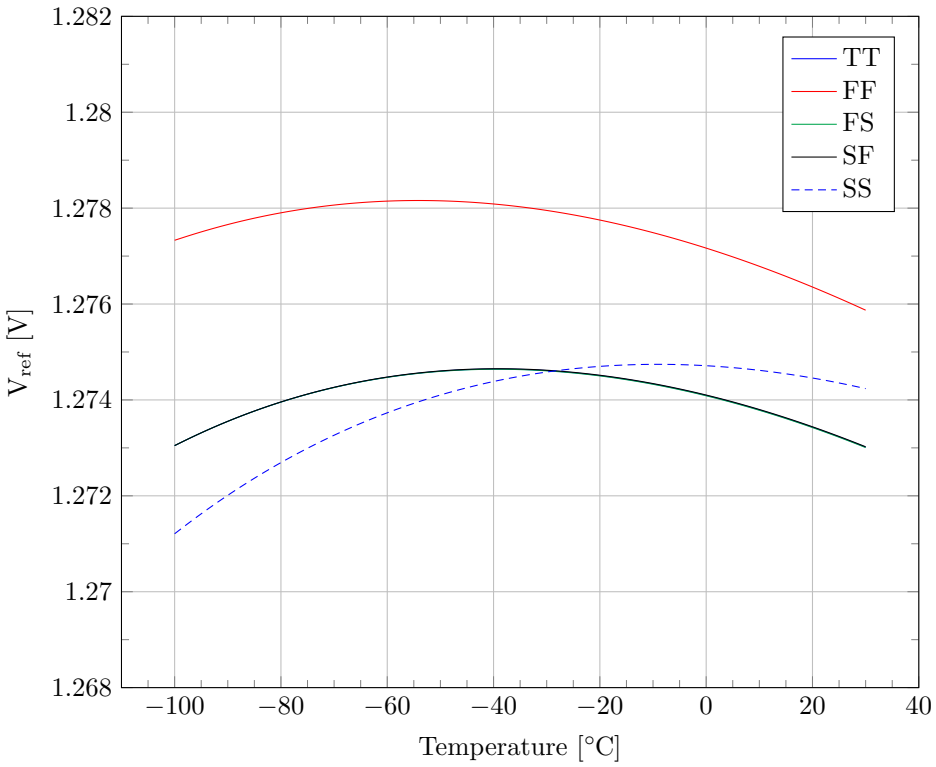


Figure 1.3: bandgap voltage reference V_{ref} corner values. Results for corners TT, FS, and SF cannot be distinguished since they are perfectly superimposed.

In figure fig. 1.3 the bandgap voltage reference as a function of temperature, provided by schematic simulations, is shown. Since the expected operating temperature is −40 °C, simulations have been done by varying the temperature in a range of ±60 °C with respect to −40 °C. In table 1.1 the results of a 1000 step Monte Carlo simulation are reported. The bandgap voltage is more affected by mismatch than process parameters, however, the standard deviation of the V_{ref} is still low (6.86 mV). In fact, the maximum variation of the output ΔV_{ref} is 40 mV. This value satisfies the requirements of the project.

	TEMP. [°C]	Min [V]	Max [V]	μ [V]	σ [mV]
Process	-40	1.269	1.282	1.275	2.04
	27	1.265	1.282	1.273	2.53
Mismatch	-40	1.256	1.296	1.275	6.85
	27	1.255	1.292	1.273	6.47

Table 1.1: Bandgap process and mismatch Monte Carlo simulations.

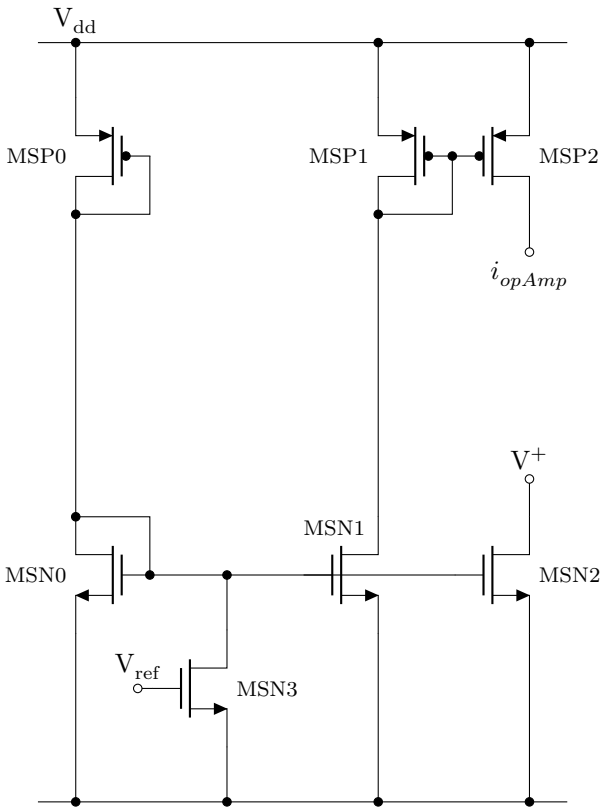


Figure 1.4: Start-up circuit for the Bandgap Voltage Reference.

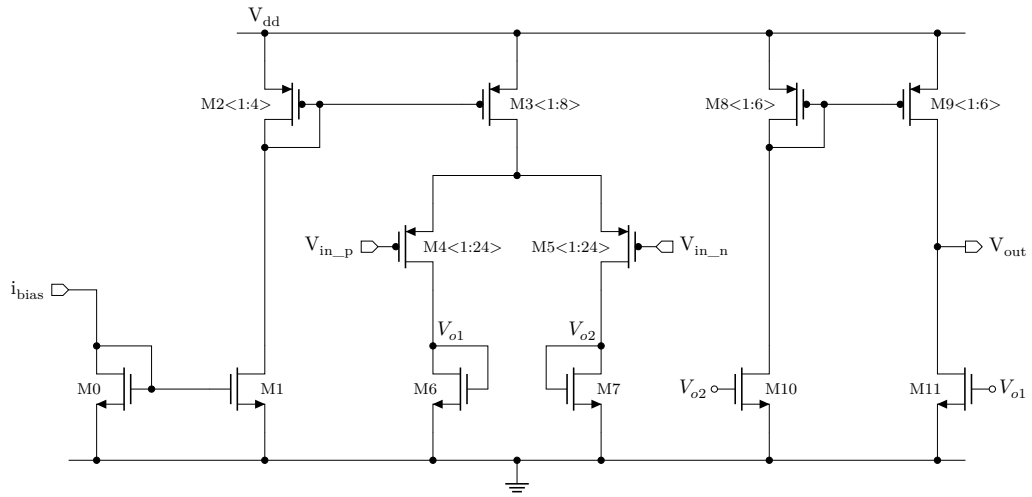


Figure 1.5: Operational amplifier schematic.

Start-up circuit

When the circuit is not powered, all transistors carry zero current because they are in the off-state. In some circuits, it may happen that, when the supply is turned on, they remain in the off-state due to the existence of degenerate bias points. In fact, if $I_1 = I_2 = 0\,\mathrm{A}$, $V_{ref} = V^- = 0\,\mathrm{V}$. Furthermore, if $V_{SG14} < \left|V_{tp14}\right|$ the operational amplifier is not correctly biased. This issue, known as "start-up" problem, is usually solved by adding a mechanism that drives the circuit out of the degenerate bias point when the supply is turned on [1]. The start-up circuit design for this bandgap is shown in fig. 1.4. This is a simple example, where the diode-connected device MSP0 provides a current which flows in the current mirror comprised of MSN0, MSN1 and MSN2 transistors. The MSN0 gate is connected to the gate of MSN1 and MSN2 mirroring the current in these branches. The drain of MSN2 is connected at node V^+ in the bandgap. The current starts to flow in the right branch of the bandgap (I_2), raising voltage V^+, and consequently V^- (due to the negative feedback loop configuration of the operational amplifier). Therefore, the current starts to flow in the left branch, too (I_1), raising the voltage V_{ref}. This is possible only if the operational amplifier is correctly biased. To solve this problem, the current mirror in the start-up circuit composed of transistor MSP1 and MSP2 provides the current needed by the operational amplifier to work correctly. When V_{ref} is high enough, MSN3 turns on, connecting the gates of MSN0, MSN1 and MSN2 to ground and turning off these transistors, and consequently, the entire start-up circuit. The problem of start-up, is that it generally requires careful analysis and simulation. The supply voltage must be ramped from zero in a dc sweep simulation (so that parasitic capacitances do not cause false start-up) as well as in a transient simulation and the behavior of the circuit examined for each supply voltage.

1.1.2 Operational Amplifier

The schematic of the operational amplifier used in the bandgap described in the previous subsection is shown in fig. 1.5. The bias current is provided from pin I_{bias}, and is mirrored in the first stage of the amplifier through M0, M1, M2 and M3 transistors.

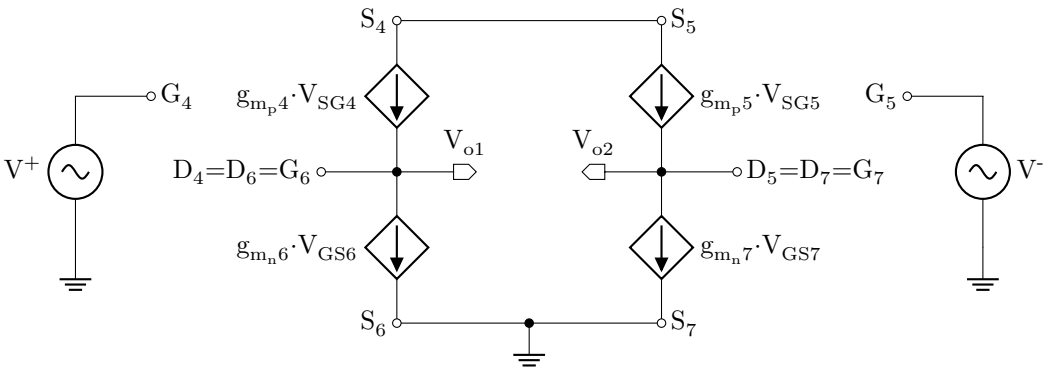


Figure 1.6: Small signal model of the first stage of the operational amplifier.

Small signal Model

In the first stage (M3-M4-M5-M6-M7) of the operational amplifier, M3, for the small signal model, is a current generator (as it is operated in a current mirror configuration), so it is considered like an open circuit. M4 and M5 have the same dimension and the same bias current, the same goes for M6 and M7. So $g_{m_p4} = g_{m_p5} = g_{m_p1}$ and $g_{m_n6} = g_{m_n7} = g_{m_n}$. The equivalent small signal model of the first stage is shown in fig. 1.6. The Kirchoff current Law is applied to node S_4, obtaining:

$$g_{m_p1} \cdot V_{SG4} = -g_{m_p1} \cdot V_{SG5} \tag{1.27}$$

$$\left(V_{S4} - V^+\right) = -\left(V_{S4} - V^-\right) \tag{1.28}$$

$$V_{S4} = \frac{V^+ + V^-}{2}. \tag{1.29}$$

With the help of eq. (1.29), the current balance in V_{o1} is:

$$g_{m_p1} \cdot V_{SG4} = g_{m_n} \cdot V_{GS6} \tag{1.30}$$

$$g_{m_p1} \cdot \left(V_{S4} - V^+\right) = g_{m_n} \cdot V_{o1} \tag{1.31}$$

$$V_{o1} = \frac{g_{m_p1}}{g_{m_n}} \frac{V^- - V^+}{2}, \tag{1.32}$$

and similarly V_{o2}:

$$V_{o2} = \frac{g_{m_p1}}{g_{m_n}} \frac{V^+ - V^-}{2}. \tag{1.33}$$

Using equations (1.32) and (1.33) it is possible to find:

$$V_{o2} - V_{o1} = \frac{g_{m_p1}}{g_{m_n}} \left(V^+ - V^-\right). \tag{1.34}$$

The second stage of the operational amplifier is composed of MOS M8, M9, M10 and M11. M10 and M11 have the same dimensions and bias currents of MOS M6 and M7 of the first stage. So, $g_{m_n10} = g_{m_n11} = g_{m_n}$. M8 and M9 are equal, too, obtaining $g_{m_p8} = g_{m_p9} = g_{m_p2}$. r_{DS9} and r_{DS11} are in parallel configuration, so $r_{DS} = r_{DS9} /\!/ r_{DS11}$. Applying Kirchoff

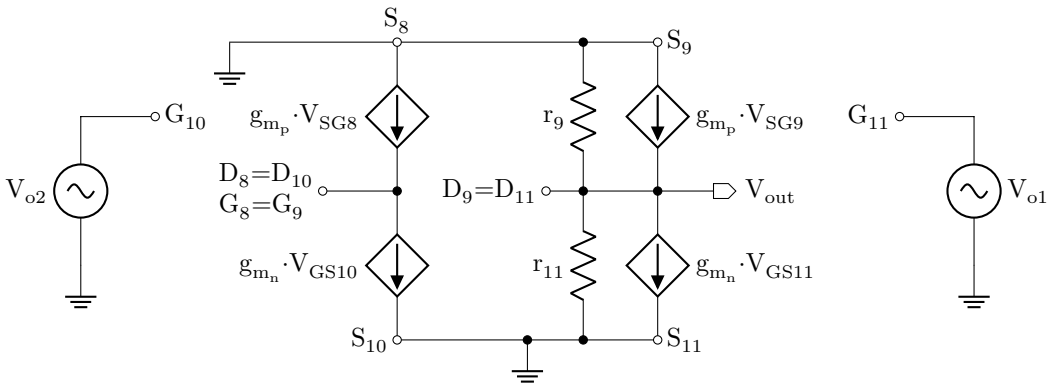


Figure 1.7: Small signal model of the second stage of the operational amplifier.

current law to node G_8:

$$g_{m_p2} \cdot V_{SG8} = g_{m_n} \cdot V_{GS10} \tag{1.35}$$

$$V_{g8} = -\frac{g_{m_n}}{g_{m_p2}} V_{o2}. \tag{1.36}$$

The current balance in V_{out}:

$$g_{m_p2} \cdot V_{SG9} + \frac{0 - V_{out}}{r_{DS}} = g_{m_n} \cdot V_{GS11} \tag{1.37}$$

$$V_{out} = -r_{DS} \cdot \left(g_{m_p2} V_{g8} + g_{m_n} V_{o1} \right). \tag{1.38}$$

With the help of eq. (1.36):

$$V_{out} = r_{DS} \cdot g_{m_n} \left(V_{o2} - V_{o1} \right), \tag{1.39}$$

and finally, using eq. (1.34)

$$V_{out} = r_{DS} \cdot g_{m_p1} \left(V^+ - V^- \right). \tag{1.40}$$

1.1.3 Current Reference

The 5 µA current reference, I_{ref}, is generated by means of the circuit shown in fig. 1.8. In order to obtain a constant current, the voltage reference V_{ref} must be independent of temperature, process parameters and supply voltage variations. The Bandgap Voltage Reference, described in section 1.1.1 has been designed to accomplish this task. With a fixed V_{ref}, it is possible to select R_t in order to have:

$$I_{ref} = \frac{V_{ref}}{R_t} = 5\,\mu\text{A} \tag{1.41}$$

For R_t to be temperature independent, two different types of resistors have to be used:

- R_p, whose value is directly proportional to the temperature
- R_n, whose value is inversely proportional to the temperature.

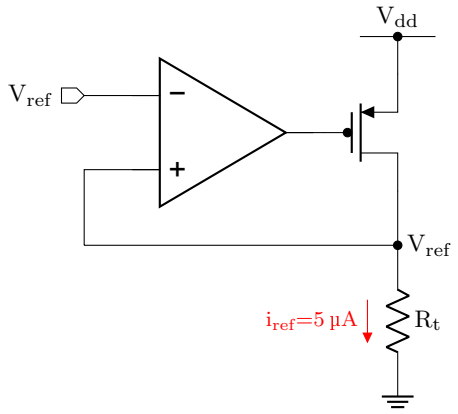


Figure 1.8: Semplified schematic of the current generator design for GAPS Front-end.

The sum of these two resistors must be constant as a function of temperature:

$$R_t = R_p(T) + R_n(T). \tag{1.42}$$

Two resistors, R_p and R_n, have been selected using the method explained in section 1.1.4 in order to obtain a fixed $I_{ref} = 5\,\mu A$. The complete schematic of the current generator is shown in fig. 1.9.

The current I_{ref} has to be mirrored in another branch of the circuit in order to be used to generate the other currents needed by the GAPS front-end. OP2, in buffer configuration, is used to mirror the voltage V_{ref} in the right branch of the circuit. Since the PMOS M12 and M13 have the same gate, drain and source voltages, the current I_{mir} is close to equal to the current I_{ref}. This has been verified by simulation, in temperature domain, and can be seen in fig. 1.10.

In order to guarantee the asymptotic stability and evaluate the robustness of the system, of the two negative feedback of OP1 and OP2, the phase margin has been extracted from simulations. The results are show in table 1.2.

	TEMP. [°C]	TT [°]	FF [°]	FS [°]	SF [°]	SS [°]
OP1	-40	67.77	65	72.81	63.02	72.22
	27	62.38	62.26	66.09	59.16	64.78
OP2	-40	55.84	54.46	57.08	55.13	58.01
	27	59.41	57.4	61.71	57.9	62.63

Table 1.2: phase margin of OP1 and OP2 feedback loop.

Afterwards, the current I_{mir} has been evaluated by varying: temperature, supply voltage and process parameters. Moreover a 1000 step mismatch and process simulation have been done. The results are shown in tables (1.3) and (1.4). The most critical cases are the FF and SS corners and the process Monte Carlo simulations.

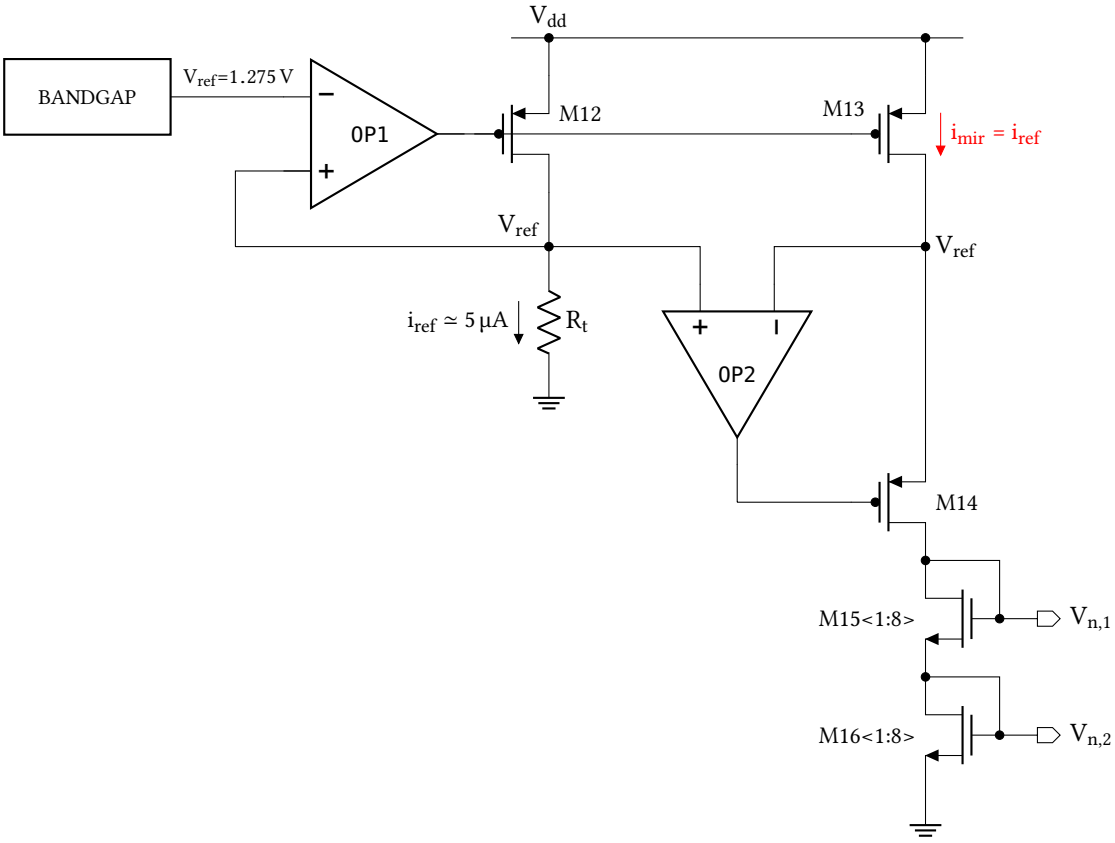


Figure 1.9: Current generator schematic.

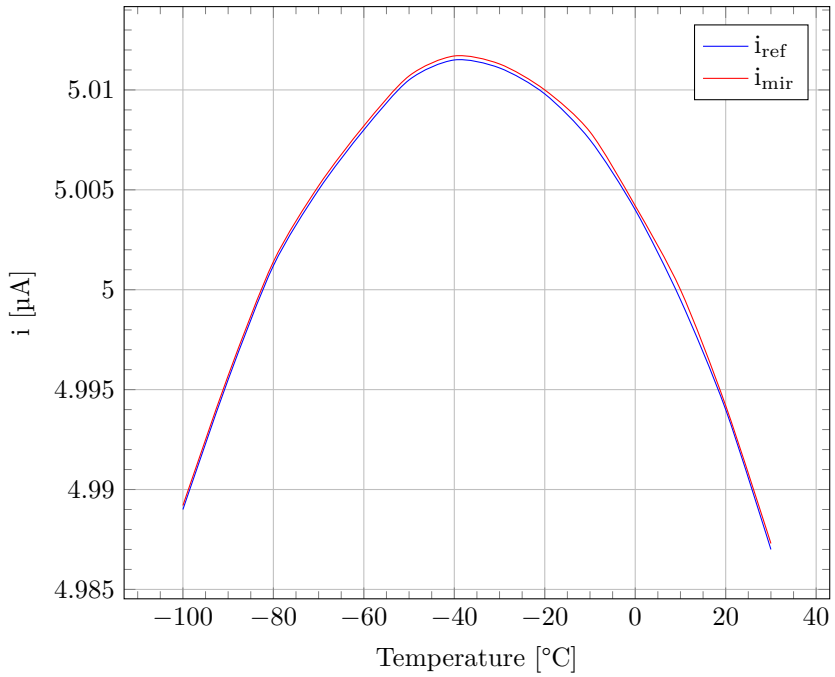


Figure 1.10: values of current I_{mir} with respect to I_{ref}.

V_{dd} [V]	TEMP. [°C]	TT [µA]	FF [µA]	FS [µA]	SF [µA]	SS [µA]
1.62	-100	4.985	5.725	4.980	4.987	4.415
	-40	5.006	5.753	5.005	5.007	4.436
	0	5.000	5.748	4.995	4.998	4.429
	27	4.980	5.734	4.980	4.982	4.41
1.8	-100	4.989	5.729	4.989	4.989	4.422
	-40	5.012	5.761	5.012	5.012	4.447
	0	5.004	5.757	5.004	5.004	4.432
	27	4.99	5.744	4.989	4.989	4.420
1.98	-100	4.990	5.731	4.990	4.990	4.423
	-40	5.012	5.762	5.012	5.013	4.441
	0	5.004	5.758	5.004	5.004	4.432
	27	4.990	5.745	4.990	4.990	4.418

Table 1.3: Values of current I_{mir} by varying: supply voltage, temperature and process parameters.

	TEMP. [°C]	Min [µA]	Max [µA]	μ [µA]	σ [nA]
Process	-100	4.340	5.697	4.990	210
	-40	4.346	5.737	5.013	215
	0	4.331	5.737	5.005	217
	27	4.312	5.726	4.991	218
Mismatch	-100	4.883	5.098	4.988	34
	-40	4.912	5.110	5.011	31
	0	4.907	5.096	5.004	30
	27	4.894	5.077	4.989	29

Table 1.4: Process and mismatch Monte Carlo simulations.

The current reference layout is shown in fig. 1.11. Its dimensions are 460 µm×125 µm.

1.1.4 Resistors choice

The resistance of an integrated resistor changes with the temperature, mainly due to the variation of charge carriers mobility in conductors, and concentration in semiconductors. In each CMOS technology, resistors can be made with different materials. In a material where the resistance increases with an increase in temperature, the material is said to have a positive temperature coefficient. When resistance decreases with an increase in temperature, the material is said to have a negative temperature coefficient. The resistance also depends on the applied voltage and the model adopted. In the 180 nm CMOS technology,

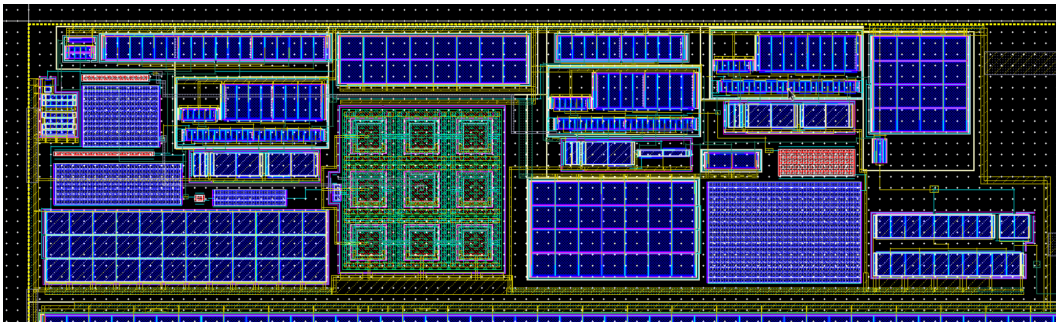


Figure 1.11: current reference layout.

the resistance model used for the GAPS project is the following [8]:

$$R(T,V) = R_0 \cdot \left(1 + T_{C1} \cdot \Delta T + T_{C2} \cdot \Delta T^2\right) \cdot \left(1 + V_{C1} \cdot \Delta V + V_{C2} \cdot \Delta V^2\right), \tag{1.43}$$

where $\Delta T = T - T_0$ (expressed in K), ΔV is the voltage drop across the resistor, T_{C1} [K^{-1}] and T_{C2}[K^{-2}] are temperature coefficients of the resistor while V_{C1}[V^{-1}] and V_{C2}[V^{-2}] are voltage coefficients of the resistor. R_0 is the resistance value at $T_0 = 25$ °C and 0 V applied, which is related to sheet resistance, R_{sh}, by the following equation [9]:

$$R_0 = R_{sh} \cdot \frac{L}{W}, \tag{1.44}$$

where W and L are the layout drawn width and length. If ΔV is constant, like in the circuit shown in fig. 1.8, eq. (1.43) can be rewritten as:

$$R(T) = k_R \cdot \frac{L}{W} \cdot \left(1 + T_{C1} \cdot \Delta T + T_{C2} \cdot \Delta T^2\right). \tag{1.45}$$

where $k_R = R_{sh} \cdot k_V$ and $k_V = \left(1 + V_{C1} \cdot \Delta V + V_{C2} \cdot \Delta V^2\right)$.

After selecting two resistance technologies, a and b, the resistance R_t (eq. (1.42)) can be rewritten as:

$$R_t(T) = R_p(T) + R_n(T) = \tag{1.46}$$

$$= k_p \cdot \frac{L_p}{W_p} \cdot \left(1 + T_{C1,p} \cdot \Delta T + T_{C2,p} \cdot \Delta T^2\right) + k_n \cdot \frac{L_n}{W_n} \cdot \left(1 + T_{C1,n} \cdot \Delta T + T_{C2,n} \cdot \Delta T^2\right) \tag{1.47}$$

where R_p is the a technology resistor and R_n is the b technology resistor.

At first, the values $x_p = \frac{L_p}{W_p}$ and $x_n = \frac{L_n}{W_n}$ that minimize $R_t(T) - R_p(T) - R_n(T)$, for some temperatures $[T_{min}, T_{min} + T_s, \ldots, T_{max} - T_s, T_{max}]$, have to be found ($T_s$ is the selected temperature step). This problem can be expressed in the form $\underline{y} = X \cdot \underline{\theta} + \underline{\epsilon}$, where $\underline{y} = \underline{R_t}$ and $\underline{\theta} = \left[x_p, x_n\right]$, namely:

$$\begin{bmatrix} R_t \\ \dots \\ R_t \end{bmatrix} = \begin{bmatrix} k_p \cdot \left(1 + T_{C1,p} \cdot \Delta T_{min} + T_{C2,p} \cdot \Delta T_{min}^2\right) & k_n \cdot \left(1 + T_{C1,n} \cdot \Delta T_{min} + T_{C2,n} \cdot \Delta T_{min}^2\right) \\ \dots & \dots \\ k_p \cdot \left(1 + T_{C1,p} \cdot \Delta T_{max} + T_{C2,p} \cdot \Delta T_{max}^2\right) & k_n \cdot \left(1 + T_{C1,n} \cdot \Delta T_{max} + T_{C2,n} \cdot \Delta T_{max}^2\right) \end{bmatrix} \begin{bmatrix} x_p \\ x_n \end{bmatrix} \tag{1.48}$$

Using the method of least squares

$$\underline{\hat{\theta}} = \left(X^T \cdot X\right)^{-1} \cdot X^T \cdot \underline{y}, \tag{1.49}$$

the error for each selected temperature T is

$$\underline{\varepsilon_T} = \underline{R_t} - \underline{X_{T,p}} \cdot x_p - \underline{X_{T,n}} \cdot x_n, \tag{1.50}$$

where:

$$\underline{X_{T,p}} = \begin{bmatrix} k_p \cdot \left(1 + T_{C1,p} \cdot \Delta T_{min} + T_{C2,p} \cdot \Delta T_{min}^2\right) \\ \cdots \\ k_p \cdot \left(1 + T_{C1,p} \cdot \Delta T_{max} + T_{C2,p} \cdot \Delta T_{max}^2\right) \end{bmatrix} \tag{1.51}$$

and

$$\underline{X_{T,n}} = \begin{bmatrix} k_n \cdot \left(1 + T_{C1,n} \cdot \Delta T_{min} + T_{C2,n} \cdot \Delta T_{min}^2\right) \\ \cdots \\ k_p \cdot \left(1 + T_{C1,n} \cdot \Delta T_{max} + T_{C2,n} \cdot \Delta T_{max}^2\right) \end{bmatrix}. \tag{1.52}$$

The Root-Mean-Square Error (RMSE), for the couple of resistance technologies (a, b), can be calculated:

$$RMSE_{a,b} = \sqrt{\frac{\sum_{n=T_{min}}^{T_{max}} \varepsilon_n^2}{\frac{T_{max} - T_{min}}{T_s}}}. \tag{1.53}$$

The main goal is to find two resistor technologies that minimize the RMSE. This task has been performed with two *for* cycles:

```
for(a=0,...,Ntec_pos)
        for(b=0,...,Ntec_neg)
                calculate and save: x_p(a,b),x_n(a,b) and RMSE(a,b)
        end
end
```

where Ntec_pos is the number of resistor technologies with positive temperature coefficient while Ntec_neg is the number of resistor technologies with negative temperature coefficient. Given all RMSE values, two technlogies (tec_1,tec_2) can be selected such that $RMSE_{tec_1,tec_2}$ is minimum and $x_{p,(tec_1,tec_2)} \geq 0, x_{n,(tec_1,tec_2)} \geq 0$.

Using this method, the two types of resistor chosen are: *N+ Diffusion resistor without silicide* (positive temperature coefficient) and *P+ Poly resistor without silicide* (negative temperature coefficient).

1.1.5 3-bit Digital to Analog Converter

As can be seen in tables 1.3 and 1.4, the mimimum and the maximum value of the current I_{mir} are respectively 4.31 µA (in process simulations at 27 °C) and 5.76 µA (in corners simulations, case FF at −40 °C with 1.98 V supply voltage). A DAC has been designed in order to compensate for this variation and obtain a current as close as possible to the required 5 µA. For dimension restrictions, design simplicity and correction effectiveness a 3-bit DAC, in binary weighted configuration, has been chosen [10]. Having 3 bits available, the DAC lsb (I_{LSB}) was initially obtained by calculating:

$$I_{LSB} = \frac{I_{max} - I_{min}}{2^3 - 1} \tag{1.54}$$

With an error margin Δi for both I_{min} and I_{max}, it can be obtained:

$$I_{LSB} = \frac{(I_{max} + \Delta i) - (I_{min} - \Delta i)}{2^3 - 1} = \frac{I_{max} - I_{min} + 2\Delta i}{2^3 - 1} \tag{1.55}$$

By placing $\Delta i = 0.3\,\mu A$:

$$I_{LSB} \approx \frac{2\,\mu A}{7} = 285.71\,nA \tag{1.56}$$

For layout design accuracy, current mirrors MOS must have the same L and multiple W with respect to the MOS of the main branch of the current mirror. For this reason, MOS with the same W and different number of fingers have been used. The LSB found in eq. (1.56) cannot be precisely obtained, by following the previous tips, due to the fact that MOS W cannot be modified at will. In order to contain the DAC dimensions, the I_{LSB} is found in this way:

- a first current mirror with a 1:4 ratio with respect to I_{mir} (generated by the current generator described in section 1.1.3) permits to obtain a 1.25 µA current (I_m);
- a second current mirror with a 1:4 ratio with respect to I_m permits to obtain a 312.5 nA current (I_{LSB}).

The 3 currents obtained with these 3 bit are:

- bit 0: 312.5 nA (ratio 1:4)
- bit 1: 625 nA (ratio 1:2)
- bit 2: 1.25 µA (ratio 1:1)

The schematic of the 3-bit DAC is shown in fig. 1.12. The final current I_{DAC} is calculated in this way:

$$I_{DAC} = b_0 \cdot \frac{1}{4} I_m + b_1 \cdot \frac{1}{2} I_m + b_2 \cdot I_m + I_f \tag{1.57}$$

The number of fingers of the rightmost branch has been chosen in a way that allows to have $I_{DAC} = 5\,\mu A$ with 011 bit combination. In fact:

$$I_{DAC,011} = \frac{1}{4} I_m + \frac{1}{2} I_m + \frac{13}{4} I_m = 4 I_m = 5\,\mu A \tag{1.58}$$

As described in section 1.1.3, the current generator is affected by process variations because of the resistor R_t. Its corner values may vary from $R_t - 15\,\%$ to $R_t + 15\,\%$. The 3-bit DAC just described can easily correct these cases. For example, if R_t value is 15 % greater than its nominal value, a 1.1 µA I_m and a 275 nA I_{LSB} are obtained. Following the eq. (1.57) and with a 101 DAC combination, the new current I_{DAC} can be calculated as:

$$I_{DAC,101} = \frac{1}{4} I_m + I_m + \frac{13}{4} I_m = \frac{9}{2} I_m = 4.95\,\mu A \tag{1.59}$$

The value just found is very close to the required 5 µA. The $R_t - 15\,\%$ case is similarly corrected with the 001 DAC combination.

The previous assumptions have been verified by simulations, as shown in table 1.5.

The entire current reference and 3-bit DAC layout is shown in fig. 1.13. Its dimensions are 460 µm×300 µm.

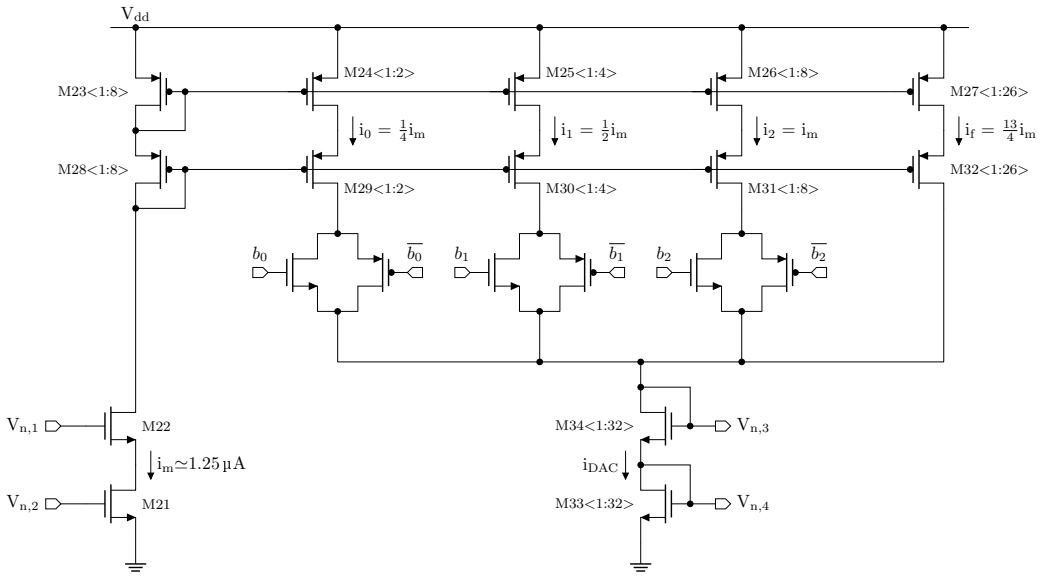


Figure 1.12: 3-bit DAC schematic.

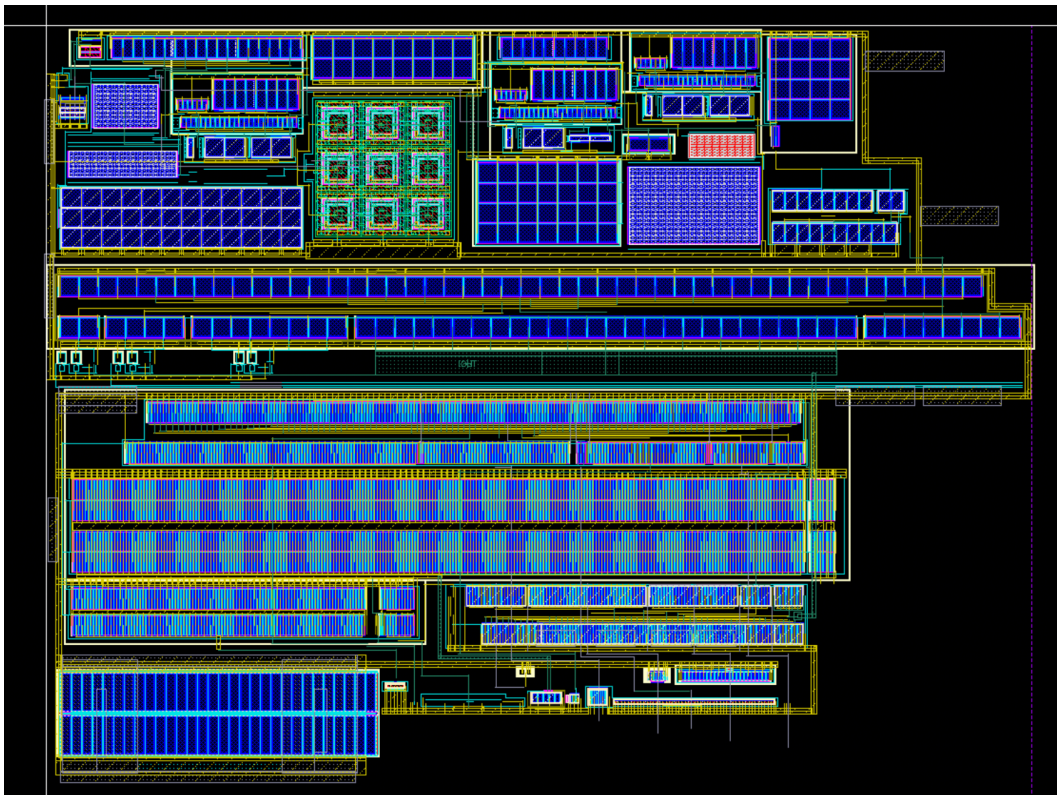


Figure 1.13: current reference and 3-bit DAC layout.

Bias [bit]	TEMP. [°C]	TT [µA]	FF [µA]	FS [µA]	SF [µA]	SS [µA]
000	-100	4.052	4.654	4.052	4.053	3.590
	-40	4.072	4.681	4.072	4.072	3.608
	0	4.066	4.678	4.066	4.066	3.601
	27	4.054	4.667	4.054	4.054	3.589
001	-100	4.364	**5.012**	4.364	4.364	3.866
	-40	4.385	**5.041**	4.385	4.385	3.885
	0	4.379	**5.038**	4.379	4.379	3.878
	27	4.365	**5.026**	4.365	4.366	3.865
010	-100	4.676	5.37	4.675	4.676	4.142
	-40	4.698	5.401	4.698	4.698	4.163
	0	4.691	5.398	4.691	4.691	4.155
	27	4.677	5.385	4.677	4.677	4.141
011	-100	**4.987**	5.728	**4.987**	**4.988**	4.418
	-40	**5.011**	5.761	**5.011**	**5.012**	4.44
	0	**5.004**	5.758	**5.004**	**5.004**	4.432
	27	**4.989**	5.744	**4.989**	**4.989**	4.417
100	-100	5.299	6.086	5.299	5.299	4.694
	-40	5.325	6.121	5.325	5.325	4.718
	0	5.317	6.117	5.317	5.317	4.709
	27	5.301	6.103	5.301	5.301	4.694
101	-100	5.611	6.444	5.611	5.611	**4.97**
	-40	5.638	6.481	5.638	5.638	**4.995**
	0	5.63	6.477	5.630	5.630	**4.986**
	27	5.613	6.462	5.613	5.613	**4.97**
110	-100	5.923	6.802	5.922	5.923	5.246
	-40	5.951	6.841	5.951	5.951	5.273
	0	5.942	6.837	5.942	5.942	5.263
	27	5.925	6.82	5.925	5.925	5.246
111	-100	6.234	7.160	6.234	6.234	5.523
	-40	6.264	7.201	6.264	6.264	5.550
	0	6.255	7.197	6.255	6.255	5.540
	27	6.236	7.179	6.236	6.236	5.522

Table 1.5: Values of current I_{DAC} by varying: DAC combinations, temperature and process parameters.

1.1.6 Current mirrors

Each block, described in appendix B, needs a specific current to work properly; these values are listed in table 1.6. All the required currents are a multiple of 5 µA (except the Shaper_2 block), so they can be easily obtained using a current generator and current mirrors, each with a different gain [8]. The Shaper_2 block current is generated using an 8-finger MOS in the main branch of the current mirrors and a 3-finger MOS in the mirror branch, obtaining a gain factor of $\frac{3}{8}$ (all the fingers must be characterized by the same W and L).

IP BLOCK	NOMINAL	MIRROR GAIN
CSA_1	10 µA	×2
CSA_2	50 µA	×10
CSA_3	250 µA	×50
INTEGRATOR	20 µA	×4
THRESHOLD	15 µA	×3
SHAPER_1	25 µA	×5
SHAPER_2	1.5 µA	$\times\frac{3}{8}$
DIFFERENTIATOR	20 µA	×4
COMPARATOR	50 µA	×10
S&H	10 µA	×2

Table 1.6: Currents needed by GAPS Front-end IP blocks

Lastly, the generated current I_{DAC} is mirrored in other branches with a mirror gain dependent on the block to bias. The required mirror gains are already listed in table 1.6. All the current mirrors are designed in cascode configuration in order to decrease the effects of process and mismatch parameters. As first analysis, the current mirrors, without considering the layout parasitic resistances and capacitances, have been evaluated for temperature range from −100 °C to 30 °C and for all the process cases. Results are shown in table 1.7. All these values are obtained using the current generator previously described. In order to obtain a current as similar as possible to the required one, in TT, FS, and SF cases the 3-bit DAC has been set to 011, in FF case it has been set to 001 and, finally, the SS case has been corrected with the 101 DAC code. The maximum relative errors of the simulation with respect to the ideal values, for each block, are:

- CSA_1: FF case, −40 °C, absolute error of 0.25 µA and a relative error of 2.5 %.
- CSA_2: FF case, −40 °C and 0 °C, absolute error of 0.40 µA and a relative error of 0.8 %.
- CSA_3: SS case, −100 °C, absolute error of 7.07 µA and a relative error of 2.82 %.
- Integrator: FF case, −40 °C, absolute error of 0.7 µA and a relative error of 3.5 %.
- Threshold Generator: FF case, −40 °C, absolute error of 0.47 µA and a relative error of 3.13 %.

- Shaper_1: SS case, −100 °C, absolute error of 0.67 µA and a relative error of 2.68 %.
- Shaper_2: SS case, −100 °C, absolute error of 0.02 µA and a relative error of 1.33 %.
- Differentiator: SS case, −100 °C, absolute error of 0.53 µA and a relative error of 2.65 %.
- Comparator: SS case, −100 °C, absolute error of 1.37 µA and a relative error of 2.74 %.
- S&H: SS case, −100 °C, absolute error of 0.25 µA and a relative error of 2.5 %.

The maximum relative error is found for the Integrator. SS case at −100 °C is, in general, the worst case scenario for the mirrored currents.

As a second analysis, a mismatch simulation for the typical case, at −40 °C and 3-bit DAC code set to 011, has been carried out. The results are listed in table 1.8, has been carried out. The mean results are in line with the required ones. The maximum and minimum values can be easily corrected by modifying the 3-bit DAC code, as demonstrated for the process simulations shown in table 1.7.

As third analysis, simulations considering the layout parasitic resistances and capacitances have been run. Simulations setting are always: typical case, at −40 °C and 3-bit DAC code set to 011. Results are shown in table 1.9.

Analog block	TEMP. [°C]	TT [µA]	FF [µA]	FS [µA]	SF [µA]	SS [µA]	id. [µA]
CSA_1	-100	10.12	10.20	10.11	10.14	10.04	10
	-40	10.19	10.25	10.19	10.19	10.15	
	0	10.16	10.23	10.16	10.16	10.12	
	27	10.13	10.20	10.13	10.13	10.09	
CSA_2	-100	49.52	49.93	49.35	49.63	48.63	50
	-40	50.06	50.40	50.04	50.09	49.86	
	0	50.03	50.40	50.02	50.05	49.82	
	27	49.90	50.29	49.88	49.91	49.67	
CSA_3	-100	247.42	249.50	246.56	247.99	242.93	250
	-40	250.27	251.99	250.17	250.42	249.20	
	0	250.15	252.02	250.05	250.25	249.07	
	27	249.46	251.44	249.39	249.54	248.34	
Integrator	-100	20.46	20.61	20.42	20.48	20.30	20
	-40	20.57	20.70	20.57	20.57	20.50	
	0	20.51	20.65	20.51	20.51	20.44	
	27	20.43	20.58	20.43	20.43	20.35	
Thr. Gen.	-100	15.29	15.40	15.26	15.31	15.17	15
	-40	15.38	15.47	15.37	15.38	15.33	
	0	15.34	15.44	15.36	15.34	15.28	
	27	15.28	15.39	15.28	15.28	15.22	
Shaper_1	-100	24.78	24.98	24.70	24.83	24.33	25
	-40	25.04	25.21	25.03	25.05	24.94	
	0	25.02	25.20	25.01	25.03	24.92	
	27	24.95	25.15	24.95	24.96	24.84	
Shaper_2	-100	1.50	1.51	1.50	1.50	1.48	1.5
	-40	1.50	1.51	1.50	1.50	1.50	
	0	1.50	1.51	1.50	1.50	1.50	
	27	1.50	1.51	1.50	1.49	1.49	
Diff.	-100	19.83	20.00	19.76	19.87	19.47	20
	-40	20.03	20.17	20.02	20.04	19.95	
	0	20.02	20.16	20.01	20.02	19.93	
	27	19.96	20.12	19.96	19.97	19.87	
Comp.	-100	49.52	49.94	49.35	49.63	48.63	50
	-40	50.07	50.41	50.04	49.63	49.86	
	0	50.04	50.41	50.02	50.10	49.83	
	27	49.90	50.30	49.89	49.91	49.68	
S&H	-100	9.93	10.00	9.90	9.95	9.75	10
	-40	10.02	10.08	10.02	10.02	9.98	
	0	10.00	10.08	10.00	10.01	9.97	
	27	9.98	10.06	9.98	9.98	9.94	

Table 1.7: current values obtained by using the current generator, its 3-bit DAC and the current mirrors deigned for the GAPS channel. In TT, FS, and SF cases the 3-bit DAC has been set to 011. In FF case it has been set to 001. In SS case the 3-bit DAC has been set to 101.

Analog block	Min [µA]	Max [µA]	μ [µA]	σ [µA]
CSA_1	9.75	10.63	10.18	0.14
CSA_2	47.36	52.71	50.05	0.82
CSA_3	236.69	263.16	250.21	4.04
Integrator	19.90	21.45	20.57	0.26
Thr. Gen.	14.87	16.09	15.37	0.19
Shaper_1	23.82	26.37	25.03	0.41
Shaper_2	1.40	1.63	1.50	0.03
Different.	19.05	21.15	20.03	0.33
Comparator	47.47	52.65	50.06	0.81
S&H	9.50	10.63	10.01	0.17

Table 1.8: mismatch Monte Carlo simulations (1000 iterations) of the current values mirrored in each GAPS analog block.

Analog block	ideal cur. [µA]	simulated cur. [µA]	relative error [%]
CSA_1	10	11.06	10.6
CSA_2	50	49.03	1.94
CSA_3	250	244.23	2.31
Integrator	20	21.55	7.75
Thr. Gen.	15	15.97	6.47
Shaper_1	25	26.46	5.84
Shaper_2	1.5	1.77	18
Different.	20	21.04	5.2
Comparator	50	51.93	3.86
S&H	10	9.97	0.3

Table 1.9: process and mismatch Monte Carlo simulations.

1.2 8 bit DAC for global threshold setting

An 8-bit Current Steering D/A Converter has been designed starting from a unary current source architecture [11, 12]. This IP block is responsible for setting the amplitude of two voltages V_{tp} and V_{tn} used by the threshold generator (described in appendix B) to generate the Signal-Over-Threshold (SOT) comparator threshold voltage. In particular, the difference between the two voltages, $\Delta V_t = V_{tp} - V_{tn}$, is used by the threshold generator: the higher ΔV_t, the higher the threshold of the SOT comparator. For design simplicity, the voltage V_{tp} remains constant by varying the DAC codes, whereas the voltage V_{tn} can vary from 0 V to $(V_{tp} + V_s)$, where V_s is a voltage margin which permits to obtain negative ΔV_t. From this point on, V_{tp} will be called V_{fix} and V_{tn} will be called V_{pos}. As a first step, the LSB of the DAC has been evaluated by considering the resolution, the range, and the gain of the channel. In order to generate 1 electron-hole pair ($e^- = 1.6 \cdot 10^{-19}$ C) in silicon, an energy of 3.6 eV is needed. Since the Charge Sensitive Amplifier (CSA) is characterized by a dynamic compression with MOS capacitor (appendix B), its gain is not constant. The maximum gain is at very low energies where it has a maximum value of 200 µV/keV. The Shaper block, instead, has a fixed gain of 1.2. Therefore, the total gain of these blocks (μ_g), at low energies, is:

$$\mu_g = \mu_{CSA} \cdot \mu_{shaper} = 200 \frac{\mu V}{keV} \cdot 1.2 = 240 \frac{\mu V}{keV}. \tag{1.60}$$

By the requirements of the project, the maximum energy to discriminate is around 1 MeV. Since the DAC bits are 8, the max value of the DAC codes is $2^8 - 1$. If each DAC code discriminates 4 keV, the maximum value value of energy discriminated is 1.02 MeV. This value is very near to the one required but, in order to add a margin of detected energy (V_s), it has been chosen that each DAC code discriminate 5 keV (a maximum value of energy discriminated of 1.275 MeV). In this case the DAC voltage LSB is

$$V_{pos,lsb} = 240 \frac{\mu V}{keV} \cdot 5\,keV = 1.2\,mV \tag{1.61}$$

and the max value of V_{pos} is

$$V_{pos,max} = V_{pos,lsb} \cdot 255 = 306\,mV. \tag{1.62}$$

1.2.1 8-bit DAC architecture

The 8-bit DAC is based on a current steering architecture as shown in fig. 1.14 [11, 13]. It is comprised of the following elements.

- A matrix of 16×16 unary current cells. The current of all the selected cells, I_p, flows in the positive branch, while the current of the non-selected cells, I_n, flows in the negative branch. These two currents can be defined as:

$$I_p = \sum_{c=0}^{255} I_{p,c} \tag{1.63}$$

$$I_n = \sum_{c=0}^{255} I_{n,c} \tag{1.64}$$

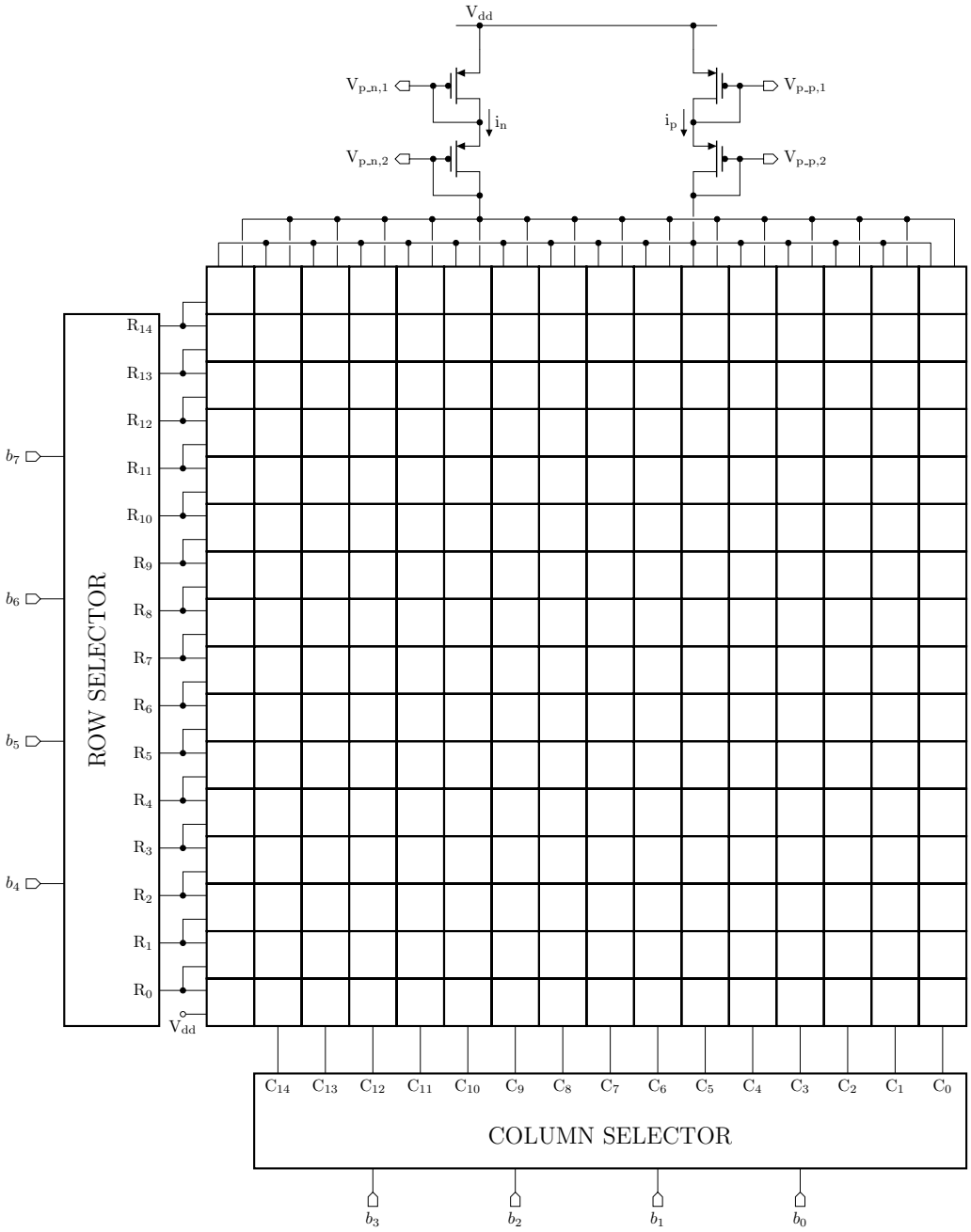


Figure 1.14: 8-bit DAC schematic.

- Two 4-bit binary-to-thermometer decoders. One decoder is used to selected the columns, the other is used to select the matrix rows. The less significant bits of the 8-bit DAC are connected to the column selector; while the most significant bits are connected to the row selector. As shown in eq. (1.65), if one row is selected, all the cells of that row are selected.

Since the DAC linearity is not fundamental in threshold setting, it is not required to adopt a common centroid or randomized approach.

1.2.2 4-bit binary-to-thermometer decoder

A 4-bit binary-to-thermometer decoder was needed for the design of the 8-bit DAC. Each combination in thermometer code is a sequence of 0s followed by a sequence of 1s. The decoder input is a n bit binary code, the corresponding output is a $2^n - 1$ bit thermometer code. Table 1.10 shows the thermometer codes for a 4-bit decoder. In fig. 1.15 the gate-level schematic diagram of the decoder circuit is shown. All the logic gates are made in their classic configuration using PMOS and NMOS.

Since in the envisioned application the decoder is used for the slow control of the ASIC, the dynamic performance is not taken into account. In the real experiment, the threshold will be set only one time after the start-up phase, so the switching time from a combination to another is not relevant.

input	output
0000	000000000000000
0001	000000000000001
0011	000000000000111
0100	000000000001111
...	...
1100	000111111111111
1101	001111111111111
1110	011111111111111
1111	111111111111111

Table 1.10: 4-bit binary-to-thermometer decoder input and output.

1.2.3 Unary current cell

The unary current cell that is the building block of the DAC 16×16 matrix is shown in fig. 1.16 [13, 12]. Each cell c is identified by a column R_i and a row C_j. All the cells are composed of:

- Two logic gates (1 OR port and 1 AND port). The logic gates are used in order to obtain:

$$s_c = (R_i \vee C_j) \wedge R_{i-1} \tag{1.65}$$

$$\overline{s_c} = \neg \left[(R_i \vee C_j) \wedge R_{i-1} \right] . \tag{1.66}$$

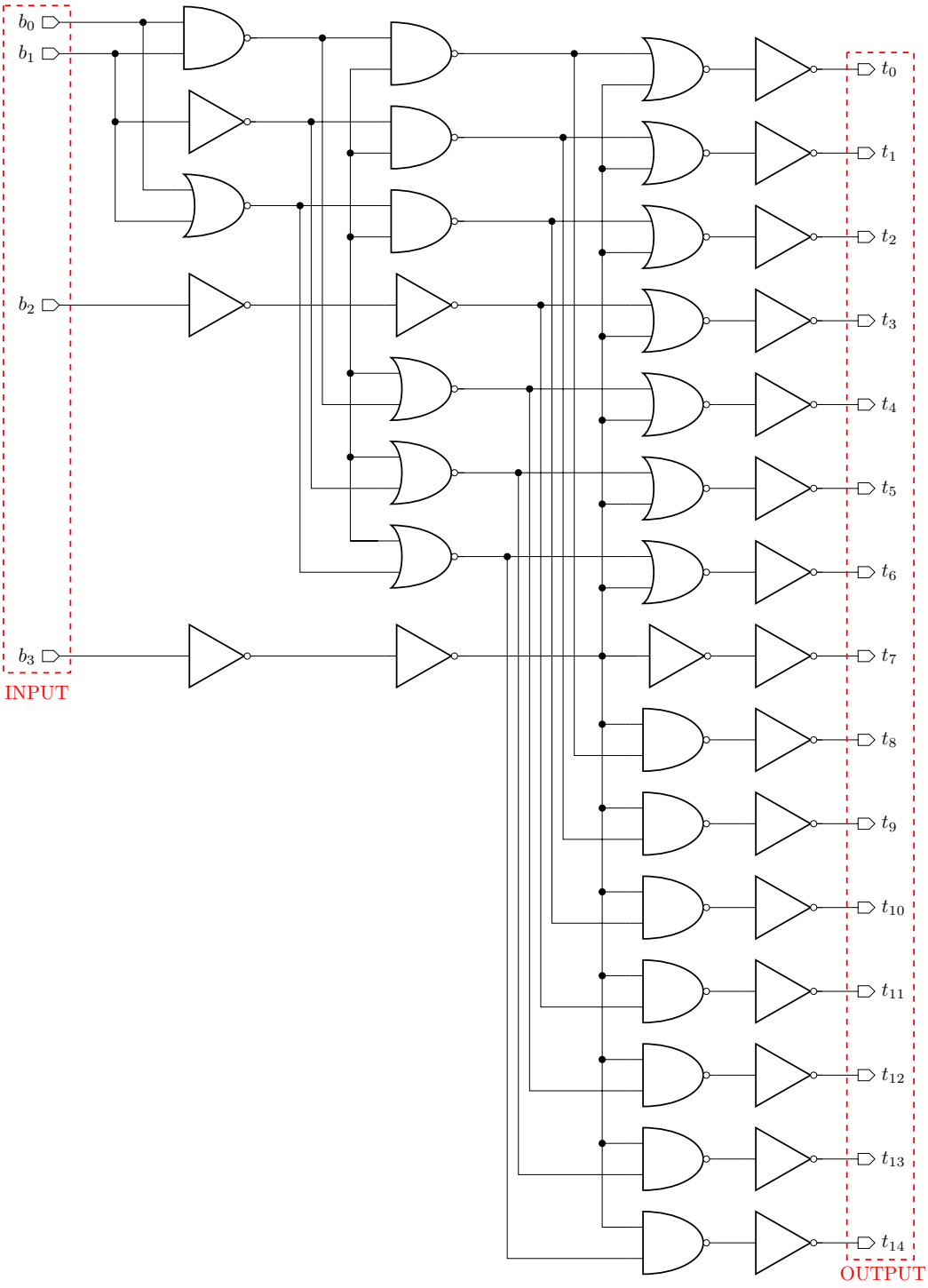


Figure 1.15: 4-bit binary-to-thermometer converter.

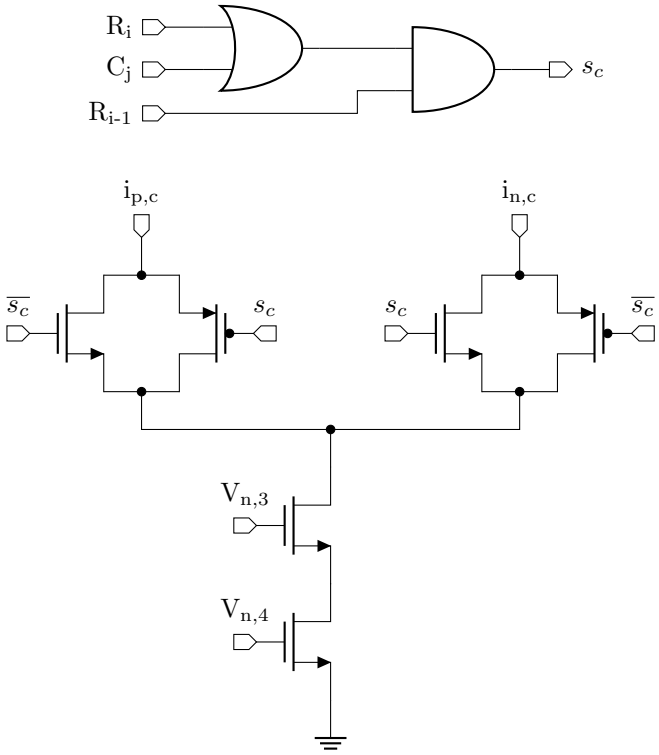


Figure 1.16: schematic of the 8-bit DAC cells.

The inputs are three logic signals. R_i and C_j are signals that identify the cell. R_{i-1} is coming from the previous row of the matrix.

- Two switches. Each switch is composed of 1 PMOS and 1 NMOS. If one switch is open, the other is closed. This happens because the NMOS of one switch is connected to the output of the logic gates while the NMOS of the other switch is connected to the negated output of the logic gates. The same happens for $\overline{s_c}$ for the PMOS.
- Two NMOS in cascode configuration. The gates of these transistors ($V_{n,3}$ and $V_{n,4}$) are connected to the gates of the 3-bit DAC of the current generator described in section 1.1.5 and shown in fig. 1.12. Since the cell ratio of the NMOS is 1:32 with respect to the 3-bit DAC NMOS, the current which flows in each cell is $I_{DAC}/32$.

$$I_c = \frac{5\,\mu\text{A}}{32} = 156.25\,\text{nA} \tag{1.67}$$

Due to the logic gates, if the cell is selected (s_c at logic 1) the current flows in the positive branch ($I_{p,c}$), otherwise (s_c at logic 0) in the negative branch ($I_{n,c}$). So the two currents which flow in the two branches of a cell c are:

$$I_{p,c} = s_c \cdot 156.25\,\text{nA} \tag{1.68}$$

$$I_{n,c} = \overline{s_c} \cdot 156.25\,\text{nA} \tag{1.69}$$

The unary current cell layout is shown in fig. 1.17. Its dimensions are 21 µm×38 µm.

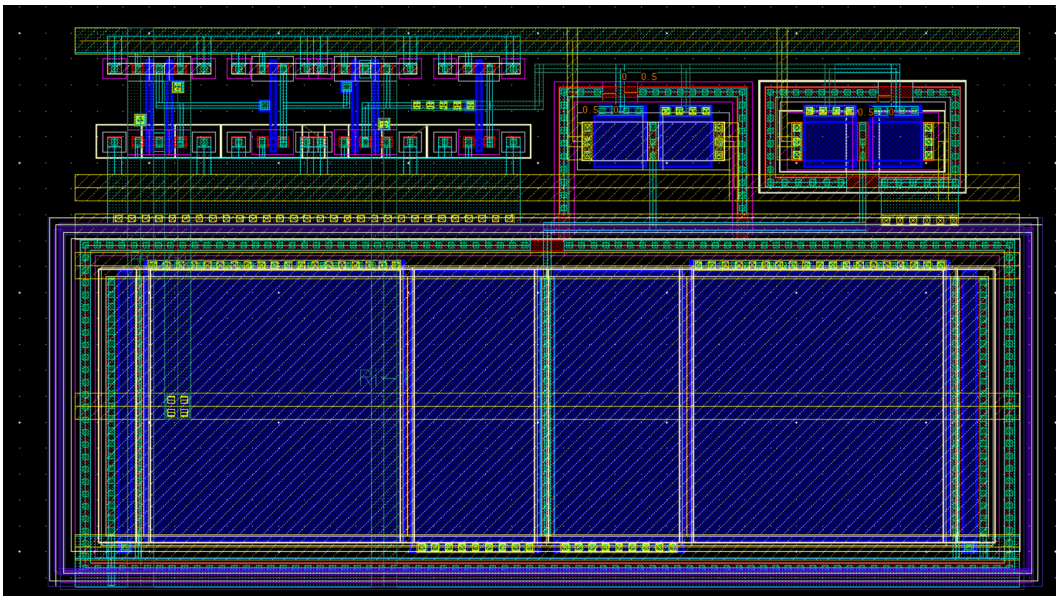


Figure 1.17: unary current cell layout.

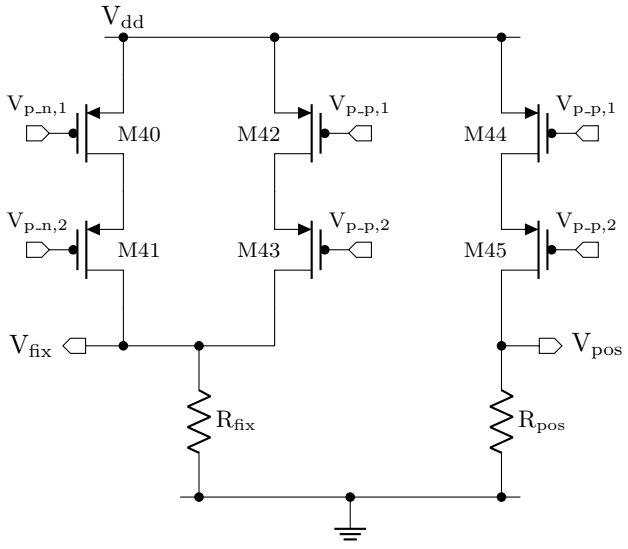


Figure 1.18: schematic of the current-to-voltage converter.

1.2.4 Threshold voltage generation

Starting from the current provided by the current steering DAC, a differential voltage is obtained based on the schematic shown in fig. 1.18. The PMOS of this part are connected in cascode mirror configuration to the cascode load of the 8-bit DAC. The current I_p flows in the branches composed of the couple (M42, M43) and (M44, M45), the current I_n flows in the branch composed of PMOS M40 and M41. The sum of the currents I_p and I_n flows in the resistor R_{fix} obtaining:

$$I_{fix} = I_p + I_n = 256 \cdot 156.25\,\text{nA} = 40\,\mu\text{A}, \tag{1.70}$$

The max value of the current which flows in R_{pos} is obtained when all the cells of the matrix are selected, obtaining

$$I_{pos,max} = 255 \cdot 156.25\,\text{nA} = 39.84\,\mu\text{A}. \tag{1.71}$$

The max value of I_{pos} is not 40 µA because one cell is non selectable due to the structure of the logic gates in each cell. The max value of selected cells is obtained when the row and column selectors have all 1s as output: $15 \cdot 16$ cells can be selected by row selector and other 15 cells by the column selector. In order to obtain the V_{pos} max value of 306 mV, R_{pos} has to be chosen in this way:

$$R_{pos} = \frac{V_{pos,max}}{I_{pos,max}} = \frac{306\,\text{mA}}{39.84\,\mu\text{A}} \simeq 7.68\,\text{k}\Omega. \tag{1.72}$$

The value of R_{fix}, instead, has been chosen in order to obtain the small margin V_s and the maximum value of discriminated energy of 1 MeV. This value is precisely obtained when V_{fix} has the same voltage of V_{pos} at a DAC code of 200. In fact, given that $\Delta V_t = V_{fix} - V_{pos}$, $\Delta V_{t,max} = V_{fix}$ when $V_{pos} = 0\,\text{V}$. $\Delta V_{t,max}$ can also be obtained as:

$$\Delta V_{t,max} = \mu_g \cdot E_{max} \tag{1.73}$$

where E_{max} is the maximum energy to be discriminated and μ_g is the gain of the channel at the shaper output as reported in eq. (1.60). So, considering that $\Delta V_{t,max} = V_{pos,lsb} \cdot \#DAC\ code$:

$$\#DAC\ code = \frac{\mu_g \cdot E}{V_{pos,lsb}} = \frac{240\,\mu\text{V/keV} \cdot 1\,\text{MeV}}{1.2\,\text{mV/DAC code}} = 200\,\text{DAC code}, \tag{1.74}$$

where $\#DAC\ code$ is the DAC value that permits to obtain the required $\Delta V_{t,max}$. Consequently:

$$V_{fix} = 200\,\text{DAC code} \cdot 1.2\,\text{mV} = 240\,\text{mV}. \tag{1.75}$$

In order to obtain this value of V_{fix}, $R_{fix} = 6\,\text{k}\Omega$. However, to guarantee the minimum ΔV_t found in the eq. (1.75) in all process cases, the chosen value of the resistor R_{fix} is 7 kΩ, as will be explained in the next section. This resistor permits to obtain a maximum $\Delta V_t = 280\,\text{mV}$ which corresponds to a maximum discriminated energy of ~1.17 MeV in the typical case. All the resistors have been chosen using the method already explained in section 1.1.4, in order to guarantee the temperature invariance.

The entire 8-bit DAC layout is shown in fig. 1.17. Its dimensions are 800 µm×480 µm.

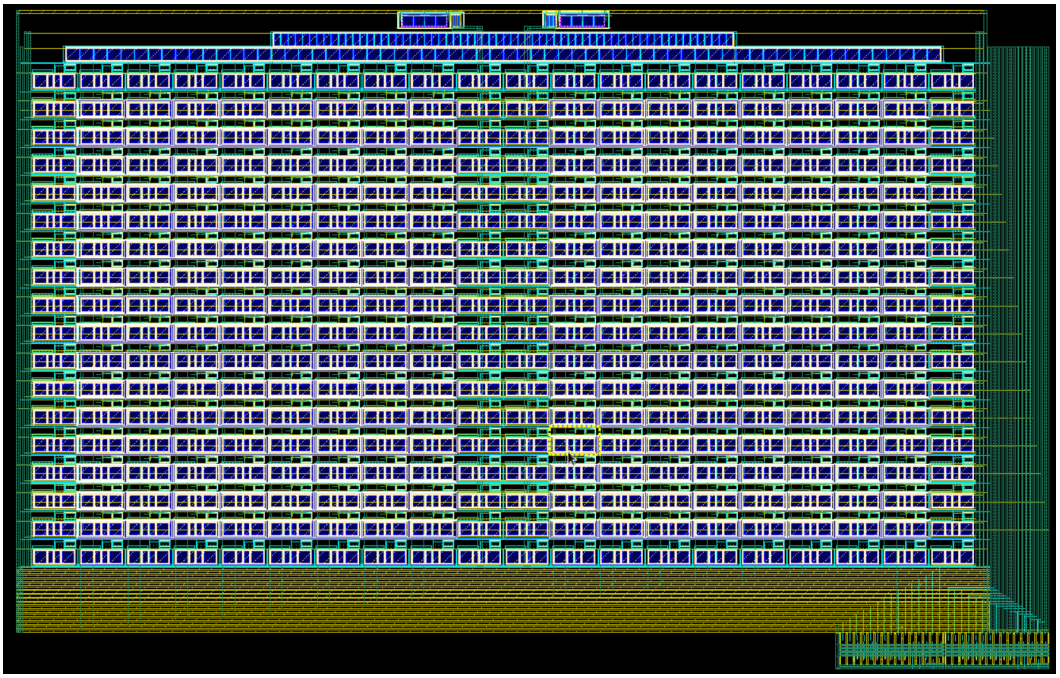


Figure 1.19: 8-bit DAC layout.

1.2.5 Simulations results

All the simulations have been carried out by evaluating the effects of temperature, supply voltage and process parameters variation on the generated threshold voltage. Results are shown in fig. 1.20 (V_{fix}) and fig. 1.21 (V_{pos}). It can be observed that both voltages are almost independent of temperature (−50 °C, −40 °C, 0 °C and 27 °C in simulations) and supply voltage (1.62 V, 1.8 V and 1.98 V) variation. However, since the resistors accuracy is in the order of ±15 %, by varying the process parameters, the voltages V_{pos} and V_{fix} have different values with respect to the nominal ones. Thanks to the solution adopted in design of the R_{fix} and R_{pos} resistors, used to generate the V_{fix} and V_{pos} voltages, FS and SF corners do not affect the V_{fix} and V_{pos} voltages. Figure 1.20 shows V_{fix} in all corners for all temperatures and supply voltages. These results can be grouped in

- FF corner: $V_{fix} \simeq 320\,\text{mV}$. This value corresponds to a maximum discriminated energy of 1.33 MeV.
- TT,FS and SF corners: $V_{fix} \simeq 280\,\text{mV}$. As previously described, this value corresponds to a maximum discriminated energy of 1.17 MeV.
- SS corner: $V_{fix} \simeq 240\,\text{mV}$. This value corresponds to a maximum discriminated energy of 1 MeV. The selection of the $R_{fix} = 7\,\text{k}\Omega$ ensures the discrimination of 1 MeV also for SS case, which was one of the requirements of the 8-bit DAC.

Figure 1.21 shows V_{pos} in the same situations shown for V_{fix}, and for V_{pos}. The results they can be grouped in:

- FF corner: $V_{pos,max} \simeq 348\,\text{mV}$, $V_{pos,lsb} \simeq 1.36\,\text{mV}$ and consequently $E_{lsb} \simeq 5.7\,\text{keV}$. V_{pos} intersects V_{fix} with a DAC code of 235.

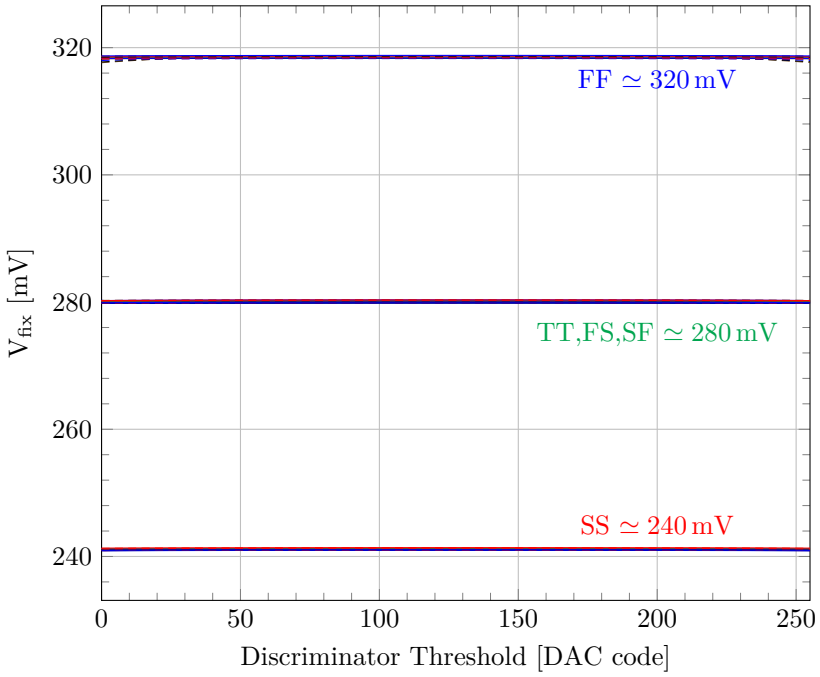


Figure 1.20: V_{fix} as obtained by varying process parameters, temperature and supply voltage.

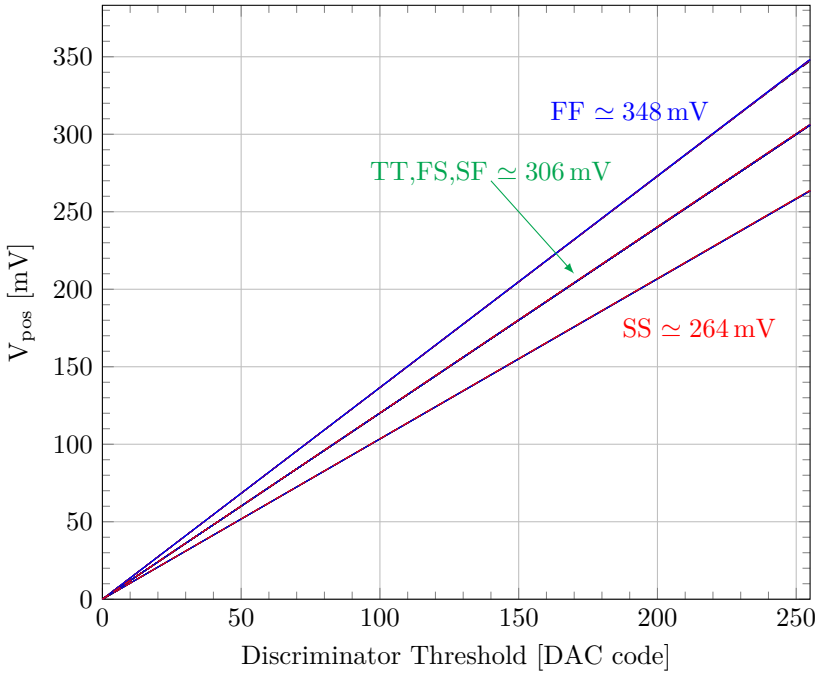


Figure 1.21: V_{pos} as obtained by varying process parameters, temperature and supply voltage.

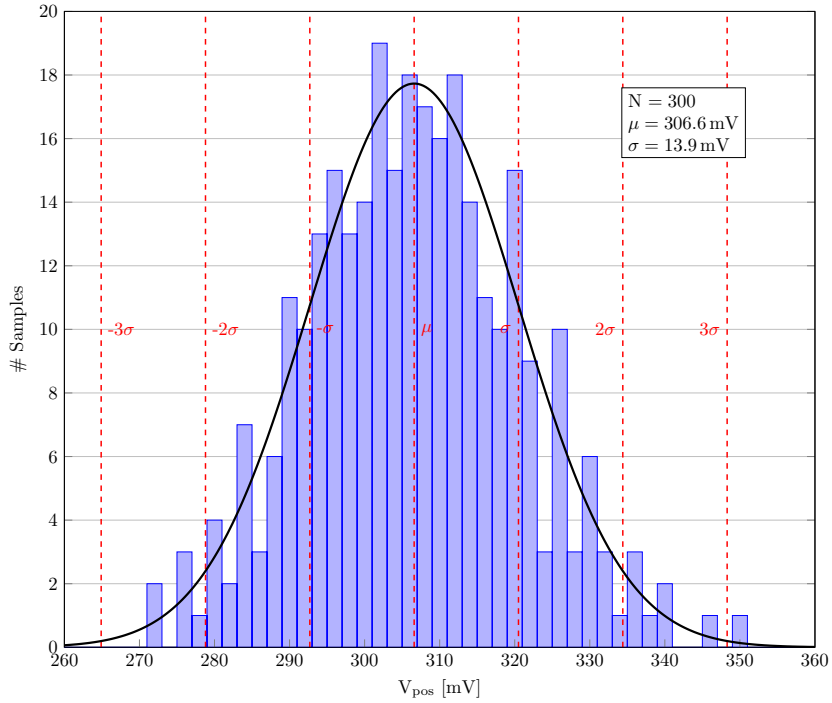


Figure 1.22: $V_{pos,max}$ process simulations with a temperature of −40 °C and 1.62 V supply voltage.

- TT, FS and SF corners: these cases are already described in the previous section. $V_{pos,max} \simeq 306$ mV, $V_{pos,lsb} = 1.2$ mV and consequently $E_{lsb} = 5$ keV. V_{pos} intersects V_{fix} with a DAC code of 233.
- SS corner: $V_{pos,max} \simeq 264$ mV, $V_{pos,lsb} \simeq 1.04$ mV and consequently $E_{lsb} \simeq 4.3$ keV. V_{pos} intersects V_{fix} with a DAC code of 230.

In the histogram in fig. 1.22, process simulations with temperature of −40 °C and 1.62 V supply voltage are shown. The 8-bit DAC is mainly affected by process, due to the resistor R_{fix} and R_{pos}, as described before. The considerations already written for corners simulations are valid also for mismatch simulations.

2 Characterization of 4 and 8 channels processors for the GAPS Si(Li) detector readout

The focus of this chapter is the experimental characterization of the analog readout channel, whose block diagram is shown in fig. 2.1, included into ASICs named SLIDER4 and SLIDER8. A low-noise charge sensitive amplifier (CSA), featuring dynamic signal compression, integrates the charge delivered by the strips of the Si(Li) detector by means of a non-linear MOS capacitor in the feedback loop [14]. A Krummenacher network is responsible for charge restoration in the feedback capacitance and for compensation of the detector leakage current. An injection capacitance has been integrated at the CSA input for calibration purposes. For Signal-to-Noise optimization, the amplifier is followed by a unipolar second order semi-Gaussian time invariant filter featuring 8 selectable peaking times (from 0.3 to 1.8 µs). The signal from the strip, after amplification and filtering, undergoes three different conditioning processes. On one side, it is converted from single-ended to differential and then it is compared to a preset differential threshold of a discriminator which can generate a Signal-Over-Threshold (SOT) pulse. A single-ended to differential sample & hold provides a signal proportional to the shaper output peak to the subsequent differential SAR ADC for analog information detection. In normal operation, the S&H sampling signal (CONV) is provided from outside the ASIC with a trigger generated by the TOF system. When the ASIC is operated in self-trigger mode, that is during calibration, the sampling signal is generated internally starting from the information provided by the zero-crossing discriminator output

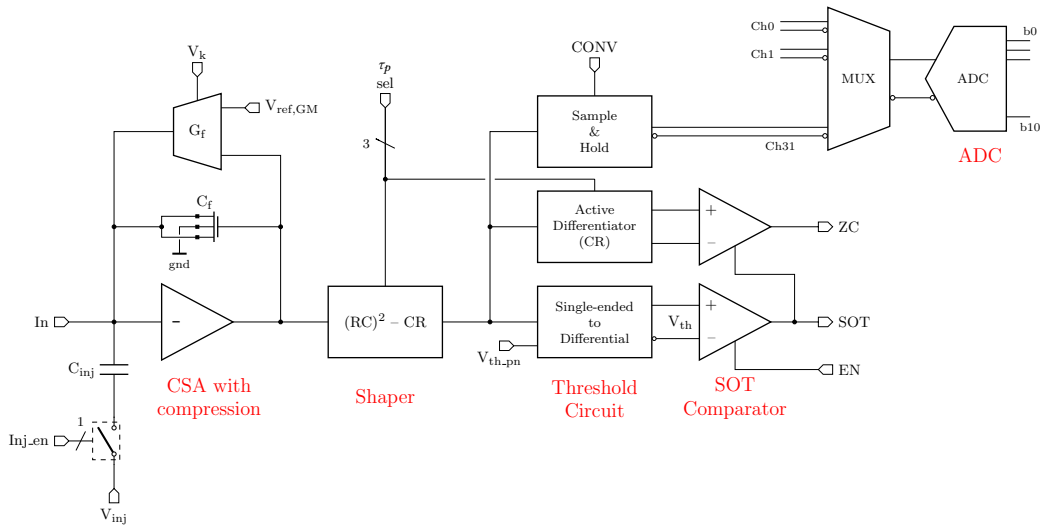


Figure 2.1: front-end channel schematic.

signal (ZC), which is synchronous with the shaper signal peak and is obtained with a further differentiation of the shaper output.

In this chapter two GAPS prototypes of the final ASIC, called SLIDER4 and SLIDER8 respectively, will be described and the results of their characterization will be illustrated.

2.1 SLIDER4: full analog 4 channels readout ASIC

SLIDER4 (SiLI DEtector Readout 4) is a protoype of the final ASIC that will be produced for the GAPS experiment. SLIDER4 is a 4 channels simplified version of the final circuit which will include 32 channels. In two of the four channels, the output of all the blocks making up the channel can be tested, while in the other two, only the channel output node is available. SLIDER4 prototype does not have a digital back-end which can generate control signals and reference voltages, thus all the signals and voltages have to be generated by external sources. It also includes the Band-Gap Reference and the current generator described in the previous chapter.

During the testing phase, GAPS detector was not connected to the input of the channels, so an injection circuit has been specifically designed and integrated in each channel. The injection circuit is described in section 2.1.1.

The experimental results of this prototype have been fundamental in order to correct potential errors of the final ASIC which will be described in section 2.1.3.

2.1.1 Injection circuit

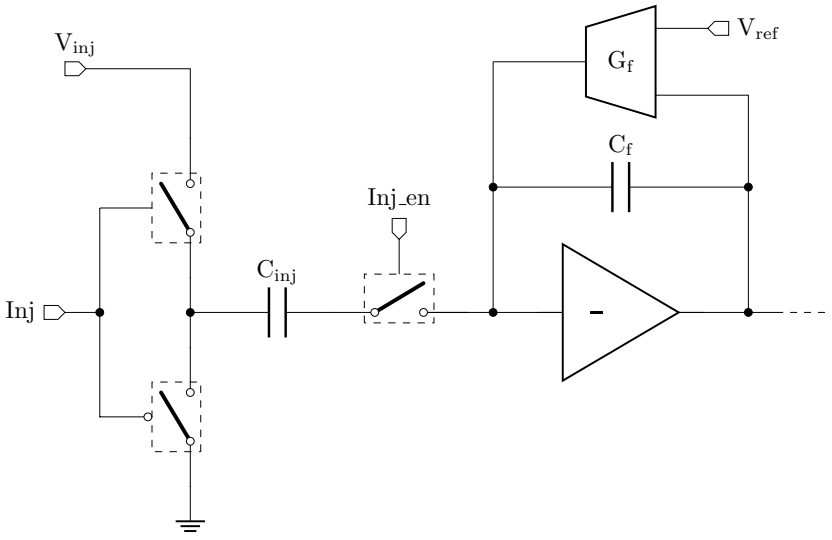


Figure 2.2: injection circuit used to test SLIDER4 channel.

The injection circuit permits to generate current pulses which simulate the release of charge due to the passage of an antiparticle through the GAPS detector. This circuit is shown in fig. 2.2.

The main components of the circuit are:

- The injection capacitance C_{inj} of 890 fF, that permits to calculate the injected charge as $Q = C \cdot \Delta V$. As already explained in section 1.2, an incoming particle with a 3.6 eV energy in a Si(Li) detector would release an electron-hole pair, which corresponds to a charge of $1.6 \cdot 10^{-19}$ C. A conversion factor can be calculated as:

$$k_n = \frac{1.6 \cdot 10^{-19}\,\mathrm{C}}{3.6 \cdot 10^{-3}\,\mathrm{keV}} = 0.044\,\frac{\mathrm{fC}}{\mathrm{keV}} \tag{2.1}$$

  Using this result, it is possible to obtain an expression of the energy of the particle, crossing the GAPS detector, function of V_{inj}:

$$E = \frac{C_{inj} \cdot V_{inj}}{k_n} = \frac{890\,\mathrm{fF} \cdot V_{inj}}{0.044\,\mathrm{fC/keV}}. \tag{2.2}$$

- Two switches: one set by *inj* signal (normally set to logic 1) and one by $\overline{inj}$. When the *inj* signal passes from logic 1 to logic 0, the capacitor C_{inj}, which was previously connected to V_{inj}, is now connected to ground. In this way a current spike is generated due to the discharge of the capacitor C_{inj}, simulating the charge injection. In more specific terms the intensity of the spike current is given by $i = C_{inj} \cdot d\Delta V/dt$, whose value is proportional to the simulated injected charge.

- An additional switch, controlled by the signal *Inj_en*. This switch permits to select in which channel the charge will be injected. This has been added for testing purposes and, in the final version of the channel, when the channel will be connected to the detector, to disconnect the channel from the injection circuit.

2.1.2 SLIDER4 test board

Each SLIDER4 ASIC has been soldered on a small daughter board. This board can be placed on the test board by means of a socket specifically designed (male connectors on the daughter boards and female connector on the test board). This allows for placing and replacing different SLIDER4 ASICs without soldering them to and desoldering them from the test board.

A test board has been specifically designed in order to test SLIDER4 channel blocks. The supply voltage of the test board is ±7 V. The main components of the test board are listed below:

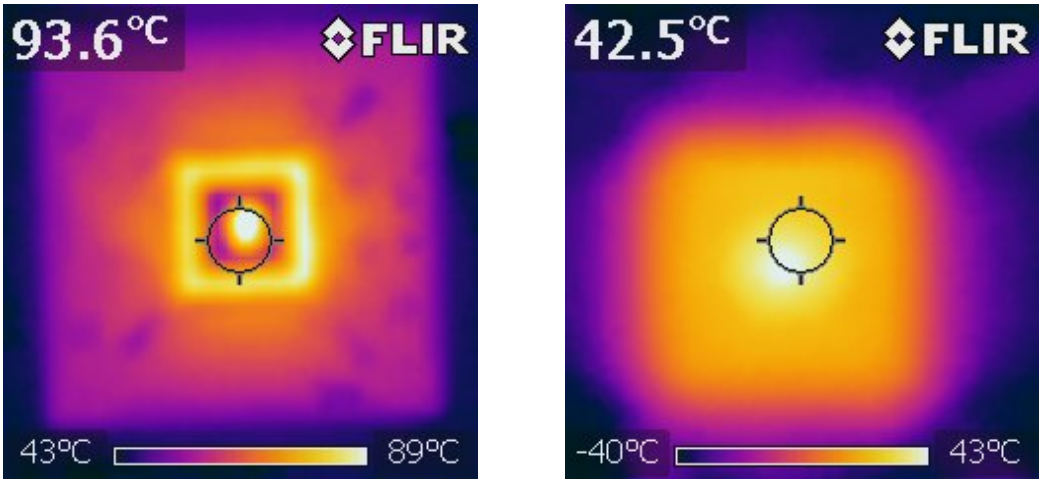
- 12 voltage references and 1 current reference, which generate specific voltages and currents for the correct operation of the ASIC.

- 2 LEMO connectors, used to provide two threshold voltages (V_{tp} and V_{tn} that, in pSLIDER32 version of the ASIC, will be generated by the 8-bit DAC described in section 1.2.1).

- 1 LEMO connector, used to provide the voltage V_{inj} (described in section 2.1.1).

- 3 test points, used to obtain the output voltages of the bandgap voltage reference and the current generator described in section 1.1.1 and section 1.1.3.

- 3 switches, used to manually select the peaking time of the shaper block.



(a) SLIDER4 ASIC temperature during tests at room temperature

(b) SLIDER4 ASIC temperature during tests at −40 °C

Figure 2.3: SLIDER4 ASIC photos taken with a thermal imager

- 8 buffers, connected to the test nodes of the channels. The buffer output can be read using an oscilloscope in order to verify that all the blocks of the channels work correctly. The main aim of these buffers is to decouple the test nodes from the load at the oscilloscope input.
- 1 socket for the SLIDER4 daughter board placing.

2.1.3 Experimental results

Different measurements have been carried out on the main blocks integrated in the SLIDER4 ASIC. The main blocks which were tested are:

- Bandgap Voltage Reference
- Current generator
- Charge Sensitive Amplifier
- Shaper
- Integrator
- Differentiator

Before starting to detail the experimental results, it has to be noted that an issue, related to a non-properly connected pad protection, was identified. The pad drew a large current and this problem made the ASIC temperature rise to a higher value than what was set for testing. Some pictures were taken with a thermal imager in order to confirm this behavior. In fig. 2.3a the ASIC is tested at room temperature reaching 100 °C, a value much higher than expected. In fig. 2.3b SLIDER4 is tested inside a refrigerator at −40 °C. Also in this case the actual ASIC temperature is much higher than expected, reaching values of 45 °C.

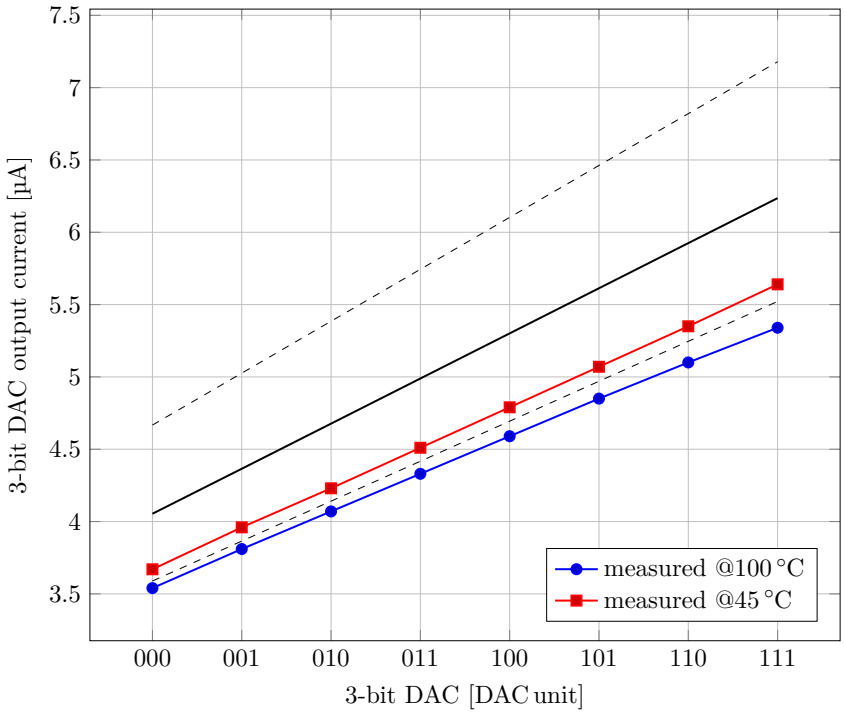


Figure 2.4: 3-bit DAC currents as a function of the DAC unit. The black line represents the typical case at room temperature. The lower dashed line represents the SS case whereas the higher dashed line represents and FF case at room temperature.

Despite the above mentioned issue, it has been possible to verify the functionality of all the structures, allowing for an extensive testing of the implemented readout architecture. All measurements have been carried out on channel 3, which was less affected by supply voltage problems, at a room temperature of 27 °C (which corresponds to the ASIC temperature of 100 °C). In the last part of the section an evaluation of the noise performance has been made.

Bandgap and current generator

The first blocks which have been tested are the bandgap voltage reference and the current generator. The SLIDER4 ASIC was tested at room temperature and at −40 °C, but due to the incidental temperature offset problem described at the beginning of section 2.1.3, the real ASIC temperature is much higher than the environment's. The measurements and the simulations of the bandgap voltage reference and of the output of the current generator are compared in table 2.1. With respect to results reported in sections 1.1.1 and 1.1.3, which consider a temperature range from −100 °C to 30 °C, new simulations have been performed in order to evaluate the block performance at the actual operating temperature. Even considering the increased temperature, the results are very promising since these blocks can operate correctly. In fact:

- the bandgap output voltage in the refrigerator at −40 °C (ASIC temperature of 45 °C) is very similar to the one obtained in the simulations;

- the value of the bandgap output voltage at 100 °C is slightly different than the simulated one which is consistent with the difference between the temperature at which the measurements were performed and the ones used in the simulations;
- the currents value are perfectly in the range of the ones obtained in the simulation. The measured current is very similar to the simulated one in the SS case (described in section 1.1.3).

TEMP. [°C]	measured		simulated	
	BG_V_{out} [V]	BG_i_{out} [µA]	BG_V_{out} [V]	BG_i_{out} [µA]
45 (-40)	1.273	4.51	1.270	4.3 - 5.7
100 (27)	1.294	4.44	1.265	4.2 - 5.8

Table 2.1: measured and simulated Bandgap voltage output (BG_V_{out}) and current generator output (BG_i_{out}). The temperature in brackets is the ambient temperature, the other is the measured chip temperature. Simulations refers to measured chip temperature.

In fig. 2.4 the currents generated by the 3-bit DAC, described in section 1.1.5, are shown. In the figure, the TT (continuous black line), SS (dashed line in the lower part of the plot) and TT (dashed line in thee upper part of the plot) simulation cases at room temperature are shown. As can be seen, this SLIDER4 ASIC is near the SS case. Since the ASIC temperature during the test was very high, the current generated is a bit lower than the SS case in the simulations. However, by using the DAC code 101, the output current is very close to the required 5 µA even for the 100 °C case.

Charge Sensitive Amplifier

CSA output measurements have been carried out in the time domain using of a LeCroy WavePro 735zi ocilloscope. The results are shown in fig. 2.5. The DC component of the signal has been removed in order to easily compare the simulations with the measurements. As an example, results are shown for an injected charge corresponding to 0.792 nC (18 MeV). The rise time, defined as the time between 10 % and 90 % of the voltage step, is approximately 20 ns. The rise time is slightly higher with respect to the simulation (5 ns), however it is much lower than the integration time that can be seen in fig. 2.8. The CSA amplitude measured is lower than the simulation, although the difference is compatible with process variation effect. The discharge time, here defined as the time between the injection and the time at which the signal crosses the baseline, depends on the injected charge. The baseline crossing is related to the negative tail following the positive pulse and due to the zero in the origin in the transfer function of the CSA [15]. In fig. 2.6 the charge restoration phase of the CSA output is shown. The CSA has a discharge time greater (700 µs) than the one obtained in the simulations (350 µs) likely to be ascribed to the non optimal bias condition that makes the discharging current lower than expected. However, the higher discharge time, will not be a problem in real experiment because the expected event rate is very low (about 100 Hz).

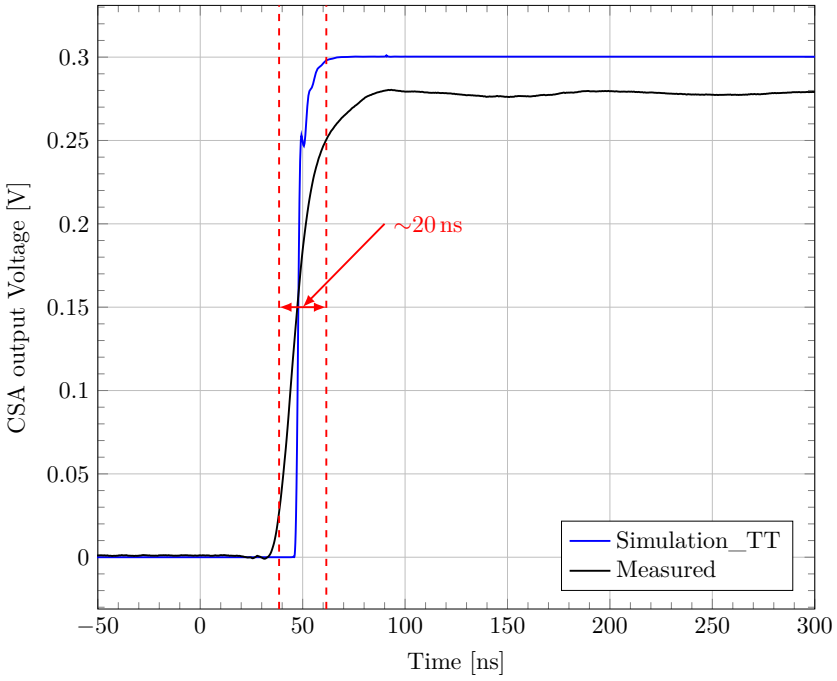


Figure 2.5: channel 3 CSA output, in the time domain. The rise time is highlighted.

An input-output transfer function measurement has been carried out by varying V_{inj} from 1 mV to 1.8 V. The results of this measurement are shown in fig. 2.7. The incoming energy values corresponding to the minimum and the maximum input voltage amplitude used in the measurements are:

$$E_{inj,min} = 1\,\text{mV} \cdot 890\,\text{fF} \cdot \frac{3.6 \cdot 10^{-3}\,\text{keV}}{1.6 \cdot 10^{-19}\,\text{C}} = 20\,\text{keV}\ (0.89\,\text{fC}),$$

$$E_{inj,max} = 1.8\,\text{V} \cdot 890\,\text{fF} \cdot \frac{3.6 \cdot 10^{-3}\,\text{keV}}{1.6 \cdot 10^{-19}\,\text{C}} = 36\,\text{MeV}\ (1.6\,\text{pC}).$$

The non-linearity of the CSA output, due to the dynamic compression, is clearly visible. The input-output channel characteristic can be divided in two parts:

- high gain region (low energies). The average low energy gain of the simulations, $\mu_{CSA,sim} = 150\,\mu\text{V/keV}$, is very close to the measured one, which is $\mu_{CSA,meas} = 140\,\mu\text{V/keV}$.
- low gain region (high energies). The average high energy gain of the simulations, $\mu_{CSA,sim} = 4.0\,\mu\text{V/keV}$, is very close to the measured one, which is $\mu_{CSA,meas} = 4.2\,\mu\text{V/keV}$.

The dynamic compression is implemented by using a MOS instead of a conventional capacitor C_f (as explained in appendix B). The value of the equivalent MOS capacitance is:

- high gain region: $C_f = 314\,\text{fF}$;
- low gain region: $C_f = 10.5\,\text{pF}$.

Measurements show that the CSA can operate in the required energy range with a gain very similar to the one obtained in the simulations.

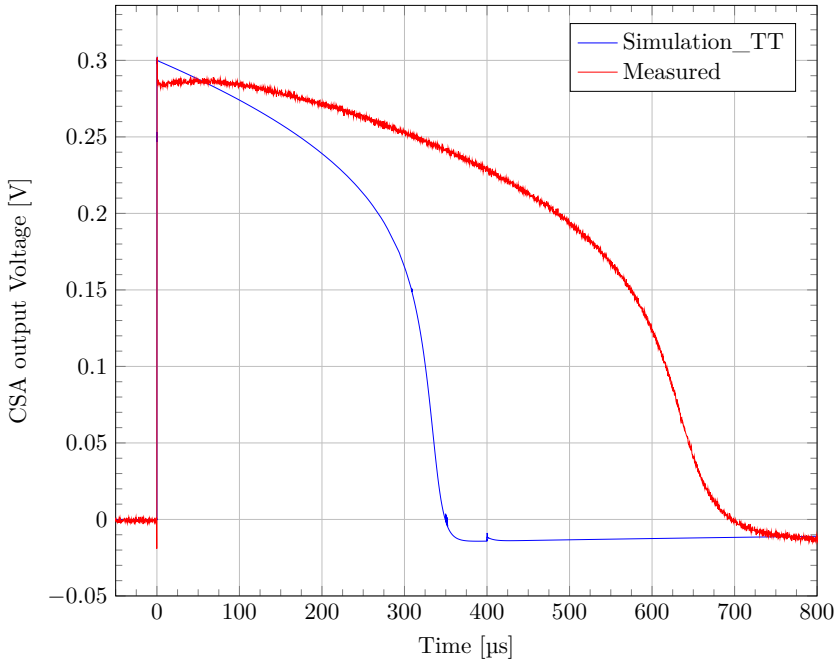


Figure 2.6: channel 3 CSA output, in the time domain.

Integrator

The integrator (the first part of the shaper block) output has been acquired by varying the peaking time. The obtained data is shown in fig. 2.8. As can be seen from this figure, the integrator output reaches the same asymptotic voltage value for all the peaking times. Moreover, the integration time varies in agreement with the shaper peaking times shown fig. 2.9.

Shaper

Measurements of the signal at the shaper output were carried out for different values of the peaking time. Results are shown in fig. 2.9. The shaper is the block most affected by the temperature issues described at the beginning of the subsection. This is the reason why measurement results do not exactly reflect the simulations. The first spotted problem is that the amplitude of the shaper output increases by increasing the peaking time instead of what was observed in the simulations where the shaper output amplitude decreased by increasing the peaking time. The second problem is that the measured peaking times are higher than the simulation ones. A comparison of peaking times is listed in table 2.2. This effect likely to be ascribed to a shift in the poles of the shaper transfer function due to a change in the transconductance feedback stage.

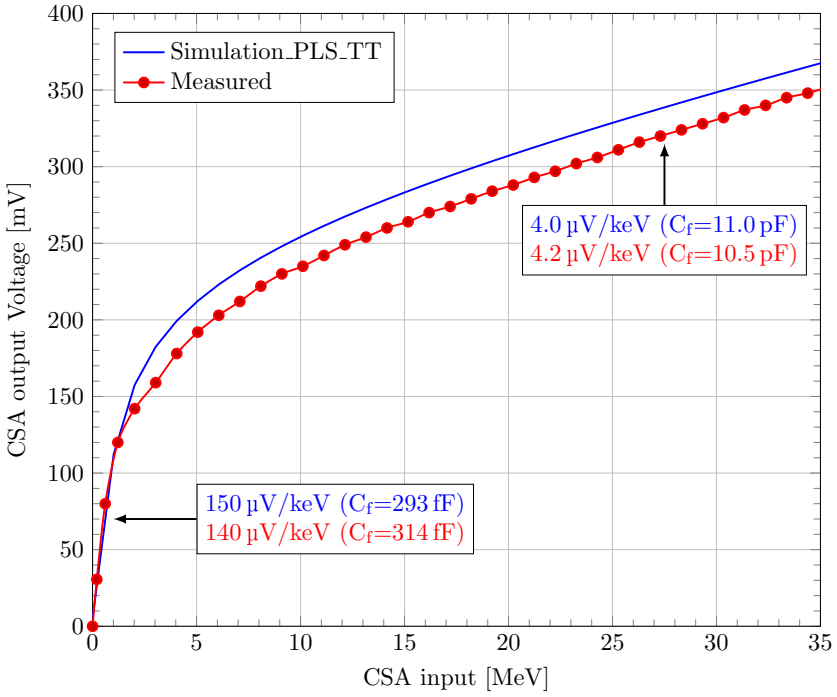


Figure 2.7: channel 3 input-output characteristic for an injected charge corresponding to an energy range from 20 keV to 35 MeV

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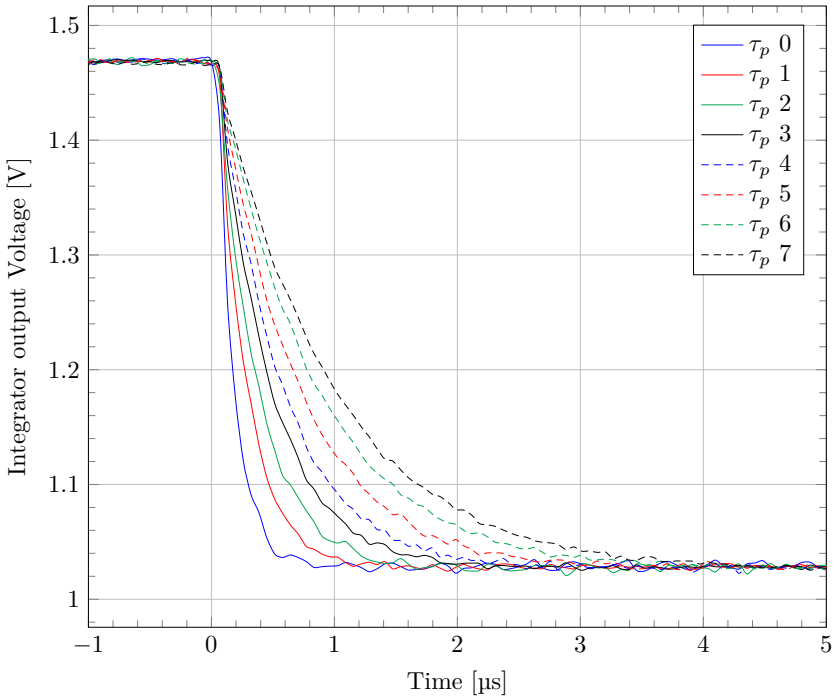

Figure 2.8: channel 3 integrator output, in the time domain.

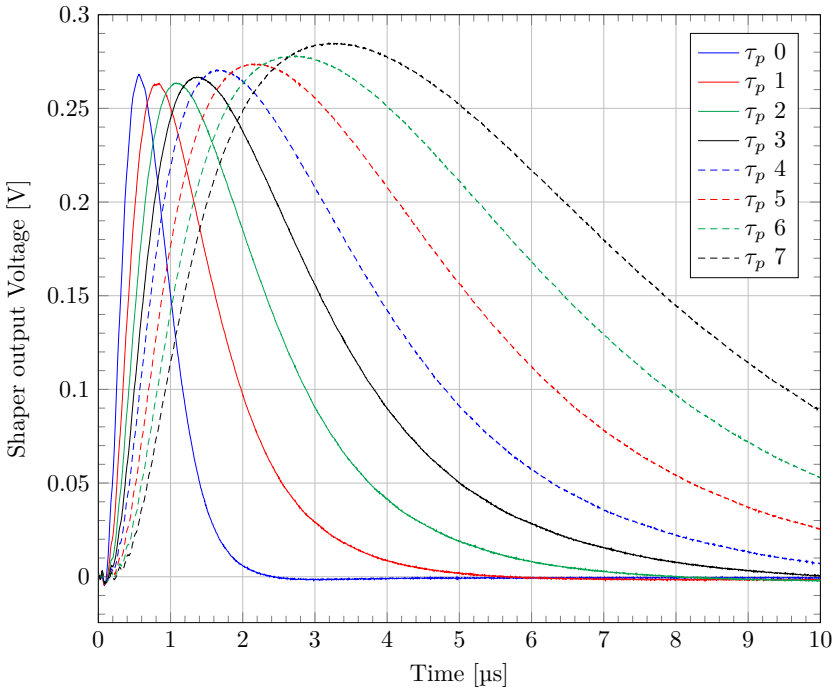

Figure 2.9: channel 3 shaper output for all peaking times.

τ_p simulated [µs]	τ_p measured [µs]
0.30	0.42
0.50	0.59
0.65	0.87
0.85	1.12
1.00	1.42
1.30	1.92
1.50	2.45
1.80	3.12

Table 2.2: comparison between measured and simulated peaking times for the signal at the SLIDER4 shaper output.

Differentiator

A differentiator has been designed in order to provide the inverted first derivative of the shaper output. The output of this block has been measured for different values of the shaper peaking time and controlling that the derivative operation is correct: the instant where the derivative is zero must correspond to the instant when the shaper output reaches its maximum value. The results are depicted in fig. 2.10. Peaking time 0 is not shown in order to keep the figure clear and easy to understand.

The behavior of the differentiator is as expected. The shaper peaking time and the

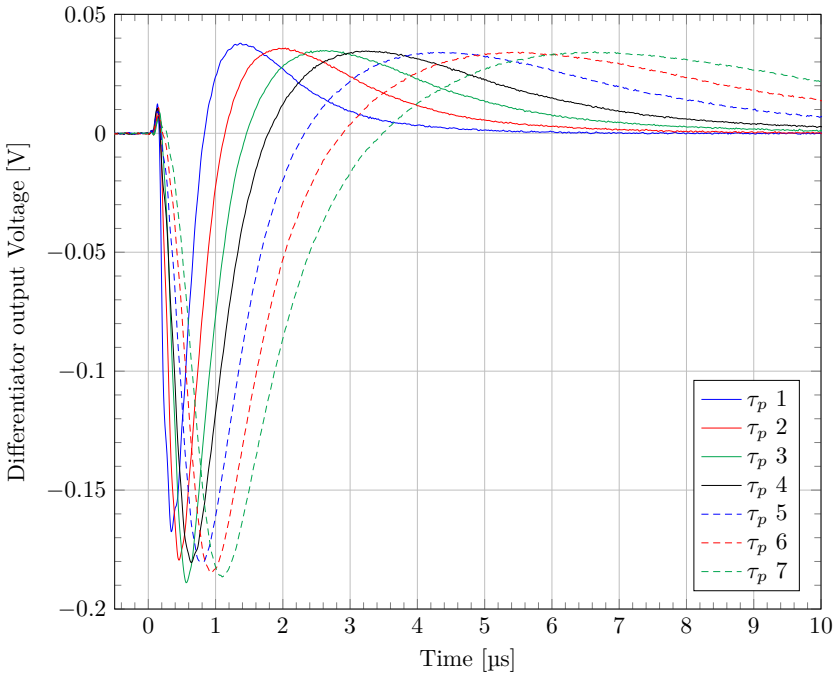

Figure 2.10: channel 3 differentiator output for peaking times from 1 to 7.

differentiator zero-crossing (ZC) times are listed in table 2.3. The delay between the ZC and the peaking time can be ascribed to the use of an approximated differentiator. Since the SLIDER4 shaper output has a peaking time greater than the simulated one, the differentiator zero-crossing time is greater than the simulated one.

τ_p measured [µs]	ZC [µs]
0.42	0.58
0.59	0.83
0.87	1.14
1.12	1.46
1.42	1.78
1.92	2.33
2.45	2.90
3.12	3.48

Table 2.3: comparison between measured peaking times of the SLIDER4 shaper and the Zero-Crossing time of the SLIDER4 differentiator.

Equivalent Noise Energy

The channel resolution has been evaluated in terms of Equivalent Noise Energy (ENE), that is the energy released in the detector that provides a Signal-to-Noise ratio of 1. ENE

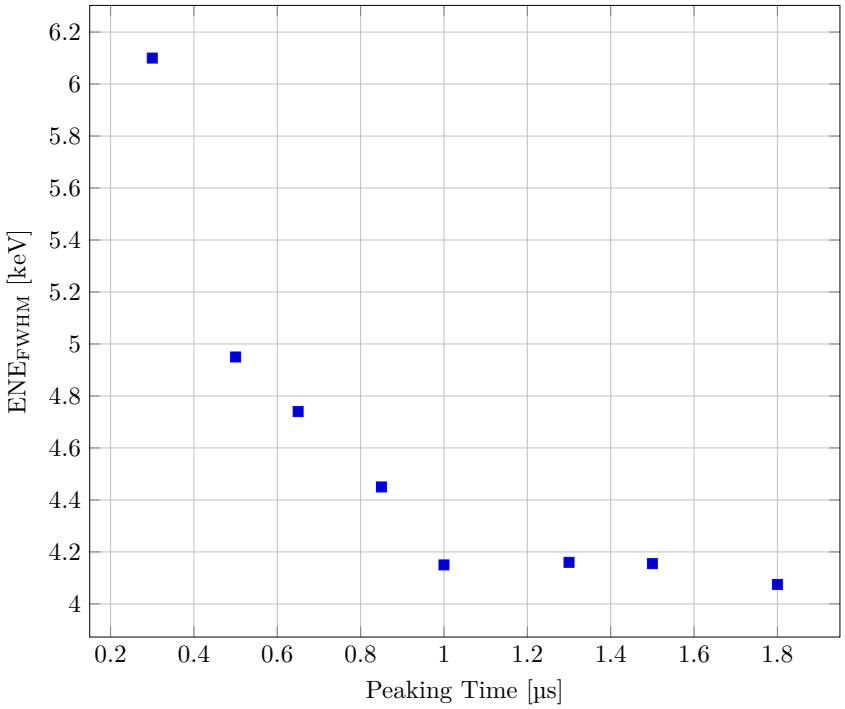

Figure 2.11: channel 3 ENE as a function of the peaking time.

measurements have been carried out for the different available values of peaking times. In order to obtain the ENE, no charge has been injected in the channel and the rms value of the output, $V_{out,rms}$, has been acquired. The ENE can be calculated as:

$$\text{ENE} = \frac{V_{out,rms}}{\mu_c} \tag{2.3}$$

where μ_c is the gain of the channel at very low energy (near 0 keV). The value of the gain is obtained by performing an input-output channel trans-characteristic measurement (like the one obtained for the CSA) of the Shaper block. Results are shown in fig. 2.11. The value of the ENE FWHM is obtained by multiplying the ENE rms value by 2.355.

In general, the ENE value is the sum of three contributions:

$$\text{ENE}^2 = \alpha \cdot \frac{1}{\tau_p} + \beta + \gamma \cdot \tau_p \tag{2.4}$$

where τ_p is the peaking time. The first two terms depend on the white and 1/f noise components in the front-end electronics and the detector capacitance C_D, whereas the third depends only on the parallel noise due to the leakage current of the sensor. As shown in fig. 2.11, the first two contributions are clearly visible (a straight line with negative slope and a horizontal line). There is no peaking time proportional contribution because the Si(Li) detector was not used during the tests.

The noise is higher than the 4 keV requirement of the project. This problem is caused by the chip temperature which was very high due to the problem explained at the beginning of this subsection.

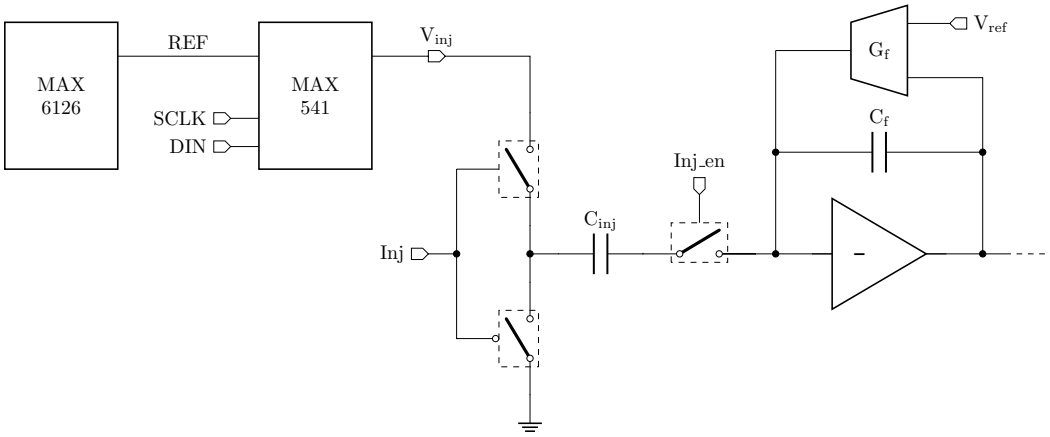

Figure 2.12: injection circuit used to test the GAPS front-end channel.

2.2 SLIDER8: mixed-signal readout processor with 8 channels and digital back-end

SLIDER8 (SiLI DEtector Readout 8), including 8 processing channels, is the first step towards the final ASIC. In this prototype, it is not possible to obtain the output of the analog blocks inside the channels. In fact, the main difference between SLIDER4 and SLIDER8, is the addition of the digital back-end. The ADC takes care of sampling the voltage stored in the sample & hold. Moreover, the digital back-end permits to generate control signals and reference voltages, by setting specific registers, as will be described in section 2.2.2.

Some changes have been done to the injection circuit, too, in order to be able to make it work with the digital back-end. The SLIDER8 injection circuit is described in section 2.2.1.

The experimental results of this prototype, which are described in section 2.2.5, are very promising. However, due to an error in the ADC design, only half of its dynamic range could be used in the measurements. The issue has been fixed in the subsequent prototype, pSLIDER32.

2.2.1 Injection circuit

An injection circuit, similar to the SLIDER4 one, has been designed for SLIDER8. The main difference with respect to SLIDER4 is the solution adopted to provide the injection voltage, as shown in fig. 2.12. In fact, the voltage V_{inj} is not set by an external source, but directly by components placed on the test board and programmed by the digital back-end section of the ASIC.

The two components used to provide the injection voltage are:

- Maxim MAX6126A25+: an ultra-high-precision, ultra lo-low-noise, series voltage reference which generates a constant voltage $REF = 2.5\,\mathrm{V}$.
- Maxim MAX541AESA: a 16-bit DAC programmable through by Serial Peripheral Interface (SPI). This component is connected to the digital back-end, which takes care of its programming. The output, V_{inj}, can vary from 0 V to *REF* (the output of

the MAX6126) with a resolution of

$$V_{inj,lsb} = \frac{2.5\,\mathrm{V}}{2^{16}-1} = 38.15\,\mu\mathrm{V}. \tag{2.5}$$

All the other parts of the injection circuit are placed inside each channel of the ASIC, as in the SLIDER4 case.

Since the 890 fF injection capacitor value is known, it is possible to calculate the LSB value and the maximum value of the injected charge. Following the same considerations already described for the SLIDER4 injection circuit (section 2.1.1) it can be obtained that:

$$Q_{inj,lsb} = 0.033\,95\,\mathrm{fC}\ (0.7716\,\mathrm{keV}),$$
$$Q_{inj,max} = 2.225\,\mathrm{pC}\ (50.568\,\mathrm{MeV}).$$

Since the ASIC bias voltage is 1.8 V, it is critical to avoid applying voltages much larger than the maximum allowed by the technology. Moreover, if the applied voltage exceeds the ASIC bias by more than 600 mV, protection diodes turn on. Therefore, the maximum injection voltage has been limited and the actual or achievable maximum value of the injected charge is:

$$Q_{inj,l\_max} = 1.823\,\mathrm{pC}\ (41.425\,\mathrm{MeV}).$$

The working temperature of the MAX541AESA and the MAX6126A25+ ranges from −40 °C to 100 °C, which are consistent with the temperature at which the ASIC will be tested.

2.2.2 SLIDER8 digital back-end

The SLIDER8 ASIC hosts a digital back-end which is responsible for the ASIC slow control setting and for generating control signals and read data at the output of the S&H. All registers are set to 0 by default. The main registers are:

- Operating Mode register, mainly composed by two bits:
  - Self-Trigger bit (S), used to enable Self-Trigger mode (0: disabled, 1: enabled). These two operating modes are described in section 2.2.3.
  - Acquisition mode bit (A), used to enable full-readout mode:
    - 0, zero suppression: the output of a channel, sampled by the ADC, can be read with the dedicated read procedure, only if the SOT comparator output of that channel is 1 (namely, if the shaper output is higher than the threshold ΔV_t)
    - 1, full-read out: the output of all channels can be read using the dedicated read procedure (even if the comparator output of some channels is 0).
- Shaper Time Constant (TTT), 3-bit used to set the shaper peaking time.
- Global Bias Adjustment (BBB): 3-bit used to set the 3-bit DAC described in section 1.1.5.
- Calibration Voltage (CAL_Voltage): 16-bit register used to set the charge to inject in all channels. The digital back-end takes care of the generation of the SCLK and MOSI (SDI) signals, which are used to set the MAX541 of the injection circuit, described

previously in section 2.1.1. From here on, the value of MAX541 output, V_{inj}, will be expressed in Calibration Voltage DAC codes. As explained before, in SLIDER8 case, each DAC code is equivalent to:

$$1\,\text{DAC code} = Q_{inj,lsb} = 0.033\,95\,\text{fC}\ (0.7716\,\text{keV})$$

- Calibration Mask: 8-bit register used to select the channels where the charge will be injected. Each bit is associated to an *inj_en* switch of one channel. The least significant bit corresponds to channel 0, the most significant bit to channel 7.
- Discriminator Enable Mask: 8-bit register used to select the channels where the charge will be read. The structure of this register is the same of the Calibration Mask.
- Event Data: eight 11-bit registers, each one associated to one channel, where the sample & hold output, digitized by the ADC, is saved.

The commands used to set and read the registers of SLIDER8 digital back-end are listed in table 2.4. The bits expressed as xxx can be either 0 or 1. Each write command has its read counterpart (for example the WRITE OPERATING MODE counterpart is READ OPERATING MODE). The only exceptions are given by the Calibration Voltage register and the read event data command. Since the Calibration Voltage register takes care of programming the MAX541 DAC, which is located outside the ASIC, the read procedure of this external DAC was not implemented directly in the ASIC.

COMMAND NAME	COMMAND CODE	INPUT DATA	OUTPUT DATA
READ EVENT DATA	00000xxx	-	Event Data Packet
READ OPERATING MODE	00010xxx	-	000000SA
READ SHAPER TIME CONSTANT	00011xxx	-	00000TTT
READ GLOBAL BIAS ADJUSTMENT	00101xxx	-	00000BBB
READ DISCRIMINATOR ENABLE MASK	01000xxx	-	8 bit word
READ CALIBRATION MASK	01001xxx	-	8 bit word
WRITE OPERATING MODE	10010xSA	-	-
WRITE SHAPER TIME CONSTANT	10011TTT	-	-
WRITE GLOBAL BIAS ADJUSTMENT	10101xxx	00000BBB	-
SET CALIBRATION DAC VOLTAGE	10110xxx	16 bit word	-
WRITE DISCRIMINATOR ENABLE MASK	11000xxx	8 bit word	-
WRITE CALIBRATION MASK	11001xxx	8 bit word	-

Table 2.4: reading and writing messages format of SLIDER8 digital back-end.

The output of each channel is read using the READ EVENT DATA command. If the ASIC is set in zero suppression mode, the digital back-end creates a single packet for each channel whose comparator has the output at logic 1. On the other hand, if the ASIC is set in full-read out, the digital back-end creates a data packet for all the channels. The structure of this packet is shown in fig. 2.13.

T_0	T_1	WORD TYPE	Description
0	0	Intermediate Word	When the digital back-end prepares n data packets, the first $n-1$ data packets have $T_0T_1 = \texttt{00}$. For each data packet, this means that the digital back-end has prepared a data packet to send with SPI but other data packets are ready to be sent, too.
0	1	Event Error	If the channel output has not been correctly sampled or stored in the corresponding register, the digital back-end prepares this type of message.
1	0	Last Word	When the digital back-end prepares n data packets, the last packets have $T_0T_1 = \texttt{10}$. This means that the other $n-1$ packets have been correctly sent with the SPI and this type of message identifies the last packet to be sent.
1	1	Empty Event	After the receipt of the "last word" message, if the user requires other packets (namely it sends another read event data command), the digital back-end will answer with an empty event message. Also in case that no channels have stored the sample & hold output in the corresponding register (for example, in zero suppression mode, the threshold is very high and injected charge is too low) the digital back-end will answer with an empty event message.

Table 2.5: Structure of the first 2 bits of the Read Event Data Packet

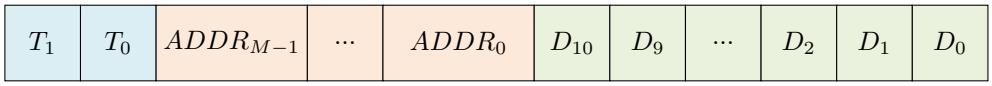

Figure 2.13: SLIDER8 read event data packet.

The event data packet is divided in 3 parts:

- T_1T_0, the two most significant bits of the read event data message, identify the type of the message, as described in table 2.5.

- $ADDR_{M-1} \ldots ADDR_0$, where $M = \log_2(N_C)$ and N_C is the number of the channels. These bits identify the channel corresponding to that data packet. In the "Event Error" case all these bits are set to 0, whereas in the "Empty Event" case they are set to 1.

- $D_{10} \ldots D_0$, represent the digitized output of the sample & hold of the channel specified in the *ADDR* bits. As for the previous bits, in the "Event Error" case all these bits are set to 0, whereas in the "Empty Event" case they are set to 1.

When the digital back-end receives a read event data command, it prepares all the packets. These are sent with the MISO (SDO) signal of the SPI protocol. Only one read

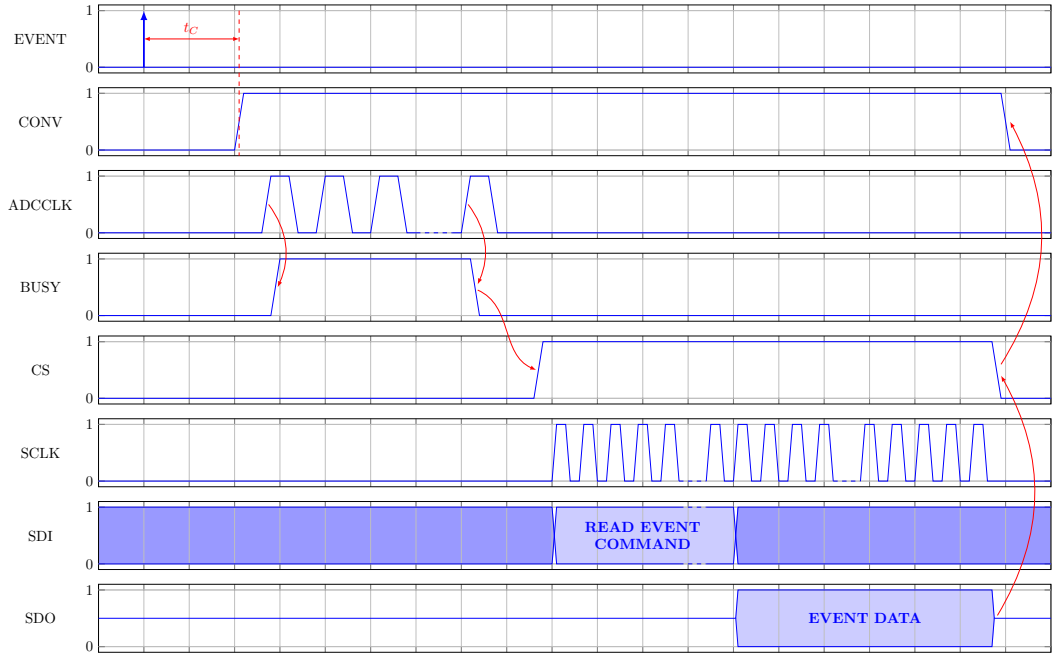

Figure 2.14: SLIDER8 non-self-trigger injection and read procedure.

event command is needed even if the digital back-end has prepared more than one data packet (namely more channels have the comparator output at logic 1 or the full read out mode is activated). In order to correctly communicate with the digital back-end, the user must provide a specific number of SPI clock hits:

$$\#SCLK = 8 + (16 \cdot N_h)\,. \tag{2.6}$$

where N_h is the number of data packets that the digital back-end has prepared to be sent. The first eight clock hits are required to send the read event data command, while the other $(16 \cdot N_h)$ are required to send the N_h data packet prepared.

2.2.3 Non-self-trigger and self-trigger mode

GAPS front-end can work in two different ways: non-self-trigger and self-trigger modes. The main difference between the two modes is related with the way the sampling signal of the sample & hold is generated. Moreover, the order of the signals which have to be send to the ASIC is slightly different. By default the ASIC works in non-self-trigger mode, but, by setting the specific register, it can be changed to self-trigger mode. All the registers described in section 2.2.2 must be set before the charge injection.

Non-self-trigger mode

In this mode the user can select the sampling time of the shaper output and store it in the sample & hold. The time diagrams of all the signals are shown in fig. 2.14. Here follows a short description of the signals (and their order) used in non self-trigger mode.

- *INJECT* (*Inj*), input signal, normally at logic 1. This signal operates on the switches of the injection circuit described in section 2.2.1. The transition from logic 1 to logic 0, corresponds to the charge injection.

- *CONV*, input signal, normally at logic 0. At the transition from logic 0 to 1, the shaper output is stored in the sample & hold. This happens since this signal operates directly on the switch of the sample & hold. As can be seen in fig. 2.14, the time between the injection and the sampling of the shaper voltage in the sample & hold is called t_C.

- *ADCCLK*, input signal, normally at logic 0. When the shaper output is stored in the sample & hold, the user must send to the ADC an exact number of clock hits. This clock is used by the ADC in order to digitize the voltage stored in the sample & hold. For each channel, the ADC needs: 3 clock hits to sample the signal without having settling problems with higher clock frequencies, 11 clock hits to digitize the S&H output and 1 clock hit to save the digitized value in the register. Moreover, other 15 clock hits are needed to digitize the temperature sensor output (even if the temperature sensor is not integrated in SLIDER8 board, this feature has been integrated for the later versions of the ASIC). The number of ADCCLK hits needed are:

  $$\#ADCCLK = N_h \cdot 15 + 15 \tag{2.7}$$

  where N_h is the number of channels with their comparator output at logic 1. In case of full read-out mode N_h is always equal to 8. In SLIDER8 case, the maximum number of clock hits is 135.

- *BUSY*, output signal, normally at logic 0. This signal passes from 0 to 1 when the user sends the first hit of ADCCLK. Instead, it passes from 1 to 0 when the ADC ends the sampling procedure. So, this signal gives an information to the user about the sampling procedure.

- *CS*, *SCLK* and *SDI* (*MOSI*), SPI input signals. These signals are used to communicate with the digital back-end through the SPI. All the commands are described in section 2.2.2.

- *SDO* (*MISO*), SPI output signal. This signal is used to communicate with the digital back-end through the SPI.

Self-trigger mode

In this mode, the system gives the user information about the instant when the shaper peaking time occurs. The differences of the signals with respect to the non-self-trigger mode are listed below:

- *BUSY*, output signal, normally at logic 0. This signal passes from logic 0 to 1 when the ZC comparator passes from logic 0 to 1 (the peaking time instant). Instead, like in non-self-trigger mode, it passes from 1 to 0 when the ADC ends the sampling procedure.

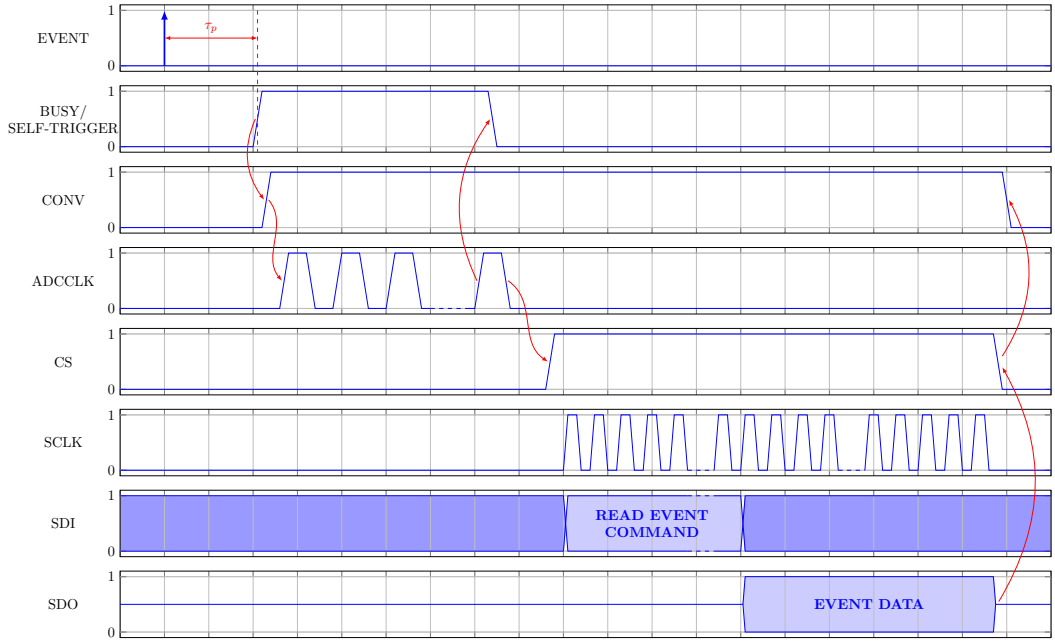

Figure 2.15: SLIDER8 self-trigger injection and read procedure.

- *CONV*, input signal, normally at logic 0. This signal works in the same way of the non-self-trigger mode, but, if the user wants to sample the shaper output at the peaking time, he has to send the CONV signal as fast as possible after receiving the busy signal.

The *inj*, *ADCCLK* and SPI signals work in the same way as the non-self-trigger mode. But the main difference with respect to the non-self-trigger mode is that, if the *BUSY* signal is not high, the shaper output cannot be stored in the sample & hold. All the signals are shown in fig. 2.14.

2.2.4 SLIDER8 test board

A specific test board has been designed in order to characterize the SLIDER8 ASIC. The board is slightly different with respect to the SLIDER4 one, described in section 2.1.2. The main differences are listed below.

- The 2 LEMO connectors used to provide the threshold voltages V_{tp} and V_{tn} have been removed and replaced with two 16-bit DACs. These DACs are the same model as the one used to generate the Calibration Voltage (Maxim MAX541AESA+), already described in section 2.2.1. The SPI signals (two chip select, one MOSI and the SPI clock) must be provided on 4 specific pins which have been placed on the test board.
- The 8 buffers and the 3 test points have been removed since in the SLIDER8 ASIC the analog blocks output are not accessible.
- 2 new connectors have been placed on the test board: the first connector is used to send the signals to the digital back-end, the second connector is used to send the signals to the two DACs which generate V_{tp} and V_{tn}.

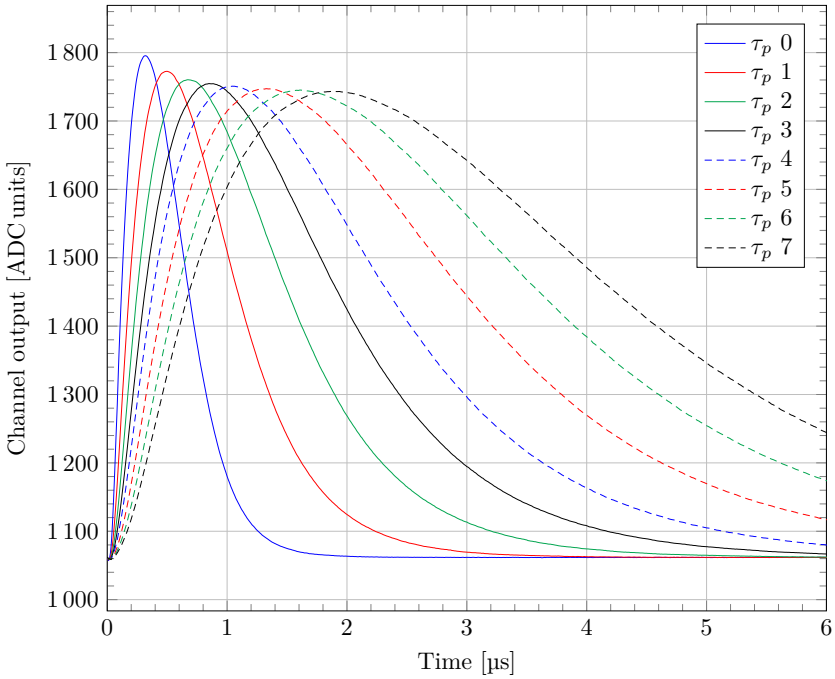

Figure 2.16: SLIDER8 Channel output for channel 1. The injected charge corresponds to an energy signal of 15.43 MeV.

All the other components are the same as for the SLIDER4 case.

2.2.5 Characterization Results

Waveform Scan

With the ASIC operated in non-self-trigger mode and by varying the interval t_C between injection and sampling time, it is possible to reconstruct the entire shaper output time response. The waveform scan represents the shaper output with a gain factor of 3.23 of the sample & hold. In figures 2.16 and 2.17, the sample & hold output of channels 1 and 8 is shown. The calibration voltage is set to 20000 DAC units, which corresponds to an injected charge of 679 fC (15.43 MeV). The amplitude of the time response at the peak decreases with the increase of the peaking time, due to the zero in the input-output transfer function of the charge sensitive amplifier.

In table 2.6, the nominal and the measured value of the peaking time are compared. The values of the measured peaking times are very close to the simulated ones. The peaking time values are affected by a very small quantization error introduced by the minimum sampling time, t_C, which is

$$t_{C,min} = \frac{1}{96 \cdot 10^6\,\text{MHz}} = 10.4\,\text{ns} \tag{2.8}$$

where 96 MHz is the clock of the microcontroller used during the characterization.

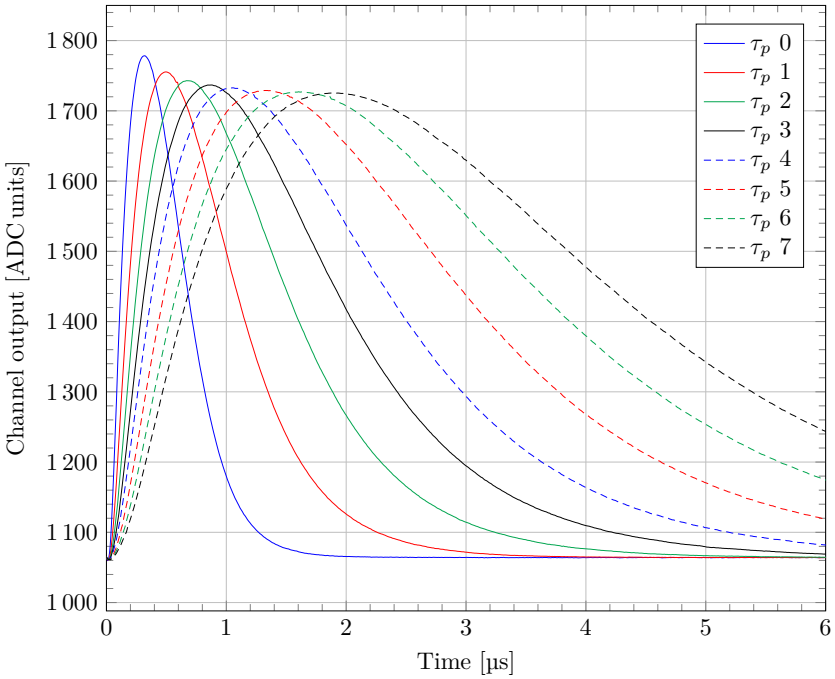

Figure 2.17: SLIDER8 Channel output for channel 8. The injected charge corresponds to an energy signal of 15.43 MeV.

τ_p	simulated τ_p [µs]	measured τ_p [µs]
0	0.30	0.30
1	0.50	0.47
2	0.65	0.65
3	0.85	0.83
4	1.00	1.00
5	1.30	1.27
6	1.50	1.54
7	1.80	1.82

Table 2.6: Comparison between ideal τ_p and measured τ_p.

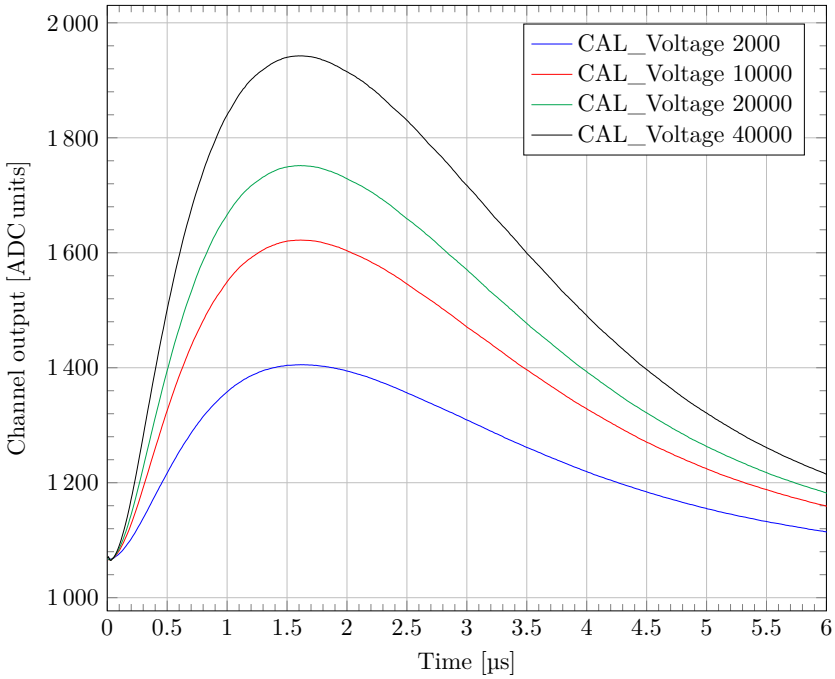

Figure 2.18: SLIDER8 channel output for channel 5 and peaking time 6 as obtained by varying the calibration voltage.

CAL Voltage [DAC units]	measured τ_3 [µs]	measured τ_5 [µs]
2000	0.84	1.27
10000	0.83	1.28
20000	0.83	1.27
40000	0.84	1.26

Table 2.7: measured τ_3 and τ_5 for different values of the injected charge.

In fig. 2.18, the channel output of channel 5, operated at the peaking time 6, is shown for different values of the injected charge. This measurement demonstrates that the channel works properly. The value of the measured peaking times for different injected charge is shown in table 2.7 (only for peaking times 3 and 5). As can be seen in this table, the value of the peaking time is almost independent of the value of the injected charge. The little differences are again caused by the minimum sampling time.

Input-output channel trans-characteristic

The input-output channel trans-characteristic represents the channel output value at the peaking time instant as a function of the injected charge. In fig. 2.19, the input-output channel trans-characteristic of channel 6 for all the peaking times is shown. The injected charge varies from 0 to 30000 DAC units (1.018 pC, 23.15 MeV). It is evident that, by increasing the peaking time, the gain decreases. Moreover, the dynamic signal compression

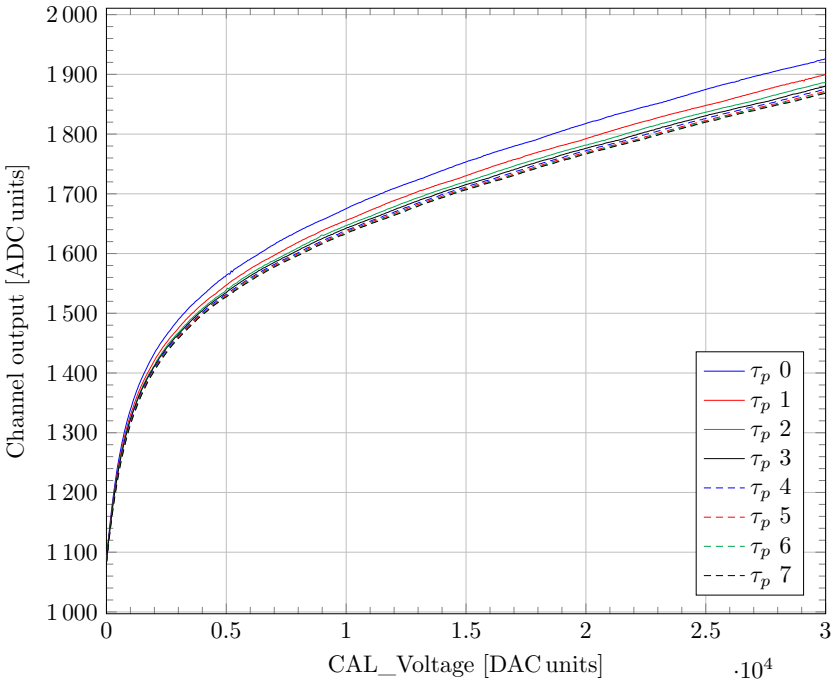

Figure 2.19: SLIDER8 input-output trans-characteristics for channel 6 at all the selectable peaking times. The injected charge varies from 0 to 30000 DAC units (1.018 pC, 23.15 MeV).

is evident, too. In fig. 2.23, the input-output channel trans-characteristic of all channels belonging to the same ASIC for the peaking time 7 is shown.

Finally, in fig. 2.21, the input-output channel trans-characteristic in the low energy region (from 0 to 30.87 keV) is shown for the 8 selectable peaking times. The data obtained from these measurements are fitted using the linear regression in order to obtain the low energy gain. The values provided by the fit are used to calculate the ENE. In table 2.8 the value of the gain is listed.

Threshold scan

The threshold scan gives an information about the electronic noise and the actual threshold of the SOT comparator. The inputs of the SOT comparator are the shaper output and the threshold voltages generated by the threshold circuit. The value of the channel baseline is very similar for all the channels (due to the transconductor work), whereas the voltages generated by the threshold generator are slightly different from one another due to the process parameters and the nature of the threshold generator. In the threshold scans, the bit A of the operating mode register is set to 0. A threshold scan consists in varying the threshold generator output voltages, without injecting charge, and to control if the Signal Over Threshold comparator fires, that is its output, that normally is at logic 0, rises to logic 1. If the SOT comparator fires, then the channel output is sampled. When the comparator threshold is close to the shaper baseline, the SOT comparator does not fire every time: the

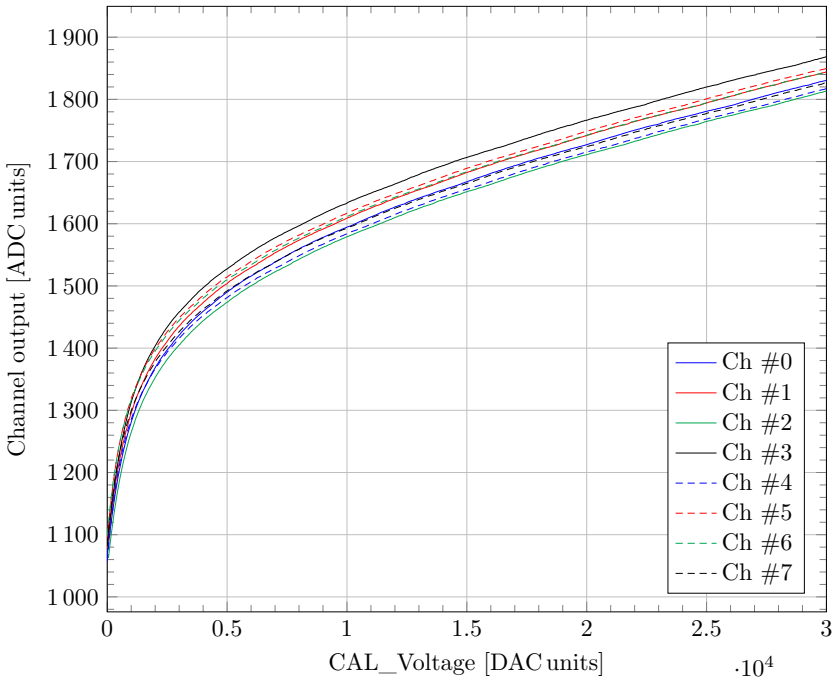

Figure 2.20: SLIDER8 input-output trans-characteristics for all the channels and peaking time 7. The injected charge varies from 0 to 30000 DAC units (1.018 pC, 23.15 MeV).

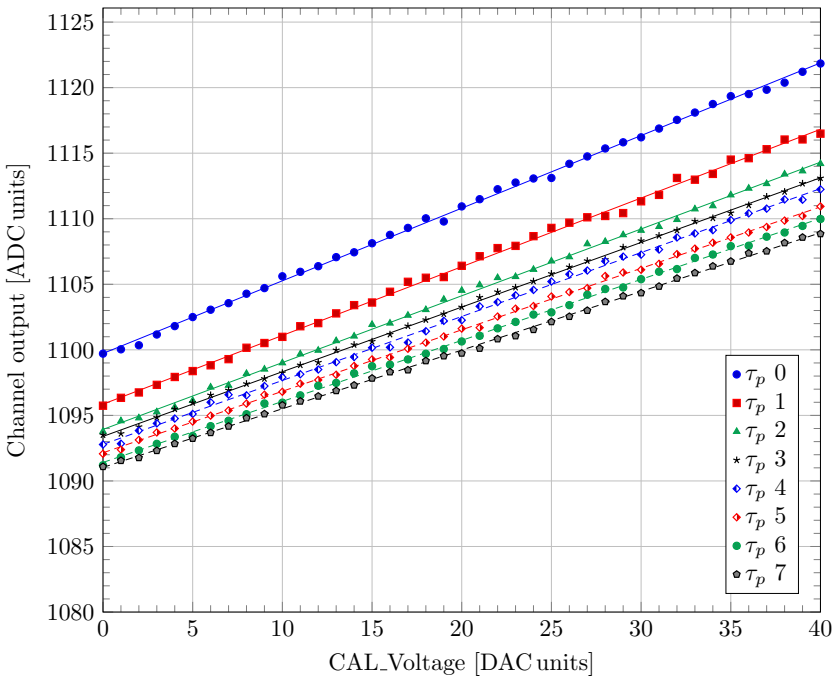

Figure 2.21: SLIDER8 low energy gain for channel 5 at all the selectable peaking times.

τ_p	Gain $\left[\frac{\text{ADC u}}{\text{DAC u}}\right]$
0	0.554
1	0.524
2	0.510
3	0.493
4	0.488
5	0.469
6	0.466
7	0.447

Table 2.8: SLIDER8 low energy region gain for all the selectable peaking times.

τ_p	Threshold [DAC u]	Noise [DAC u]
0	301	28.9
1	299	23.8
2	298	25.3
3	299	21.3
4	298	19.9
5	300	18.3
6	300	18.9
7	298	17.8

Table 2.9: fit values obtained by fitting the data values for channel 4.

number of hits in this range provides information about the channel noise. A threshold scan was performed, by varying the value of the voltage V_{tp} at the threshold generator input and keeping the value of the voltage V_{tn} at 0 V. Since the channel threshold is given by the difference $V_{tp} - V_{tn}$, by increasing the value of V_{tp} the channel threshold increases. The threshold scans shown in the next figures are obtained by fitting the experimental data using the function:

$$f(x) = 50 - 50 \cdot erf\frac{x-a}{\sqrt{2}\cdot b} \tag{2.9}$$

where erf is the error function

$$erf(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}dt, \tag{2.10}$$

a is the channel comparator threshold and b is the standard deviation of the noise. a and b are expressed in DAC codes.

In fig. 2.22 a threshold scan of the channel for the 8 selectable peaking times is shown. The extracted threshold and the standard deviation of the noise are listed in table 2.9. As expected, the value of the standard deviation increases for the lower peaking times. This effect is related to the contribution from the series noise, which is proportional to the inverse of the peaking time as shown in eq. (2.4). Instead, the value of the extracted threshold remains constant for each peaking time.

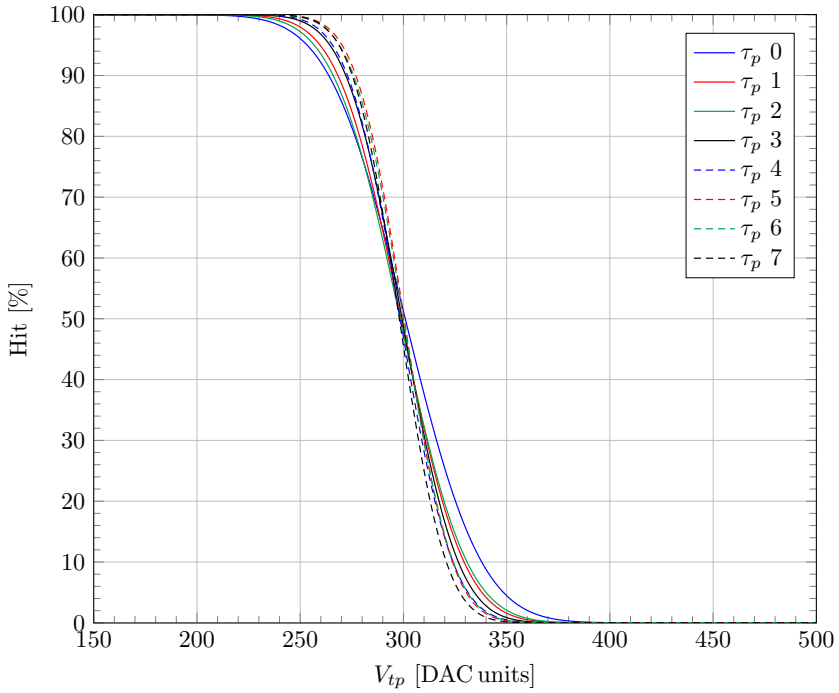

Figure 2.22: SLIDER8 threshold scan of the channel 4 as obtained by varying the peaking time.

In fig. 2.23, a threshold scan for all the channels and the peaking time 3 is shown. In table 2.10, the extracted threshold and the standard deviation of the noise are listed. As expected, the threshold changes from channel to channel. However, the threshold dispersion is higher than expected. Its value is 246.22 DAC units, which corresponds to 9.39 mV (186.9 keV). To comply with this large dispersion, in the subsequent version of the ASIC (pSLIDER32), a 3-bit DAC for threshold fine trimming has been included in each channel.

Channel	Threshold [DAC u]	Noise [DAC u]
0	440	15.9
1	634	15.7
2	107	15.3
3	667	16.5
4	299	21.3
5	695	22.2
6	879	21.0
7	610	19.2

Table 2.10: fit values obtained with peaking time 3.

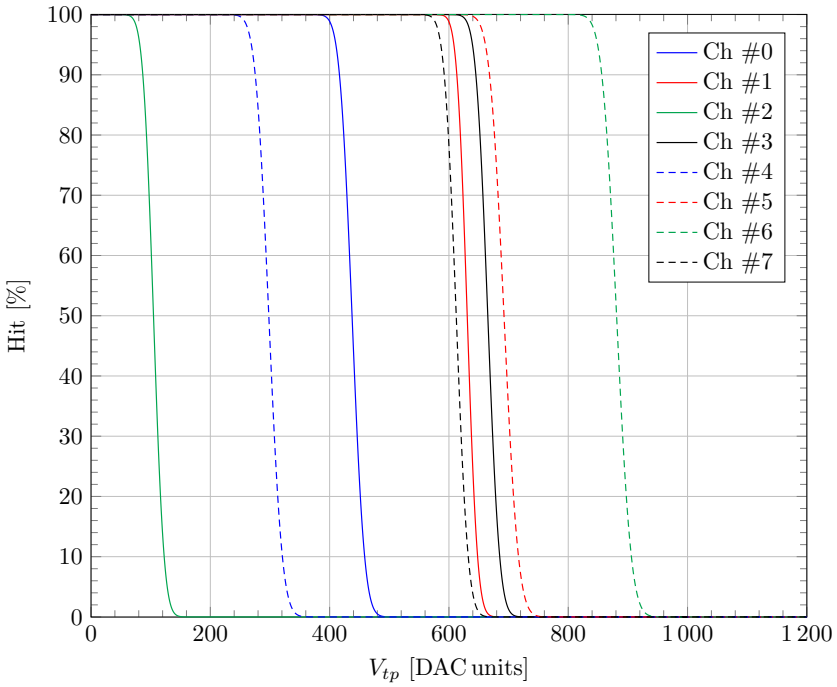

Figure 2.23: SLIDER8 threshold scan for all the channels and peaking time 3.

Equivalent Noise Energy

Starting from the threshold scan and input-output trans-characteristic, the Equivalent Noise Energy (ENE) of the SLIDER8 ASIC has been evaluated by means of the following equation

$$ENE\left[\frac{\text{DAC units}}{\frac{\text{ADC units}}{\text{DAC units}}}\right] = \frac{b\,[\text{DAC unit}]}{G_{n,S\&H}\left[\frac{\text{ADC units}}{\text{DAC units}}\right]}, \tag{2.11}$$

where

- b is the noise obtained in the threshold scan measurements.
- $G_{n,S\&H}$ is the gain, in the low energy region, obtained from the input-output trans-characteristic, at the channel output.

In order to obtain the ENE, expressed in keV:

- the value of b must be expressed in V:

$$b\,[\text{V}] = b\,[\text{DAC units}] \cdot \frac{2.5}{2^{16}}\left[\frac{\text{V}}{\text{DAC units}}\right] \tag{2.12}$$

  where:

  - 2.5 V is the voltage reference of the 16-bit injection DAC described in section 2.2.1.
  - $\frac{2.5}{2^{16}}\left[\frac{\text{V}}{\text{DAC units}}\right] = 38.15\left[\frac{\mu\text{V}}{\text{DAC units}}\right]$.

- the value of $G_{n,S\&H}$ must be expressed in V/keV:

$$G_{n,S\&H}\left[\frac{\text{V}}{\text{keV}}\right] = G_{n,S\&H}\left[\frac{\text{ADC units}}{\text{DAC units}}\right] \cdot \frac{\frac{2 \cdot 1.8}{2^{11}}\left[\frac{\text{V}}{\text{ADC units}}\right]}{k_D\left[\frac{\text{keV}}{\text{DAC units}}\right]} \tag{2.13}$$

  where:

  – 1.8 V is the supply voltage of the 11-bit ADC of the channel. Because of the differential nature of the ADC, the value of the maximum voltage range of the ADC input is multiplied by 2, therefore obtaining:

$$\frac{2 \cdot 1.8}{2^{11}}\left[\frac{\text{V}}{\text{ADC units}}\right] = 1.758\left[\frac{\text{mV}}{\text{ADC units}}\right] \tag{2.14}$$

  – The conversion factor DAC units-keV can be found using the capacitance equation and the conversion factor C-keV already found in section 2.1.1:

$$k_D\left[\frac{\text{keV}}{\text{DAC units}}\right] = \frac{C_{inj}[\text{fF}] \cdot 38.15\left[\frac{\mu\text{V}}{\text{DAC units}}\right]}{0.044\left[\frac{\text{fC}}{\text{keV}}\right]} \tag{2.15}$$

  Moreover, the value of the gain must be divided by the sample & hold gain, which is 3.23 [V/V], because the threshold detector is directly connected to the shaper output (whereas the gain $G_{n,S\&H}$ is expressed using the units of the ADC connected after the sample & hold). The value of the shaper Gain can be obtained as:

$$G_{n,sh} = \frac{G_{n,S\&H}}{3.23} \tag{2.16}$$

- Finally, the FWHM value of the ENE is found by multiplying the noise, b, by 2.35 and dividing it by the channel gain at low energy.

$$ENE_{FWHM}[\text{keV}] = 2.35 \cdot \frac{b[\text{V}]}{G_{n,sh}\left[\frac{\text{V}}{\text{keV}}\right]}. \tag{2.17}$$

The mean value of the ENE, averaged over the 8 channels, for all the peaking times, is shown in fig. 2.24. The results show that the noise at room temperature is higher than expected. After a thorough analysis of the circuit and the technology, it has been found that the excess noise can be ascribed to the following effects:

- a parasitic resistance in series to the CSA input in the SLIDER8 layout which is higher than the simulated one. This problem has been eliminated in pSLIDER32 layout.

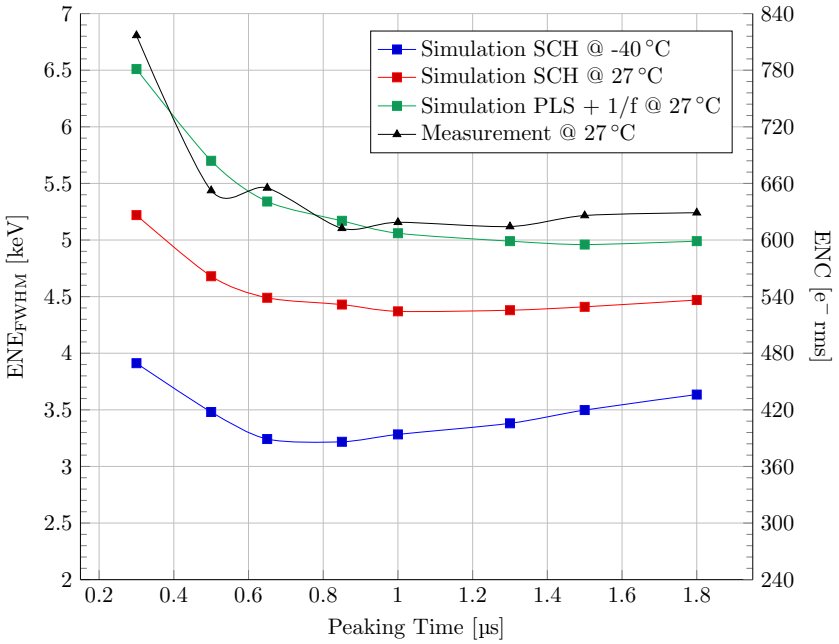

Figure 2.24: mean SLIDER8 ENE.

- According to measurements performed on a single MOS device, flicker noise coefficient is larger than in the model provided by the technology.

Considering the measured flicker noise and the series gate resistance in the input device, FWHM is in agreement with simulation results. Moreover, the ENE is found to be in agreement with eq. (2.4), described in SLIDER4 section. However, the ENE is larger than the 4 keV specification set for the readout channel.

3 Characterization of the 32 channels prototype of the flight ASIC for the readout of the GAPS Si(Li) tracker

In this chapter the last prototype, pSLIDER32 (prototype SiLI DEtector Readout 32), developed before the production of the final ASIC, is described.

3.1 pSLIDER32 architecture

pSLIDER32 is the last prototype that has been produced before the construction of the final chip. This version is composed of all the 32 channels. In fig. 3.1 pSLIDER32 layout is shown. As depicted in the figure, the circuit dimension is 3.14×3.14 mm^2.

With respect to SLIDER8, the blocks and features described in the following have been introduced:

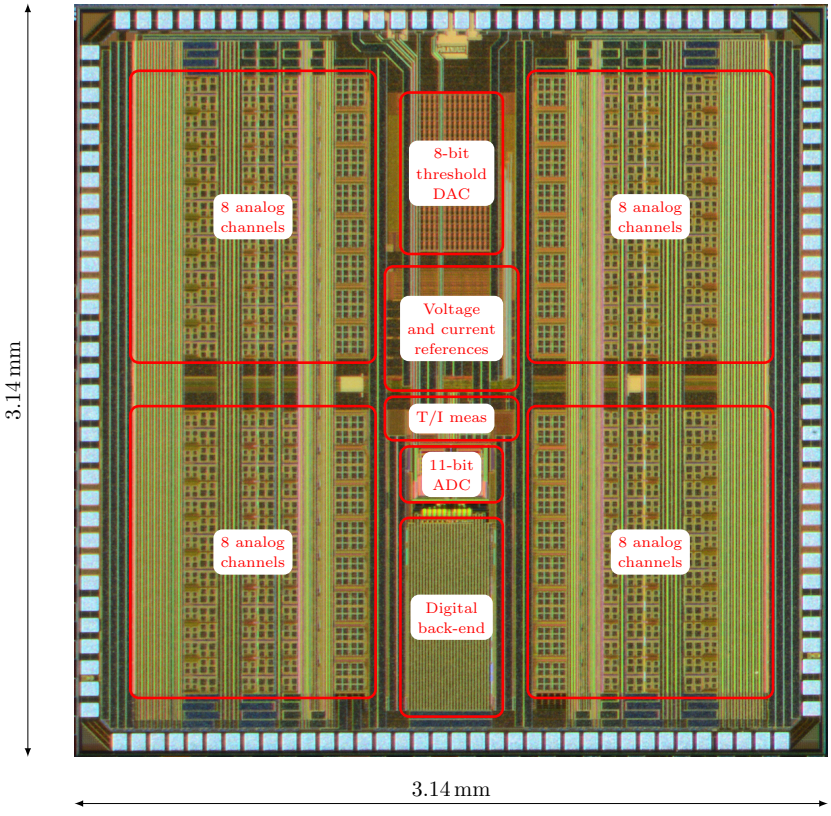

Figure 3.1: pSLIDER32 layout.

- An 8-bit threshold DAC (described in section 1.2.1) used for the generation of the voltages V_{tp} and V_{tn}. The threshold generator uses these two voltages in order to generate the differential threshold voltage (V_{th} in fig. B.37) needed by the SOT comparator. This block is located in the high part of the layout. With respect to the use of an external discrete commercial component, the main advantages of this integrated solution are:
  - lower power consumption.
  - All the components are located on the ASIC and, consequently, there will be fewer components on the front-end board.
  - Adequate LSB value of the generated threshold, even if the bits of the DAC is reduced from 16 (in SLIDER8 case) to 8.
- A 3-bit fine-trimming DAC located in each channel. This block is used for the fine trimming of the SOT comparator threshold, whose variations are caused by process parameters.
- A detector leakage current readout and a temperature sensor readout. These parts are located in the center of the layout in the T/I meas block. A more detailed description will be given in section 3.1.1.
- Channel 0 and channel 31 have all the analog block outputs externally accessible for testing purposes.

Each side of the pSLIDER32 ASIC is composed of 32 pads, for a total of 128 pads. All the pads are connected to the package pins by wire-bonding. In fig. 3.2 the pSLIDER32 package pin diagram is shown. As can be seen in the figure, the pins can be grouped into four families:

- Channel Inputs. These 32 pins are connected to the CSA input of each channel. In the final experiment, each one of these pins will be connected to a different strip of the detector.
- Analog Outputs. 16 pins connected to the outputs of the analog blocks of the channels 0 and 31. In particular the accessible blocks are: the Charge Sensitive Amplifier (CSA), the Integrator (INT) (first part of the Shaper), the Shaper (SHAP), the Differentiator (DIFF), the Zero Crossing comparator (ZC), the Signal Over Threshold comparator (SOT), and sample & hold (CHP and CHM) outputs.
- Digital I/O. 37 pins are used by the digital section. In particular:
  - 10 pins are used for the digital supply voltage (DVDD, DGND, DVDD/IO,DGND/IO, DVDD/IO_3.3V, DGND/IO_3.3V)
  - 12 pins are used for the SPI communication between the ASIC and the external user (SCLK, SDI, SDO, CSEL<0>, CSEL<1>, CSEL<2> and all their inverted polarity signals).
  - 8 pins are used for the injection procedure described in SLIDER8 section 2.2.3 (INJECT, CONVABORTN (CONV), ADCCLK, BUSY and all their inverted polarity signals)

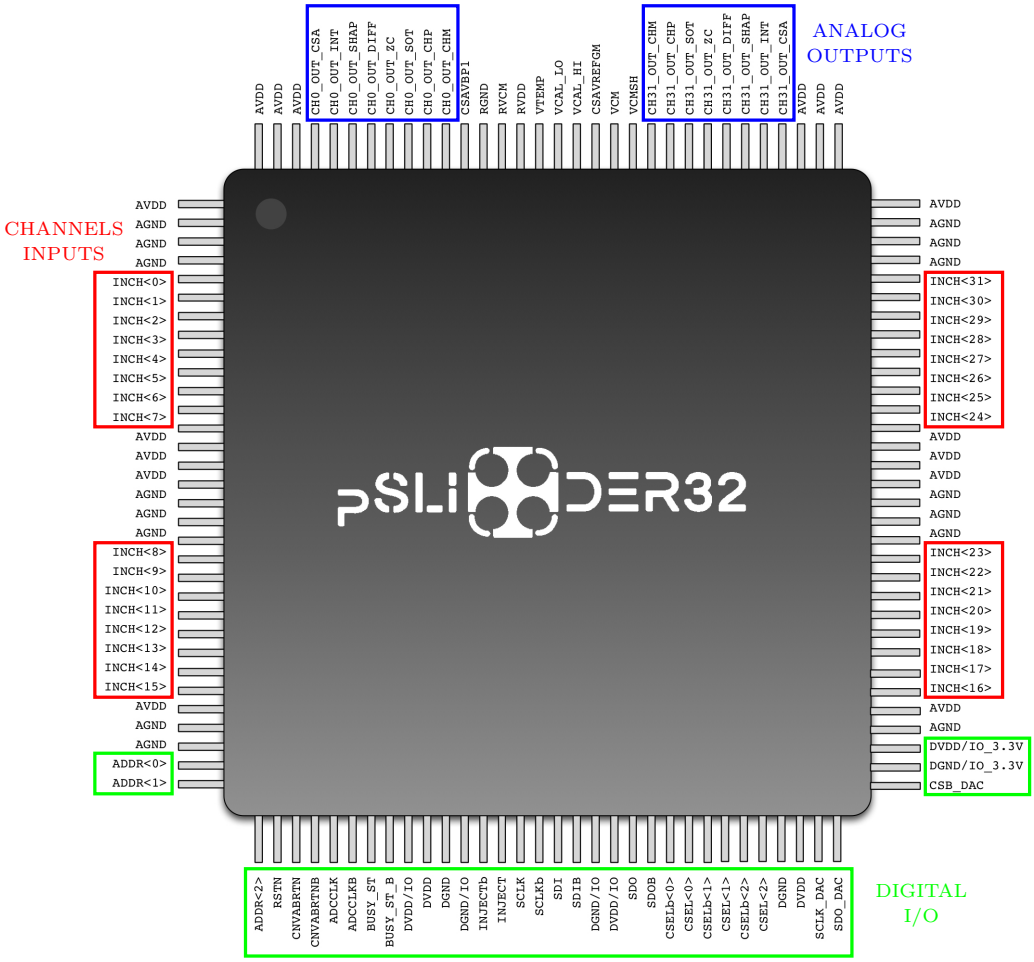

Figure 3.2: pSLIDER32 pin diagram.

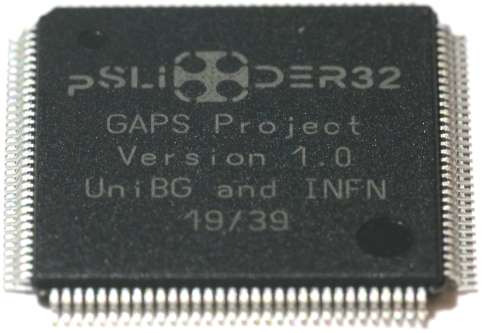

Figure 3.3: pSLIDER32 package.

  - 3 pins are used to set the address (ADDR<0>, ADDR<1> and ADDR<2>) of the ASIC: if the user want to communicate with the ASIC, the SPI CSEL signals must be equal to their corresponding ADDR signals.
  - 3 pins are used for the SPI communication between the ASIC and the 16-bit DAC of the injection circuit (SCLK_DAC, SDI_DAC and CSB_DAC).
  - the last pin is used by the reset signal (RSTN) whose purpose is to restore the Digital Back-end register to the default values.
- All the other pins are used for the analog supply voltage (AVDD and AGND) and for voltage references of the analog blocks.

In fig. 3.3 the pSLIDER32 package is shown. It consists in a plastic thin quad flat pack (TQFP128) with an area of 14×14 mm^2 and a pitch of 0.4 mm.

3.1.1 Temperature sensor and detector leakage current readout circuit

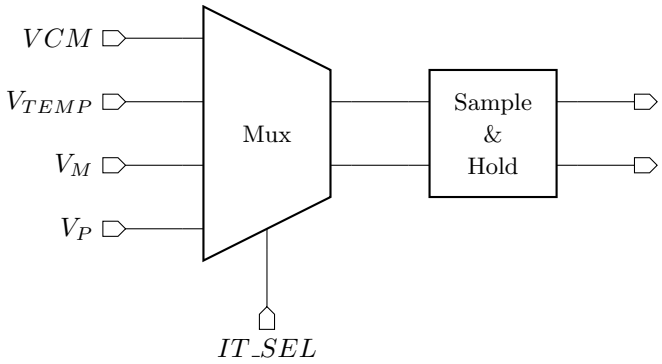

Figure 3.4: pSLIDER32 Multiplexer.

In pSLIDER32 a peripheral block has been introduced with the main purpose of digitize two different quantities:

- The operating temperature using a temperature sensor, external to the ASIC.

- The detector leakage current using the circuit shown in fig. 3.5, placed inside the ASIC.

The multiplexer, shown in fig. 3.4, permits to select the voltage to be stored in the sample & hold and digitized with the 11-bit ADC. If the signal IT_SEL is set to 1, the multiplexer selects the voltages of the leakage currents (V_P and V_M), otherwise the voltage $VTEMP$, obtained by the temperature sensor, and VCM (fixed at 0.9 V).

Temperature sensor

The temperature sensor chosen for the pSLIDER32 test board is the Texas Instruments LMT84. The approximated value of the output voltage of the LMT84 (V_T), as a function of temperature, is:

$$V_T[\mathrm{mV}] = 870.6\,\mathrm{mV} - \left[5.506\,\frac{\mathrm{mV}}{^\circ\mathrm{C}} \cdot (T - 30\,^\circ\mathrm{C})\right] - \left[0.001\,76\,\frac{\mathrm{mV}}{^\circ\mathrm{C}^2} \cdot (T - 30\,^\circ\mathrm{C})^2\right]. \quad (3.1)$$

From this equation the temperature T can be obtained (expressed in °C):

$$T[^\circ\mathrm{C}] = 30 + \frac{5.506 - \sqrt{(-5.506)^2 + 4 \cdot 0.00176 \cdot (870.6 - V_T\,[\mathrm{mV}])}}{2 \cdot (-0.00176)} \quad (3.2)$$

The differential sample & hold shown in fig. 3.4 introduces a gain factor of 5.14 whereas $V_{CM} = 0.9\,\mathrm{V}$. The value of the sample & hold output is

$$V_o = G_{S\&H} \cdot (V_{CM} - V_T)\,, \quad (3.3)$$

so

$$V_T = V_{CM} - \frac{V_T}{G_{S\&H}} = 0.9\,\mathrm{V} - \frac{(ADC\_code - 1024) \cdot 1.76\,\mathrm{mV}}{5.14} \quad (3.4)$$

where *ADC_code* is the sample & hold output digitized by the ADC and 1.76 mV is the lsb value of the ADC, expressed in mV.

Detector leakage current measurement circuit

The PMOS structure, highlighted in fig. 3.5, is replicated in each channel and connected to the buses MonBusP and MonBusN. The current which flows in the MOS P0 and P1 are:

- i^* (P0) which is mirrored from another branch of the circuit where the current is known and fixed (i_k). In fact, such a current is generated to supply the Krummenacher feedback circuit. Moreover, the current mirror introduces a current gain factor of 10, obtaining:
$$i^* = 10 \cdot i_k \quad (3.5)$$
- i_{leak} (P1) which is mirrored from the branch of the Krummenacher circuit used to compensate the detector leakage current (i_{krum}). The main characteristic of this current is that it is the sum of the current i_k and the current i_{det}, which is the leakage current coming from the detector. So:
$$i_{krum} = i_k + i_{det}. \quad (3.6)$$
In P1 current mirror the gain factor is 10, too, so i_{leak} can be expressed as:
$$i_{leak} = 10 \cdot i_{krum} = 10 \cdot (i_k + i_{det}) = i^* + 10 \cdot i_{det} \quad (3.7)$$

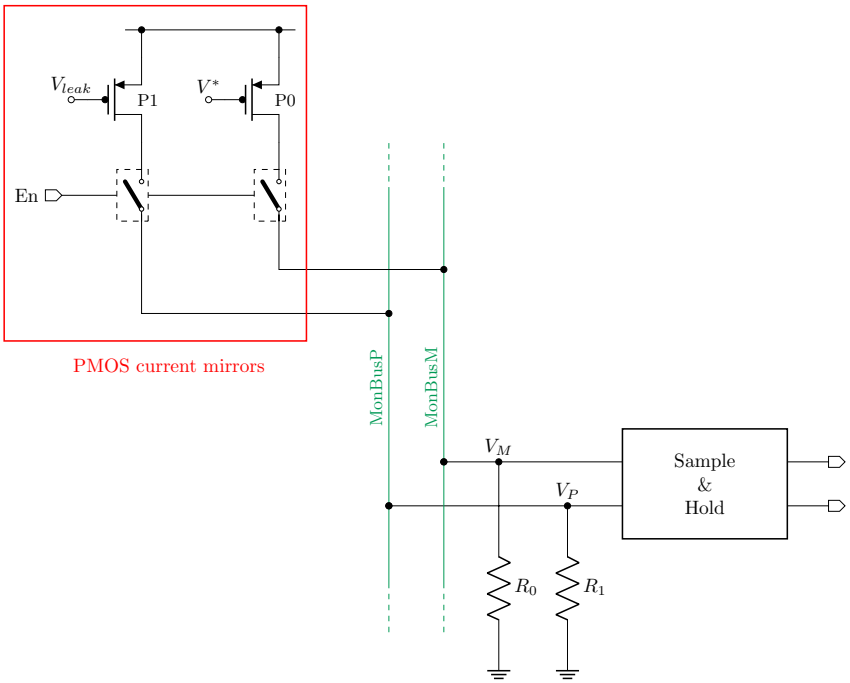

Figure 3.5: pSLIDER32 Leakage Current Detector.

The switches controlled by the signal *En* permit to select the channels from which the leakage currents will be read. The Leakage Current Mask register takes care of generating the 32 *En* signals, one for each channel. The sum of the currents of the channels selected, flow directly in the buses MonBusP and MonBusM. So:

$$i_{leak,tot} = \sum_{i=0}^{31} i_{leak,i} = \sum_{i=0}^{31} i_i^* + 10 \cdot \sum_{i=0}^{31} i_{det,i} \tag{3.8}$$

$$i_{tot}^* = \sum_{i=0}^{31} i_i^* \tag{3.9}$$

where $i_{leak,tot}$ flows in the bus MonBusP and finally in the resistor R_1, obtaining $V_P = i_{leak,tot} \cdot R_1$. Otherwise, i_{tot}^* flows in the bus MonBusM, then in the resistor R_0, obtaining $V_M = i_{tot}^* \cdot R_0$. The voltages V_P and V_M are then stored in the sample & hold, which introduces a gain factor of 5.14 for each. Moreover, the resistors R_0 and R_1 are equal. so, the voltage that is sampled by the ADC is:

$$V_{det,tot} = 5.14 \cdot (V_P - V_M) = 5.14 \cdot R_0 \cdot 10 \cdot i_{det,tot}, \tag{3.10}$$

and

$$i_{det,tot} = \frac{V_{det,tot}}{5.14 \cdot 10 \cdot R_0}. \tag{3.11}$$

As in the temperature sensor case, the ADC has a 1.76 mV LSB value and $VCM = 0.9\,\text{V}$. The output of the ADC is expressed in ADC codes, so:

$$V_{det,tot} = [(1024 - ADC\_code) \cdot 1.76\,\text{mV}] \tag{3.12}$$

and, using the eq. (3.11):

$$i_{det,tot} = \frac{[(1024 - ADC\_code) \cdot 1.76\,\text{mV}]}{5.14 \cdot 10 \cdot R_0}. \tag{3.13}$$

3.1.2 Injection circuit

The injection circuit designed to test pSLIDER32 is slightly different from the one used for the SLIDER8 characterization (described in section 2.2.1). The Maxim MAX6126A25+ has been replaced with the Maxim MAX6126AASA21, which generates a constant voltage $REF = 2.048\,\text{V}$. Using this component, all the DAC dynamic range can be used. The 16-bit DAC MAX541AESA, like in the SLIDER8 case, can vary its output voltage from 0 V to *REF* (the MAX6126AASA21 output), and the LSB value is:

$$V_{inj,lsb} = \frac{2.048\,\text{V}}{2^{16} - 1} = 31.25\,\mu\text{V}. \tag{3.14}$$

Moreover, the injection capacitance of 890 fF has been replaced with a 1.184 pF capacitance. This change has been made to accommodate a requested increase in input range. The LSB value of the injected charge and its maximum value are:

$$Q_{inj,lsb} = 0.037\,\text{fC}\ (0.841\,\text{keV}),$$
$$Q_{inj,max} = 2.425\,\text{pC}\ (55.1\,\text{MeV}).$$

As in the SLIDER8 case, the MAX6126 and the MAX541 are placed on the test board (or on the front-end board) whereas all the other parts of the injection circuit are directly integrated inside each channel of the ASIC.

3.1.3 pSLIDER32 digital back-end

The pSLIDER32 digital back-end has been modified in order to be able to set the voltages of the blocks included in the new architecture. All the 8-bit registers of SLIDER8 are replaced with 32-bit registers in order to work with the 32 channels architecture. The new/modified registers are:

- Operating Mode register, now composed of three bits:
  - The Self-Trigger bit (S) and the Aquisition Mode bit (A) are the same as in the SLIDER8 digital back-end.
  - The read out leakage current bit (I): this bit controls the signal *IT_SEL* shown in fig. 3.4. If this bit is set to 1, the digital back-end reads the sum of the detector leakage currents of the channels selected by the appropriate register (leakage current mask register). The leakage current is read by using the READ SEU FLAGS/TEMPERATURE SENSOR command. If this bit is set to 0 the digital back-end, instead, reads the value acquired by the temperature sensor.
- CSA reference adjustment register, composed by:
  - Room temperature bit (H): if the SLIDER8 tests are carried out at room temperature this bit must be set to 1. This bit modifies the currents, which flow in each channel blocks, in order to compensate for ASIC behavior at different temperatures. In particular, it modifies a resistor used to measure the leakage current and the temperature.

  - Reference adjustment (RRR): 3-bit used to control the reference voltage of the Krummenacher charge restoring block in the CSA. ($V_{ref,GM}$ in fig. 2.1).

- Global Bias adjustment register, now composed of four bits:

  - Select temperature source bit (T): this bit is unused on pSLIDER32. However it has been added for the final version of the ASIC where a temperature sensor will be integrated directly on the ASIC.

  - The Global Bias (BBB) bits work in the same way as in the SLIDER8 case.

- Leakage Current Mask: 32-bit register used to select the channels where the leakage current will be read. Each bit generates the signal *En* which controls the switches, shown in fig. 3.5, of the corresponding channel. The least significant bit corresponds to channel 0, the most significant bit to channel 31. By using the READ SEU FLAGS/TEMPERATURE SENSOR command the digital back-end reads the sum of the leakage currents of the channels selected by this register.

- Calibration Mask: 32-bit register with the same function as in the SLIDER8 case.

- Discriminator Enable Mask: 32-bit register with the same function as in the SLIDER8 case.

- Discriminator Threshold: 8-bit register used to set the 8-bit DAC described in section 1.2.1.

- Fine Threshold Adj.: 32 3-bit registers. Each register is connected to one 3-bit DAC for the fine trimming of the threshold.

In table 3.1 all the messages used to set the pSLIDER32 back-end registers are listed. All the SLIDER8 8-bit commands are replaced with 32-bit commands and, as in the SLIDER8 case, all the bits expressed as xxx can be either 0 or 1. New commands have been added to set the new registers (as the Leakage Current Mask, the Discriminator Threshold and the Fine threshold registers).

COMMAND NAME	COMMAND CODE	INPUT DATA	OUTPUT DATA
READ EVENT DATA	00000xxx	-	Event Data Packet
READ SEU FLAGS/TEMPERATURE SENSOR	00001xxx	-	SEU & Temperature Word
READ OPERATING MODE	00010xxx	-	00000ISA
READ SHAPER TIME CONSTANT	00011xxx	-	00000TTT
READ CSA REFERENCE ADJUSTMENT	00100xxx	-	0000HRRR
READ GLOBAL BIAS ADJUSTMENT	00101xxx	-	0000TBBB
READ LEAKAGE CURRENT MASK	00111xxx	-	32 bit word
READ DISCRIMINATOR ENABLE MASK	01000xxx	-	32 bit word
READ CALIBRATION MASK	01001xxx	-	32 bit word
READ DISCRIMINATOR THRESHOLD	01010xxx	-	DDDDDDDD
READ FINE THRESHOLD ADJ. CH. #NNNNN	011NNNNN	-	00000FFF
WRITE OPERATING MODE	10010ISA	-	-
WRITE SHAPER TIME CONSTANT	10011TTT	-	-
WRITE CSA REFERENCE ADJUSTMENT	10100xxx	0000HRRR	-
WRITE GLOBAL BIAS ADJUSTMENT	10101xxx	0000TBBB	-
SET CALIBRATION DAC VOLTAGE	10110xxx	16 bit word	-
WRITE LEAKAGE CURRENT MASK	10111xxx	32 bit word	-
WRITE DISCRIMINATOR ENABLE MASK	11000xxx	32 bit word	-
WRITE CALIBRATION MASK	11001xxx	32 bit word	-
WRITE DISCRIMINATOR THRESHOLD	11010xxx	DDDDDDDD	-
WRITE FINE THRESHOLD ADJ. CH. #NNNNN	111NNNNN	00000FFF	-

Table 3.1: Reading and writing messages format of pSLIDER32 digital back-end

The commands that have been added with respect to SLIDER8 are:

- READ SEU FLAGS/TEMPERATURE SENSOR, which will be described in section 3.1.3.
- WRITE/READ LEAKAGE CURRENT MASK.
- WRITE/READ DISCRIMINATOR THRESHOLD.
- WRITE/READ FINE THRESHOLD ADJ. CH.

READ SEU FLAGS/TEMPERATURE SENSOR

The READ SEU FLAGS/TEMPERATURE SENSOR command is used to acquire the value of the temperature and the detector leakage current which flows in the pSLIDER32 channels. If the read out leakage current bit "I", described in section 3.1.3, is set to 1 the answer is the digitized value of the temperature, otherwise the output is the digitized value of the detector leakage current. The data packet is shown in fig. 3.6. It is divided in two parts:

- The first 11 bits contain the digitized value of the temperature/leakage current depending on the bit I.
- The other 7 bits contain the SEU flags, shown in table 3.2, which represents the status of the registers. If the status of one of these flags changes its value during a measurement, the corresponding register could be compromised.

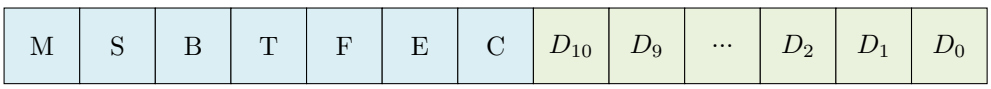

Figure 3.6: pSLIDER32 read temperature sensor/leakage current packet.

FLAG	Controlled Registers
M	Operating Mode
S	Shaper Time Constant
B	Global Bias Adjustment
T	Discriminator Threshold
F	Fine Threshold Adjustment
E	Discriminator Enable Mask
C	Leakage Current Mask

Table 3.2: pSLIDER32 SEU flags.

3.2 pSLIDER32 setup and front-end board

For pSLIDER32 testing, initially, a specific test board has been designed. For the later measurements the front-end board shown in fig. A.36 has been used.

3.2.1 Test board

The pSLIDER32 test board is mainly composed of:

- one power supply connector used to provide the single bias voltage of +7 V
- a specific socket for the ASIC. With this component it is possible to mount and extract the ASIC without soldering it to the test board. This solution makes it possible to test several samples with only one test board.
- The 16-bit DAC Maxim MAX541AESA of the injection circuit, described in section 3.1.2.
- The Voltage Reference Maxim MAX6126AASA21 of the injection circuit, described in section 3.1.2.
- The temperature sensor Texas Instruments LTM84, described in section 3.1.1.
- 16 analog output switches. Each one of these is connected to one analog block output of the channels 0 and 31. These blocks are already listed in section 3.1 and shown in blue in fig. 3.2. As can be seen in fig. 3.7, all the switches outputs of one channel are connected together to the same buffer. Because of this configuration only one switch can be active at the same time.
- 2 buffers. These components are connected to the output of the switches described above and shown in fig. 3.7. These buffers are used to decouple the analog outputs from the measurement instruments. Moreover they introduce a gain factor of 2.
- 3 address switches. These swiches identify each front-end board when they are connected together in rows of 6. In fact, the data acquisition system must be capable to communicate with only one of these 6 Front-end boards. In order to obtain this, the 3 SPI chip selects and the 3 address switch values must be exactly the same during the SPI communication.

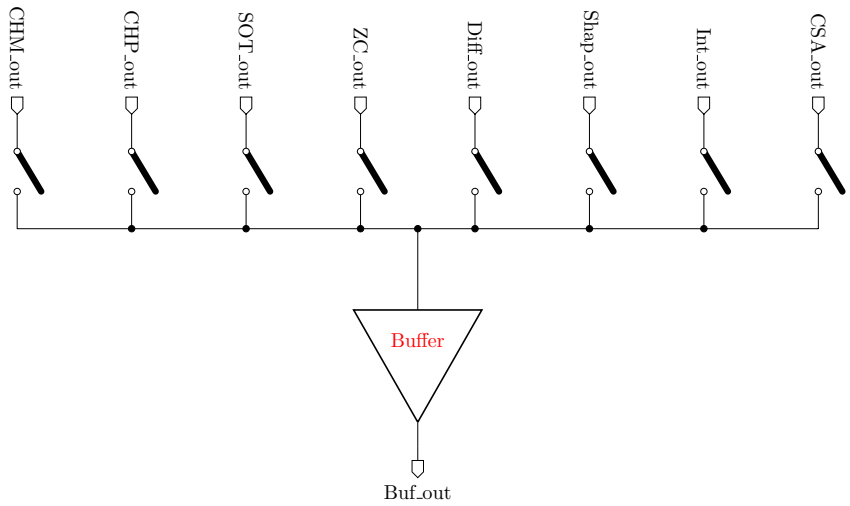

Figure 3.7: analog switches schematic of the pSLIDER32 test board. This structure is replicated on the test board for channels 0 and 31.

- 3 LDO (Low-DropOut) regulators. These components translate the test board supply voltage of 7 V in:
  - analog ASIC supply voltage (1.8 V);
  - digital ASIC supply voltage (1.8 V)
  - Calibration 16-bit DAC supply voltage (3.3 V).

  Their task is to generate a constant and least noisy possible supply voltage for the ASIC.
- one 24-pin connector. By means of this connector, the SPI signals (SCLK, SDI, SDO, CSEL<0>, CSEL<1>, CSEL<2> and their negated), the sampling procedure signals (INJECT, CONV, ADCCLK, BUSY and their negated) and 4 ground pins are sent to the ASIC from the measurement instrument (in the pSLIDER32 case, an FPGA has been used to test the ASIC).

This board implementation followed the rule where analog and digital supply voltages are separated. This prevents the digital signals from having an effect on the analog voltage integrity.

The features of this test board have been exploited for all the analog measurements that will be described in section 3.3.

3.2.2 Front-end board

The front-end board that houses the pSLIDER32 ASIC is shown in fig. A.36. The particular "cross" like shape is needed to allow the "round" detectors to be placed in the empty spaces of the front-end board and connected to the channels of the ASIC. Some of the components of this board are the same as in the test board previously described. The main differences are:

- the socket for the ASIC is removed and the ASICs are directly soldered on the top of the board.

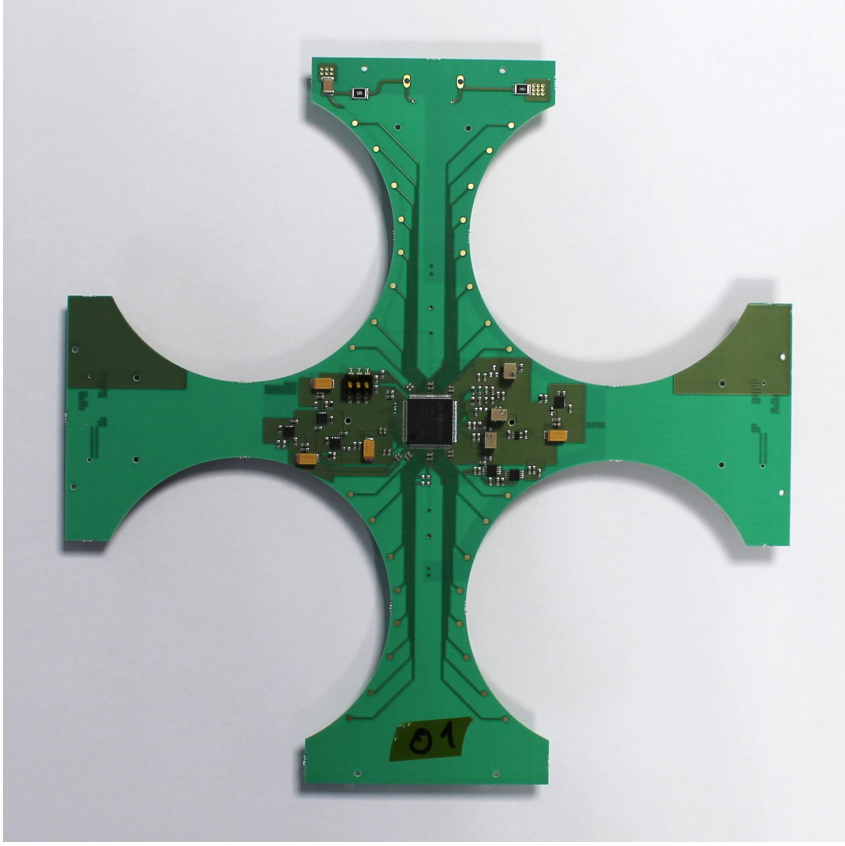

Figure 3.8: pSLIDER32 front-end board.

- The PCB supply voltage connector and the 24-pin connector are replaced with two ERNI high-speed micro connectors (male 254877, female 354178), because, in the final experiment, all the supply voltages will be provided by means of a flex rigid board. Obviously, the ERNI connectors are two: one to connect a front-end board to the previous one, the other is used to connect it to the following FEB. The last front-end board in the chain of six requires an additional terminating connector that hosts the 100 Ω resistors needed to adapt the 100 Ω differential digital signal traces.
- The 16 analog output switches and the 2 buffers are removed, since all the ASICs are tested before the real experiment.

3.3 Analog Measurements

The first tests that have been carried out concern the analog outputs of the blocks of the channels 0 and 31 that have been made accessible in pSLIDER32. In particular, the CSA and shaper outputs have been acquired using an oscilloscope. All shown results are not averaged. As described in section 3.2 the analog outputs are connected to a non-inverting discrete operational amplifier that introduces a gain factor of 2.

3.3.1 CSA

The time response of the CSA to a charge pulse at the input has been measured by exploiting the injection circuit and by varying the emulated injected charge from 10000 DAC units (370.04 fC, 8.41 MeV) to 50000 DAC units (1.85 pC, 42.05 MeV). As an example, the acquired time responses of the channel 0 CSA are shown in fig. 3.9. In this figure the DC component of the signal has been removed in order to better evaluate the rise time of the CSA. Moreover, the relevant calculated rise times are shown in fig. 3.10 as a function of the injected charge. From this plot it is clearly visible that for lower energies the rise time is higher with respect to the ones obtained at higher energies. This behavior is in agreement with the simulation results and is related to the increase in the feedback capacitance which, in turn, results in an increase of the loop gain. It is worth noting that the rise time is much shorter than the integration time. Therefore, the time response of the amplifier can be considered as an ideal voltage step.

3.3.2 Shaper

Also the signals at the shaper output were acquired. This was done by placing a probe before the buffer, which saturates for higher energies. The main problem of this acquisition type is the introduction of noise, that is clearly visible in fig. 3.11, where the channel 0 shaper output for different values of the peaking time is shown. The injected charge in this figure is 20000 DAC units (740.08 fC, 16.82 MeV). Moreover, the output for the first 2 peaking times is clearly affected by the probe placed directly at the output of the shaper, which introduces a resistive and a capacitive load that the channel is not able to handle. Since the shaper output is not greatly affected by the probe load for higher peaking times, more analog acquisitions are shown in fig. 3.12, obtained by varying the injected charge from 10000 DAC units (370.04 fC, 8.41 MeV) to 50000 DAC units (1.85 pC, 42.05 MeV) and maintaining the peaking time fixed at 1.3 µs. In table 3.3 the measured peaking times for different injected charge are listed. The measured values exhibit a slight deviation with

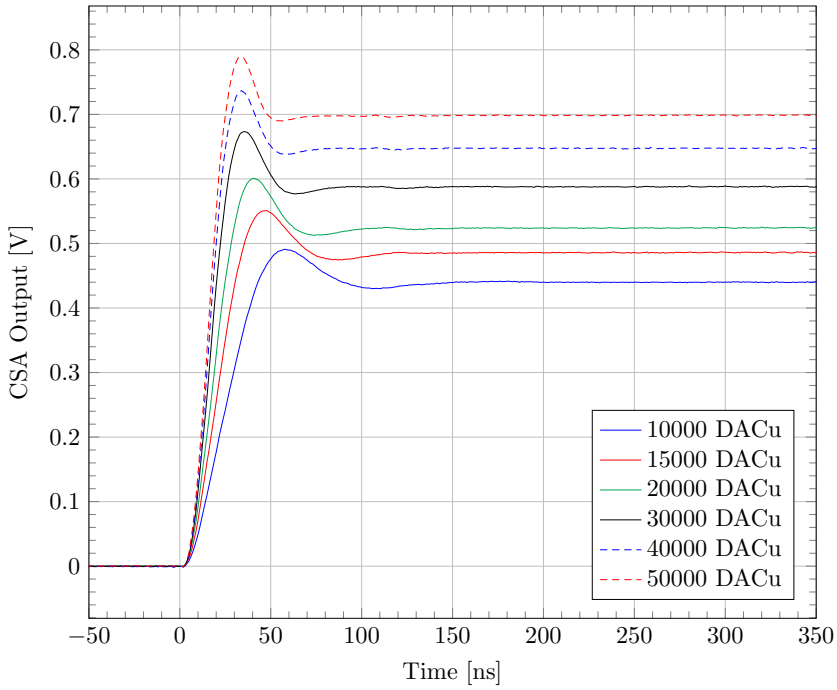

Figure 3.9: pSLIDER32 CSA output of the channel 0. The amplitude has a gain factor of 2 introduced by a non-inverting operational amplifer used to decouple the CSA output from the oscilloscope probe.

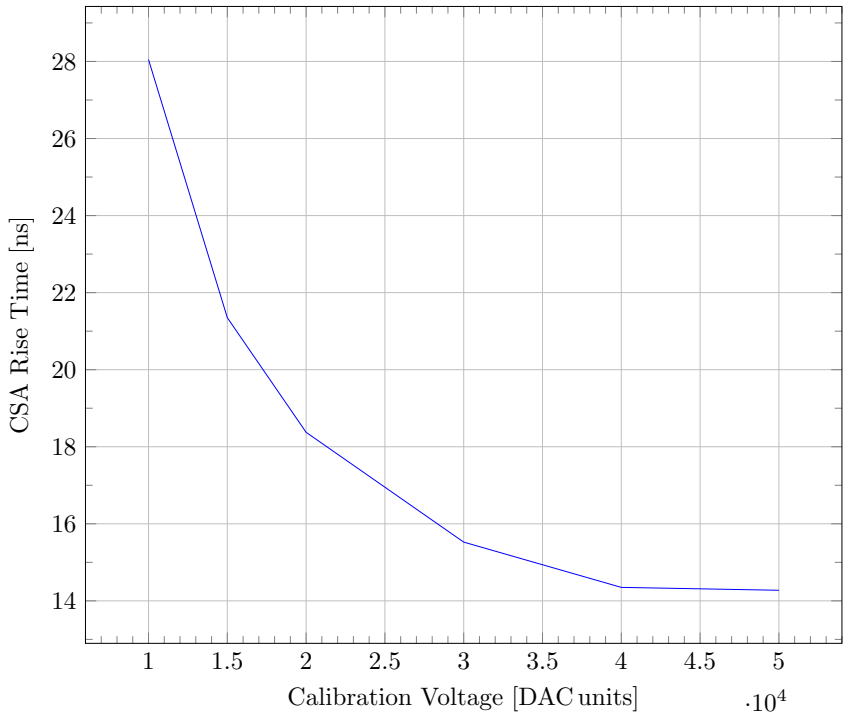

Figure 3.10: pSLIDER32 CSA rise times of the channel 0 as a function of the injected charge.

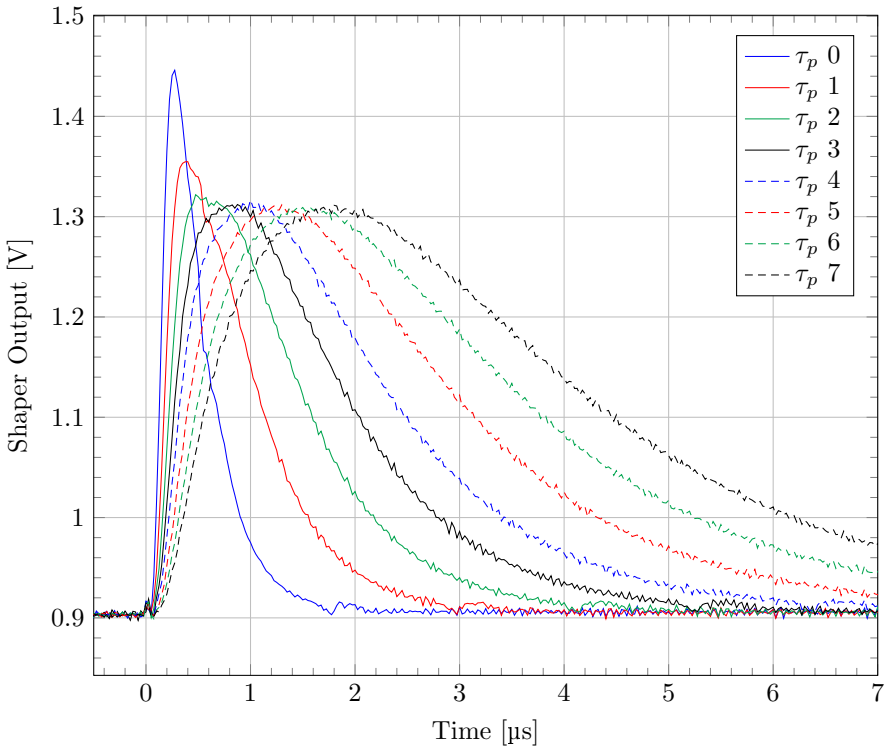

Figure 3.11: pSLIDER32 channel 0 shaper output for different values of the peaking time.

respect to the nominal one (1.3 µs). Nonetheless, these discrepancies, in the order of few %, do not affect the filter behavior and in particular its time response which maintains the expected unipolar semi-Gaussian shape.

3.4 Digital Measurements

Measurement results reported in this Section have been carried out by using the pSLIDER32 digital back-end. So, all the results are obtained by sampling the shaper output voltage stored in the sample & hold and then by digitizing it using the ADC. As in the SLIDER8

Injected Charge [DAC units]	measured τ_p [µs]
10000	1.27
20000	1.21
30000	1.29
40000	1.25
50000	1.31

Table 3.3: pSLIDER32 measured peaking times, obtained from analog measurements, for the peaking time 5 and different values of the injected charge.

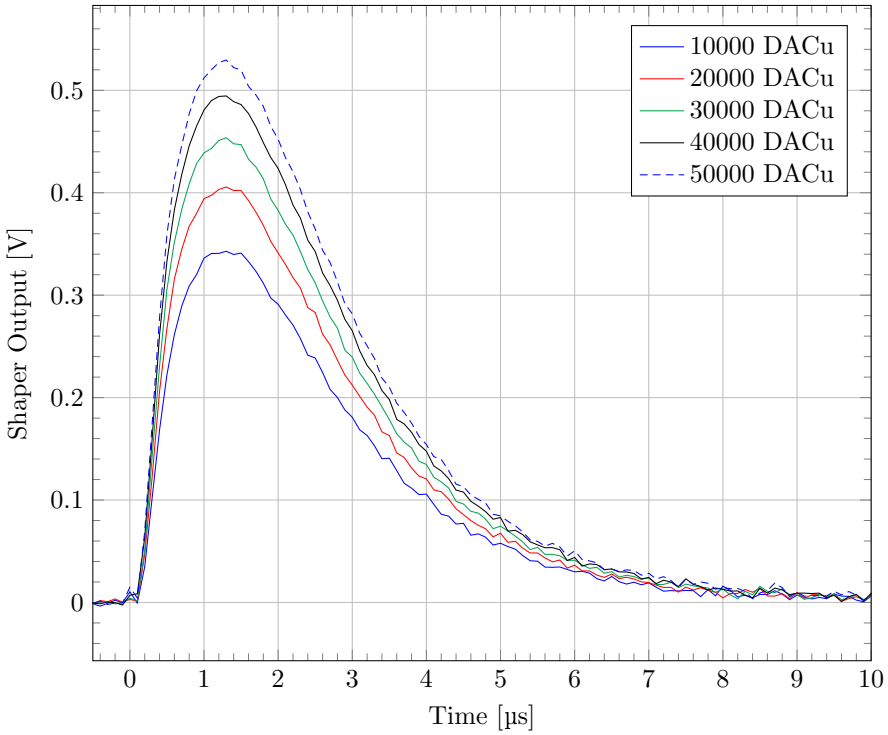

Figure 3.12: pSLIDER32 channel 0 shaper output for different values of the injected charge and for the peaking time 5.

ASIC, the pSLIDER32 front-end can be operated both in non-self-trigger mode and self-trigger mode (these two modes have been already described in section 2.2.3). All the measurements that will be presented in the next sections were carried out in non-self-trigger mode, except for section 3.4.6 where some self-trigger mode tests are reported. Since in this section all the values in the graphs and in the tables are expressed in DAC units and ADC units, a short list with the conversion factors from ADC units and DAC units to voltage is shown:

- 11-bit Channel ADC:

$$1\,\text{ADC unit} = \frac{2 \cdot 1.76\,\text{V}}{2^{11}} = 1.72\,\text{mV} \tag{3.15}$$

  where 1.76 V is the ADC input dynamic range. This value is multiplied by a factor of 2 due to the differential nature of the ADC.

- 16-bit Calibration Voltage DAC, already described in section 3.1.2:

$$1\,\text{DAC unit} = \frac{2.048\,\text{V}}{2^{16} - 1} = 31.25\,\mu\text{V}. \tag{3.16}$$

3.4.1 Waveform Scan

The waveform scans described in this subsection represent the channel time response, given by the shaper output multiplied by the gain factor introduced by the sample & hold, 5.14 V/V. By varying the interval t_C between the injection and the sampling time it is

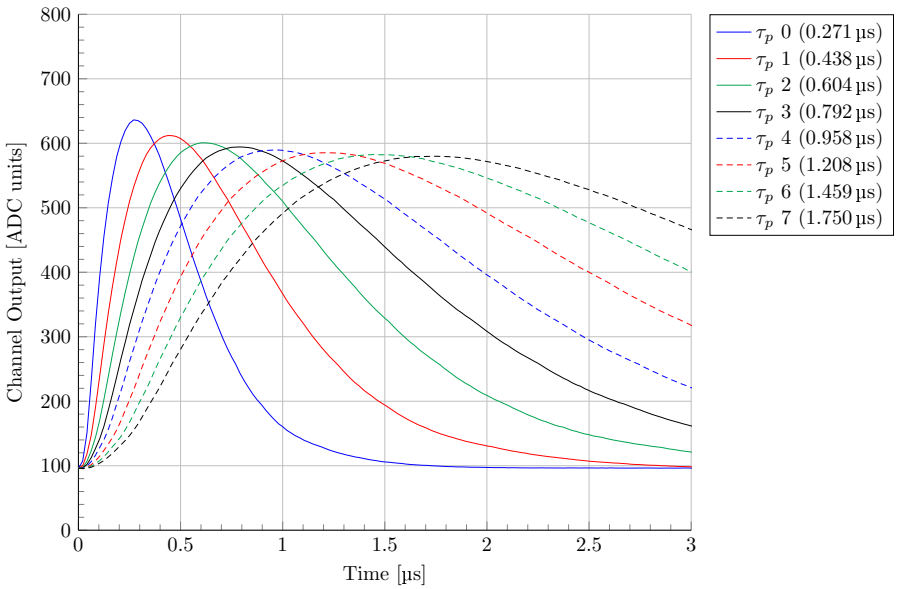

Figure 3.13: pSLIDER32 channel 0 output as obtained by varying the peaking time.

possible to reconstruct the channel time response. The same charge is injected up to 100 times in order to average the results over many responses. In figures 3.13 and 3.14 the time responses of the channels 0 and 28 are shown. The calibration voltage is set to 1000 DAC units, which corresponds to an injected charge of 37 fC (841 keV).

In particular, fig. 3.13 shows that the channel 0 works properly even if it has all the analog blocks accessible and, consequently, more parasitic resistance and capacitance. As explained before, channels 0 and 31 (with test points) have different gain with respect to the other channels (without test points), so the maximum value reached at the peaking time is slightly different. In table 3.4 the mean and the standard deviation of the peaking times of all the channels are reported. The values of the measured peaking times are very similar to the simulated ones. The small differences between the measurements and the simulations are mainly caused by the error introduced by the minimum t_C step, which is

$$t_{C,min} = \frac{1}{48 \cdot 10^6\,\text{MHz}} = 21\,\text{ns} \tag{3.17}$$

where 48 MHz is the clock of the FPGA used during the characterization.

In fig. 3.15, the time response of all the 32 channels belonging to the same ASIC are shown for the peaking time 4. It has been verified that all the channels in the ASIC work properly. The peaking times shown in the figure confirm what has been already reported in table 3.4. The value of the gain is different for each channel, so, the value reached at the peaking time is different for each channel. Information about the gain is given in section 3.4.2. In table 3.5 the minimum value, the maximum value, the mean value and the standard deviation of the baseline of all channels for all the peaking times is given. All the values are expressed in *ADC code*.

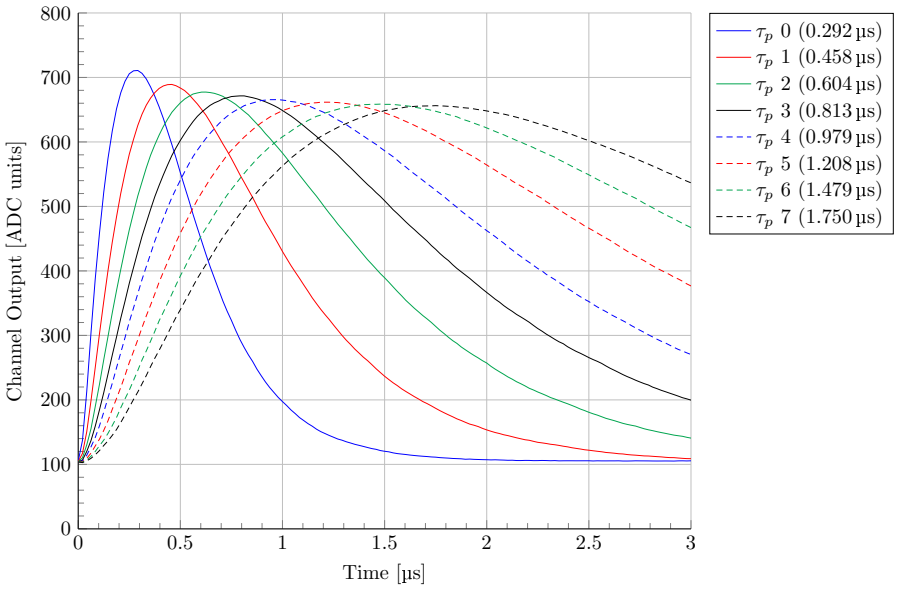

Figure 3.14: pSLIDER32 channel 28 output as obtained by varying the peaking time.

τ_p	simulated τ_p [µs]	measured τ_p [µs]	σ τ_p [ns]
0	0.30	0.29	5
1	0.50	0.46	5
2	0.65	0.63	10
3	0.85	0.79	13
4	1.00	0.96	15
5	1.30	1.22	22
6	1.50	1.47	27
7	1.80	1.75	21

Table 3.4: pSLIDER32 peaking times obtained from digital measurements.

τ_p	minimum	maximum	mean	std
0	60.39	123.88	90.67	16.46
1	60.04	123.01	89.94	16.37
2	59.83	122.67	89.64	16.34
3	59.91	122.05	89.51	16.24
4	59.87	122.59	89.62	16.31
5	59.43	122.06	89.53	16.25
6	59.60	121.81	89.50	16.30
7	59.62	122.19	89.45	16.26

Table 3.5: pSLIDER32 baseline values. All the values are expressed in *ADC units*.

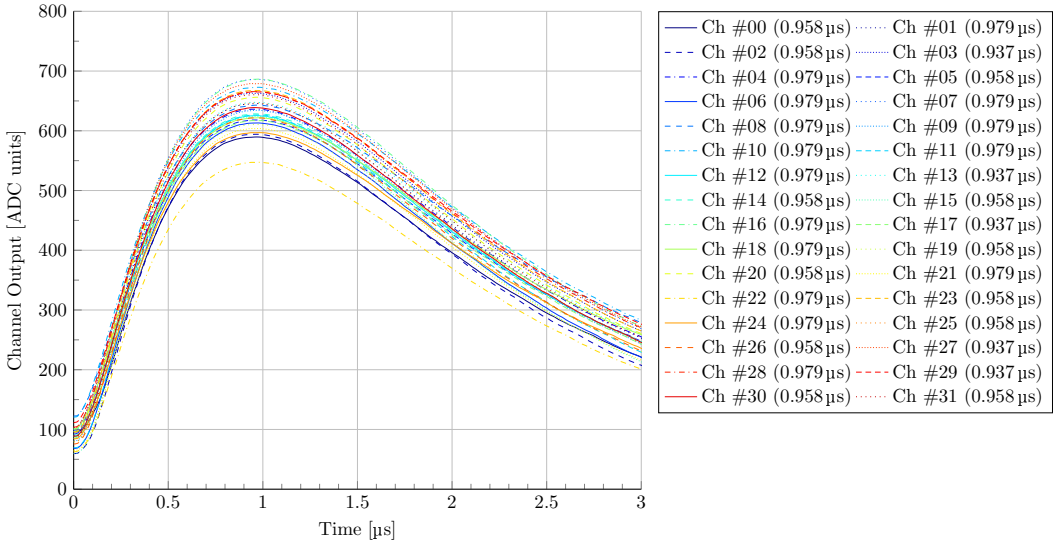

Figure 3.15: pSLIDER32 all channels output for peaking time 4.

In fig. 3.16 the channel 15 output for the peaking time 5 is shown for different values of the calibration voltage from 1000 DAC units (37 fC, 841 keV) to 20000 DAC units (740 fC, 16.82 MeV). As expected, the peaking time changes negligibly when the injected charge is changed.

3.4.2 Input-output channel trans-characteristic

In this subsection a description of the input-output channel trans-characteristic of the 32 channels is given. In order to obtain this curve, the channel output must be sampled precisely at the peaking time. In fig. 3.17 the result obtained for the channel 12, for all the 8 selectable peaking times, is shown. The values of the injected charge ranges from 0 to 60000 DAC units (2.22 pC, 50.45 MeV). As expected from the simulations, the gain increases for the lower peaking times. This is also confirmed by the waveform scans shown in the previous subsection. The dynamic compression feature of the channel is clearly visible in the figure.

In fig. 3.18 the input-output channel trans-characteristic of all the channels for the peaking time 2 is shown.

In fig. 3.19 the high gain region of channel 11, for the peaking time 3, is shown. In order to calculate the ENE of the channels, it is fundamental to find the value of the gain at very low energies (near 0 eV injected).

As a first attempt, a simple linear regression has been applied in order to fit the values obtained from the measurements. For this fit, only the values obtained with charge injection from 0 to 100 DAC units (3.7 fC, 84.1 keV) have been used. The gain, even for low energies, is not perfectly linear. If a larger range of values were used for the linear regression, a lower gain with respect to the real one would be obtained. The slope of the fit line represents the gain.

To improve the accuracy of the extraction method, a higher degree polynomial regression has been applied. From the tests, it was discovered that a cubic curve represents the gain behavior almost perfectly, for injected charge between 0 and 300 DAC units (11.1 fC,

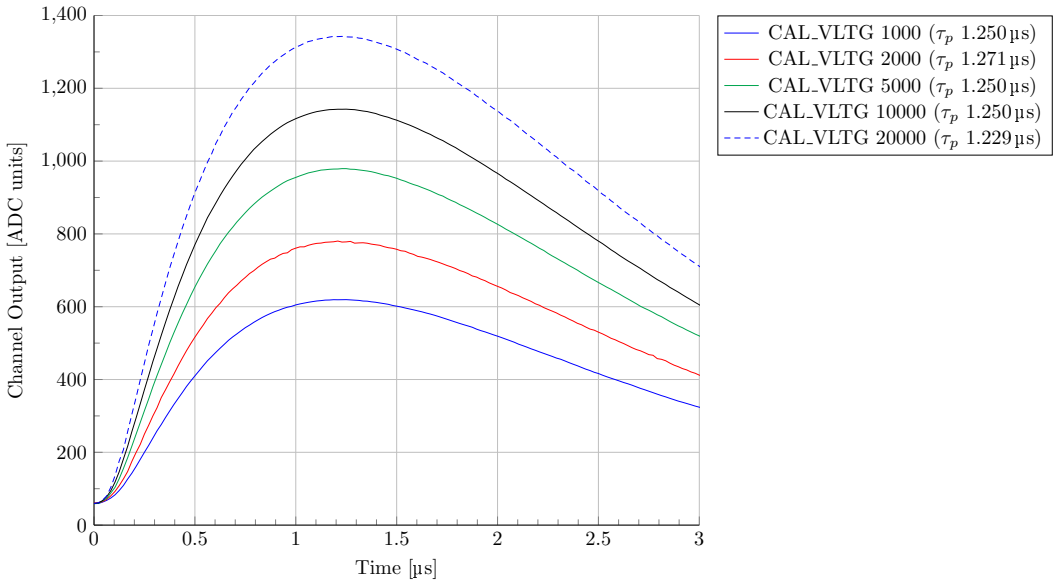

Figure 3.16: pSLIDER32 channel 15 output for peaking time 5 as obtained by varying the calibration voltage.

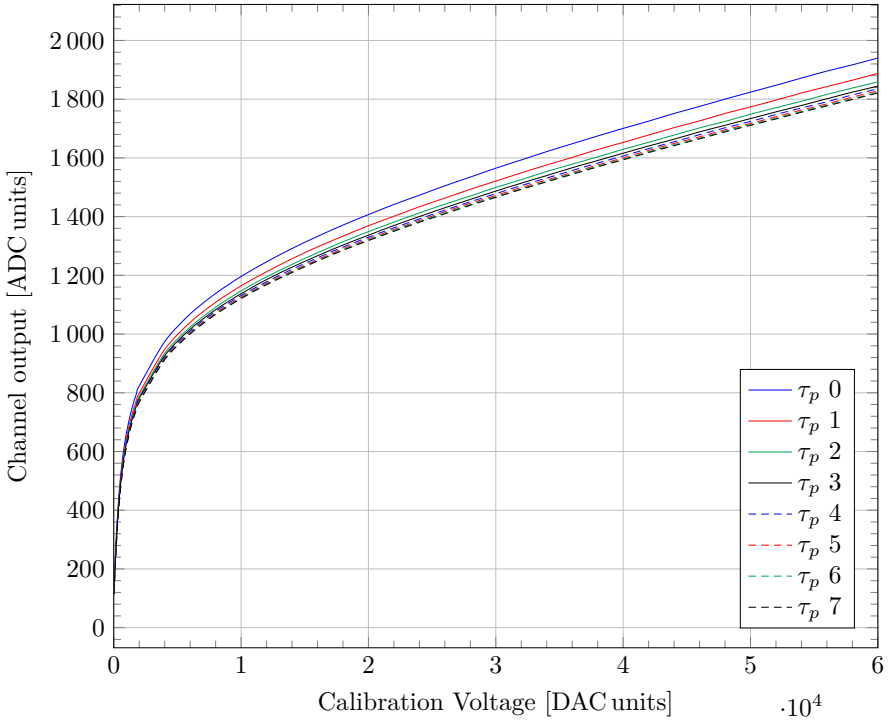

Figure 3.17: input-output trans-characteristic for pSLIDER32 channel 12 measured for all the selectable peaking times.

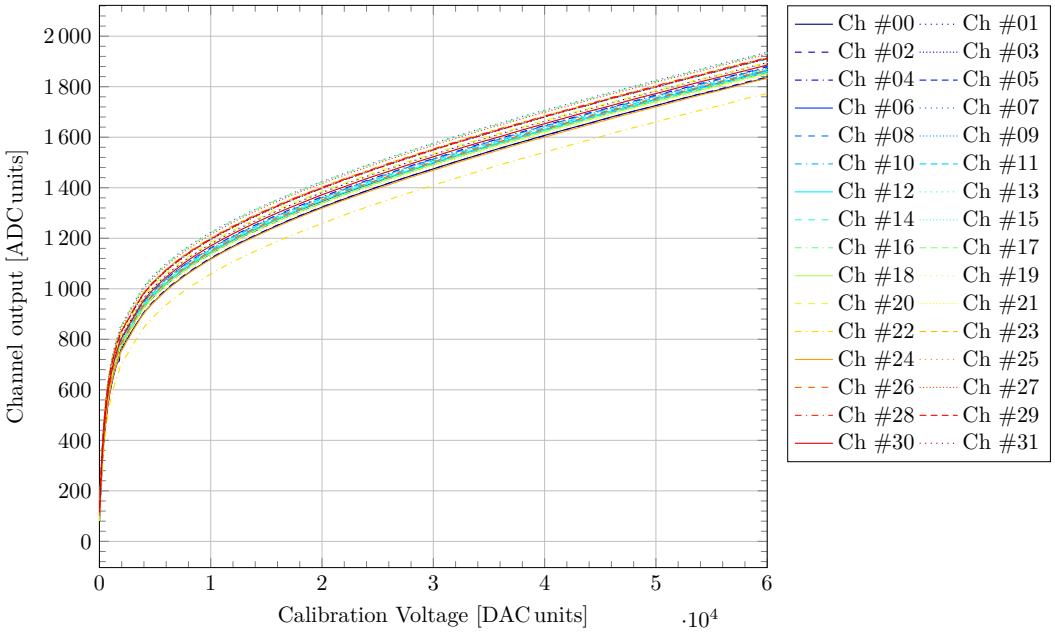

Figure 3.18: input-output trans-characteristic for all the channels in the pSLIDER32 chip (peaking time 2).

252.3 keV). Higher degree curves do not introduce significant improvements in the fit. A generic 3rd degree polynomial

$$f(x) = a \cdot x^3 + b \cdot x^2 + c \cdot x + d \tag{3.18}$$

can be differentiated

$$\frac{df(x)}{dx} = 3a \cdot x^2 + 2b \cdot x + c \tag{3.19}$$

and, if $x = 0$, it can be obtained that the gain of the derivative in 0 is equal to c.

In table 3.6 the minimum, the maximum, the mean, and the standard deviation of the gain values obtained with the linear regression and the cubic regression are shown. As expected, at lower peaking times, the gain is higher. Moreover the gains found with the cubic regression are higher than the linear regression ones. The cubic fit provides a better interpolation of the acquired data in the low energy region.

3.4.3 Pedestals

A pedestal measurement consists of a repeated sampling of the channel output without the charge injection. If all the channels have the same gain, the standard deviation of the pedestal represents the channel noise at the sample & hold output. In order to obtain the equivalent input noise, the pedestal standard deviation must be divided by the channel gain. The mean value of the pedestal, instead, represents the baseline of the channel (already described in section 3.4.1). In fig. 3.20 and fig. 3.21 the results obtained for the peaking times 0 and 6 are shown respectively. As expected, the noise and consequently the pedestal standard deviation, decreases with the increase of the peaking time.

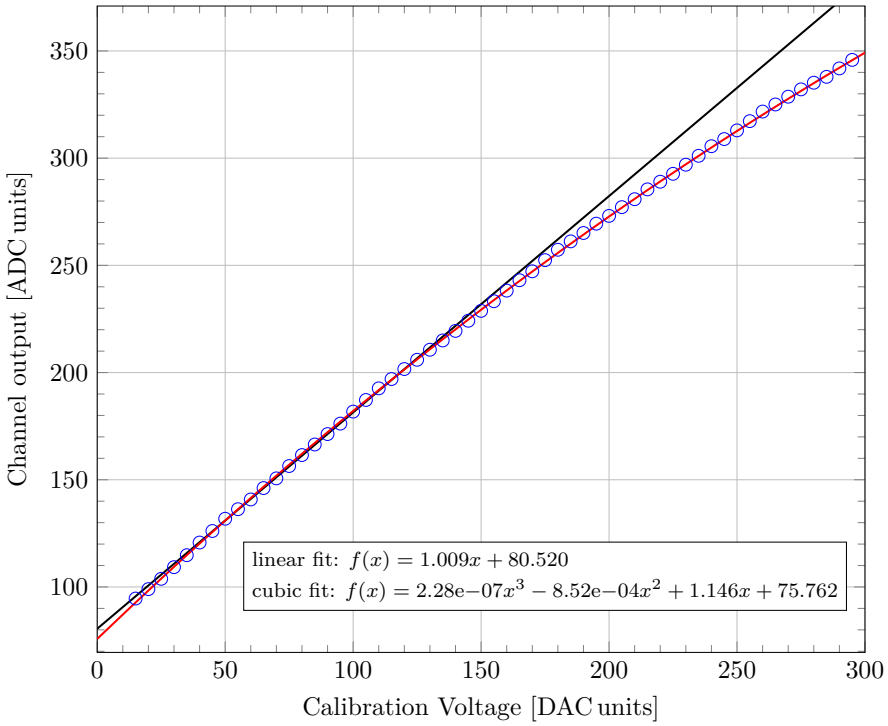

Figure 3.19: input-output trans-characteristic for channel 11 in the high gain region (peaking time 3).

	τ_p	minimum	maximum	mean	std
Linear fit	0	0.972	1.203	1.119	0.057
	1	0.871	1.139	1.055	0.056
	2	0.836	1.100	1.021	0.055
	3	0.804	1.078	1.002	0.057
	4	0.776	1.061	0.983	0.058
	5	0.748	1.040	0.964	0.058
	6	0.723	1.022	0.947	0.058
	7	0.711	1.014	0.903	0.057
Cubic fit	0	1.057	1.431	1.312	0.072
	1	0.937	1.296	1.207	0.064
	2	0.884	1.235	1.153	0.061
	3	0.848	1.192	1.121	0.059
	4	0.820	1.165	1.096	0.058
	5	0.788	1.126	1.061	0.056
	6	0.758	1.099	1.035	0.056
	7	0.732	1.069	1.008	0.055

Table 3.6: pSLIDER32 high gain values obtained with the linear regression and the cubic regression. All the values are expressed in $\frac{ADC\,units}{DAC\,units}$.

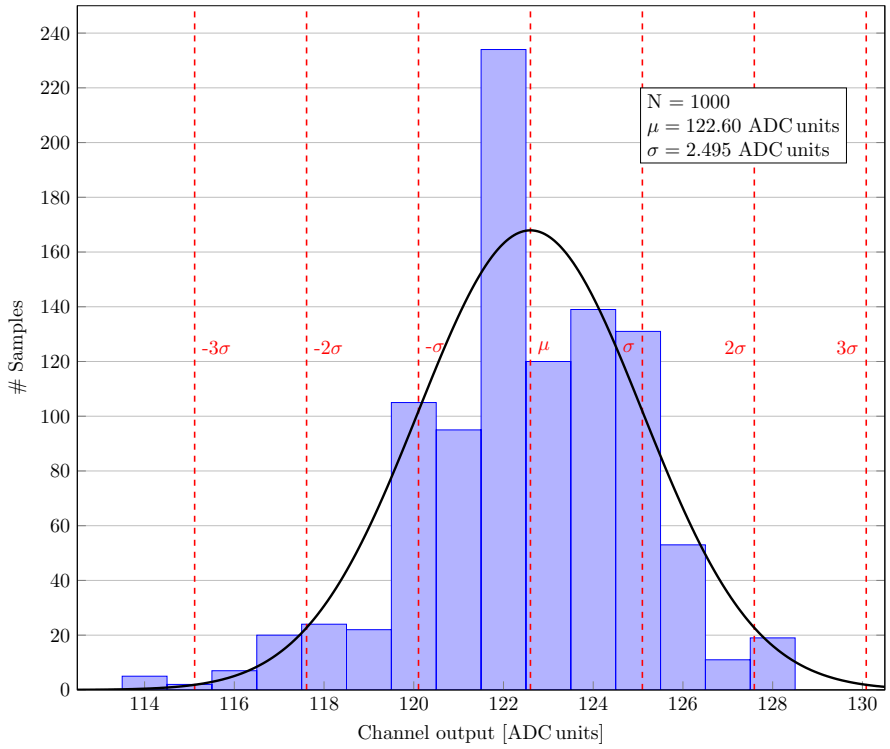

Figure 3.20: pSLIDER32 channel 8 pedestal for peaking time 0.

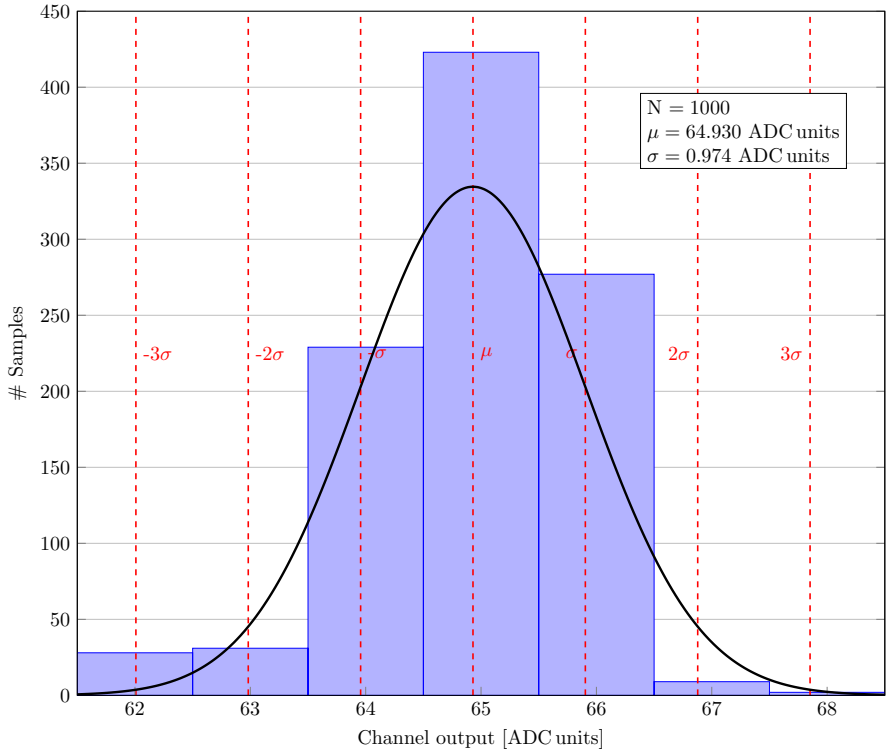

Figure 3.21: pSLIDER32 channel 21 pedestal for peaking time 6.

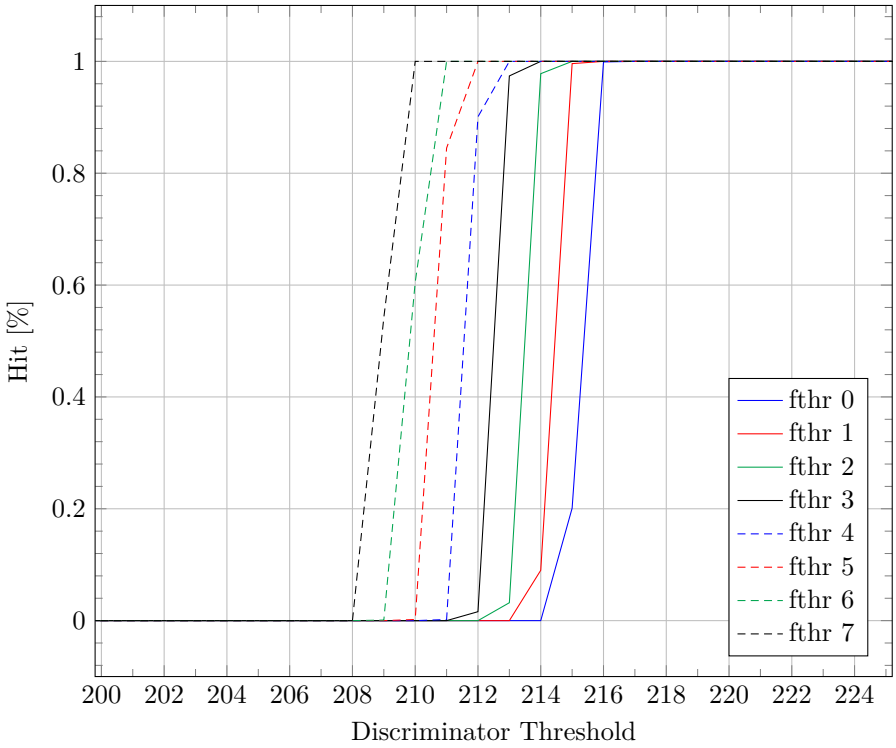

Figure 3.22: pSLIDER32 channel 18 threshold scan for the peaking time 5 as obtained by varying the fine threshold.

3.4.4 Threshold Scan

In the threshold scans the bit A of the operating mode register is set to 0. In this way, if the Signal Over Threshold comparator output is at logic 1, the channel output is sampled. Otherwise, if the Signal Over Threshold level is 0, the channel output is not sampled. So, if the threshold is higher than the baseline of the channel the comparator never fires, whereas if the threshold is lower than the baseline the comparator always fires. The most interesting case is when the comparator threshold is close to the baseline: the number of hits in this range provides information about the channel noise. So, a threshold scan has been performed by varying the 8-bit DAC described in section 1.2.1 from 0 to 255 DAC units. In fig. 3.22 a threshold scan for every configuration of the fine threshold trimming DAC is shown. On the y-axis the firing efficiency, expressed as the percentage of the Signal Over Threshold comparator hits over the number of samples, is reported. As explained in section 1.2.1 for lower DAC codes the threshold is higher, so, in this zone, the SOT comparator fires only for large injected charge. These threshold scans show that each bit of the fine threshold DAC is able to correct, on average, 0.913 DAC_thr units.

In fig. 3.24 the threshold scan of all channels, with fine threshold set to 011 and peaking time 4, are shown. As can be seen from this plot, the threshold dispersion is not optimized. Thus, for each channel and peaking time, the values of the fine threshold that minimize the global threshold dispersion must be found.

As a first step, the data obtained from the threshold scan must be fitted with the function:

$$f(x) = 0.5 + 0.5 \cdot erf\frac{x-a}{\sqrt{2}\cdot b} \tag{3.20}$$

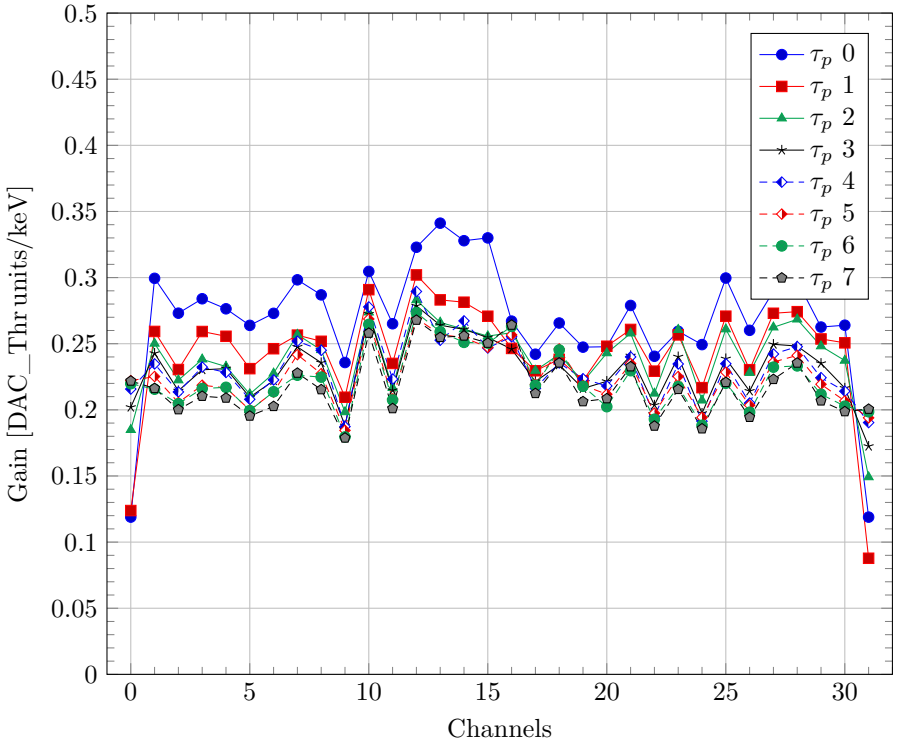

Figure 3.23: Conversion from DAC_thr units to keV for all the channels and peaking times.

where erf is the error function, which permits to obtain:

- a: the channel SOT comparator threshold (corresponding to a 50% firing efficiency);
- b: the noise.

These two parameters are expressed in DAC_thr units.

Using the a value just found for every channel, it is possible to calculate the threshold dispersion, that is 4.532 DAC_thr units. The difference between the maximum and the minimum value of the parameter a is

$$\Delta a = a_{max} - a_{min} = 17.18\,\text{DAC\_thr units}. \tag{3.21}$$

In fig. 3.23 the conversion from DAC_thr units to keV for all the channels and peaking times is shown. The mean conversion value is 0.234 DAC_thr units/keV. The resulting value of the incoming energy that can be discriminated from the comparator is 4.27 keV/DAC_thr units which is a value very close to the one obtain in the simulations described in section 1.2.

If this operation is done for every fine threshold value, the minimization of the global threshold dispersion can be easily obtained:

- as a first step, the mean $\overline{a}$ is calculated by means of the values of a obtained from the threshold scan for all the combinations channel-peaking time/fine threshold.
- The second step consists in finding, for each channel and peaking time, the value of the fine threshold that provides a value of a as close as possible to $\overline{a}$.

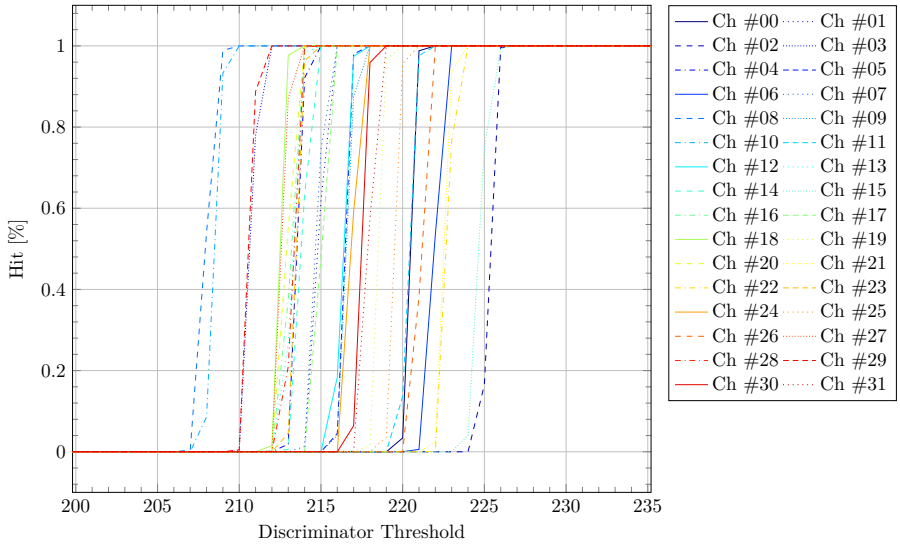

Figure 3.24: threshold scan for all the channels in pSLIDER32 for the peaking time 4 with the fine threshold set to 011.

In fig. 3.25 the fine threshold of all the channels is set to minimize the threshold dispersion. The resulting minimized threshold dispersion is 2.19 DAC_thr units. If the outliers are removed from the calculation of the threshold dispersion, its value changes to 0.421 DAC_thr units. However, in order to obtain such a small value of global threshold dispersion, the number of channels that are considered as outliers is 10. This is a value too big to consider the ASIC working correctly. In conclusion, the global threshold dispersion value found is not optimal due to the 3-bit fine trimming DAC LSB which is too small.

In the future ASIC production the size of the LSB will be increased. The value of the new fine threshold DAC LSB that will minimize the threshold dispersion is found in this way:

- the maximum range e_a, expressed in DAC_thr units that the fine threshold DAC will correct, is found as:

$$e_a = 2 \cdot \max\left(a_{max} - \overline{a}, \overline{a} - a_{min}\right). \tag{3.22}$$

- This value is then divided by the maximum number of combinations of the 3-bit fine threhsold DAC, obtaining:

$$e_{LSB} = \frac{e_a}{2^3}. \tag{3.23}$$

The value of e_{LSB} found is 3.065 DAC_thr units.

Before applying this correction, new simulations will be carried out in order to evaluate the degradation of the tuning capability [16, 17]. Moreover, results obtained from the characterization of other ASICs will be kept in consideration to identify the best value of the LSB that minimize the threshold dispersion.

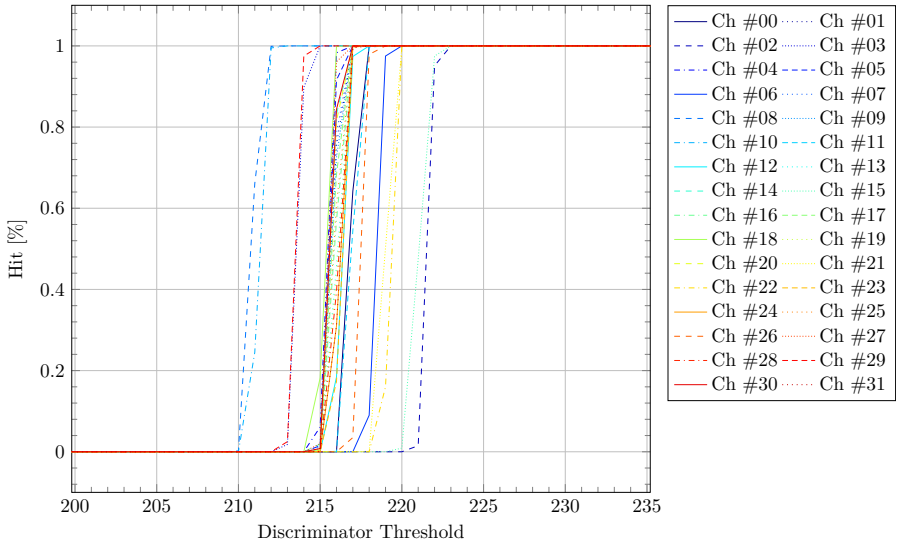

Figure 3.25: threshold scan for all the channels in pSLIDER32 for the peaking time 4 with the fine threshold set to minimize the threshold dispersion.

3.4.5 ENE

The ENE has been evaluated for all the channels and peaking times using the gain found with the cubic regression. The ENE has been calculated by means of

$$ENE[\text{DAC units}] = \frac{V_{S\&H,rms}[\text{ADC units}]}{G_n \left[\dfrac{\text{ADC units}}{\text{DAC units}}\right]}, \tag{3.24}$$

where

- $V_{S\&H,rms}$ is the standard deviation of the data obtained in the pedestal measurements.
- G_n is the gain, in the low energy region, obtained from the input-output channel trans-characteristic measurements with the cubic fit.

In order to obtain the ENE expressed in keV:

$$ENE_{FWHM}[\text{keV}] = 2.35 \cdot \frac{ENE[\text{DAC u}] \cdot C_{inj}[\text{fF}] \cdot 31.25 \left[\dfrac{\mu\text{V}}{\text{DAC u}}\right]}{0.044 \left[\dfrac{\text{fC}}{\text{keV}}\right]} \tag{3.25}$$

$$= 2.35 \cdot ENE[\text{DAC u}] \cdot 0.841 \left[\frac{\text{keV}}{\text{DAC u}}\right]. \tag{3.26}$$

Since the noise is Gaussian, the FWHM equals 2.35 times its r.m.s. value.

In fig. 3.26 and in fig. 3.27 the ENE is shown for all the channels and all the peaking times. The heat-map shows that there are some regions (near channel 14) noisier than others. However, all the channels have an ENE lower than the 4 keV value set by the project requirements although this limit holds for a detector capacitance of 40 pF.

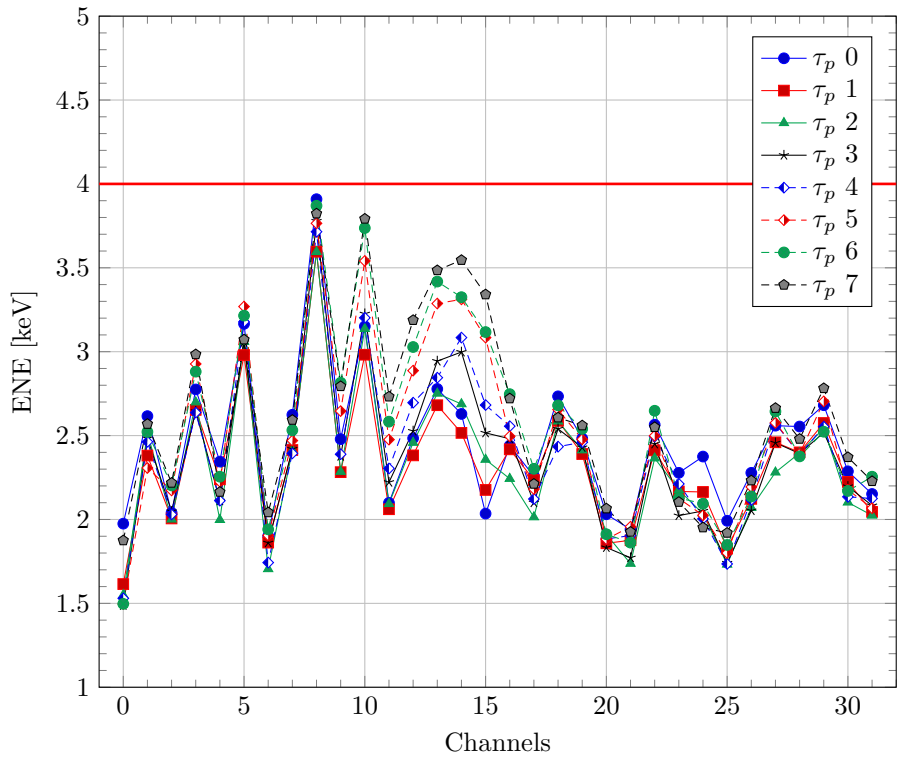

Figure 3.26: ENE for all the pSLIDER32 channels for all the selectable peaking times.

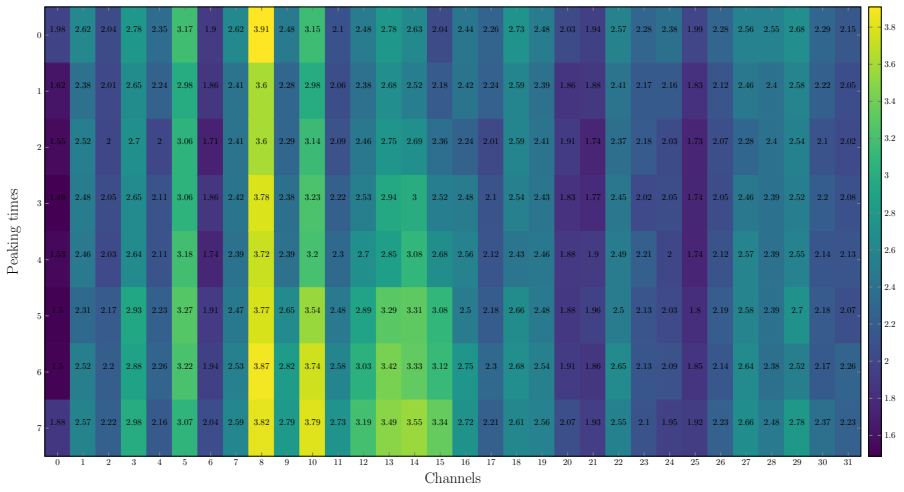

Figure 3.27: Heat map of the ENE for all the pSLIDER32 channels and all the peaking times.

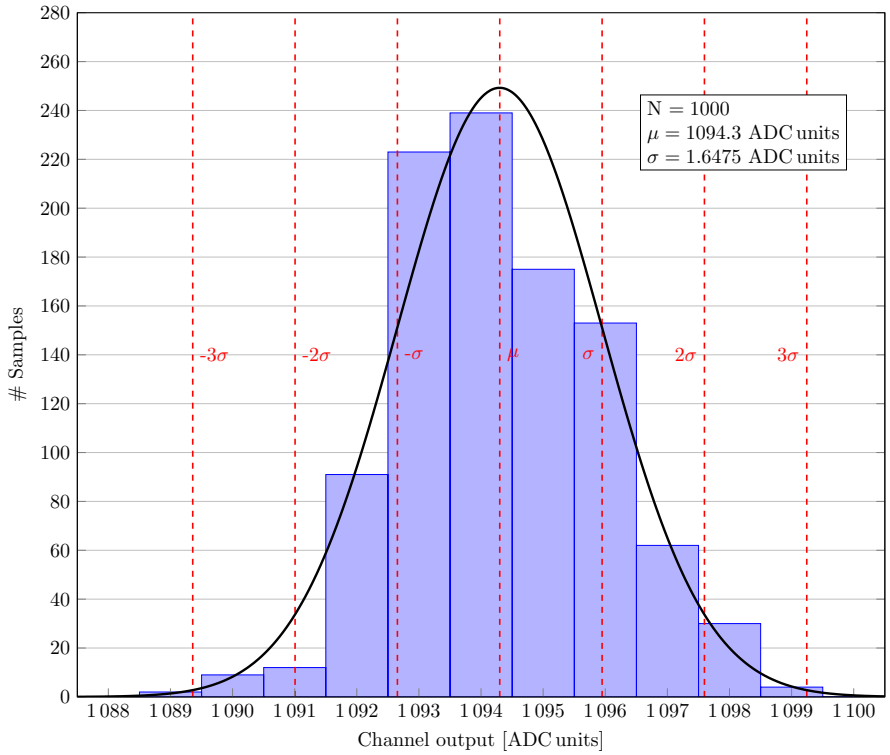

Figure 3.28: statistical analysis of pSLIDER32 channel 21 output sampled 1000 times in self-trigger mode for peaking time 4.

3.4.6 Self-trigger mode

The pSLIDER32 self-trigger mode works in the same way as for the SLIDER8 chip, already described in section 2.2.3. The ZC comparator fires at the shaper peaking time, as a consequence the digital back-end automatically generates the signal used to sample the channel output. This mode will be used to detect incoming particles that are not synchronous with the trigger provided by the experiment. However, during the ASIC characterization tests, the injection circuit will be used instead of the real detector. For this type of tests, the same charge is injected in a single channel (in order to prevent cross-talk between the channels) a predefined amount of times. The inject charge is 10000 DAC units (0.37 pC, 8.41 keV). From the digitized output results, the mean and the standard deviation are calculated. Statistical analysis of results from the characterization of channel 21 are reported in fig. 3.28, while all the means and standard deviations of all the channels are reported in table 3.7. As can be seen, self-trigger results are very similar to the one obtain in non self-trigger mode (described in section 3.4.1 and section 3.4.2). The little difference of the amplitude acquired in self-trigger and non self-trigger mode is due to the delay in the peaking sampling time. More in detail, in self-trigger mode, a delay between the ZC comparator transition and the sampling signal is introduced by the digital back-end.

ch	ST mean [ADC units]	ST std [ADC units]	ch	ST mean [ADC units]	ST std [ADC units]
0	1074.80	1.432	16	1185.18	1.634
1	1136.23	1.600	17	1106.25	1.520
2	1082.90	1.518	18	1106.62	1.560
3	1156.29	1.579	19	1097.85	1.510
4	1122.97	1.615	20	1147.09	1.494
5	1107.63	1.541	21	1094.32	1.647
6	1105.57	1.687	22	1025.09	1.967
7	1185.99	1.892	23	1162.59	1.816
8	1126.50	1.903	24	1081.14	1.830
9	1124.36	1.721	25	1137.19	1.708
10	1161.33	1.659	26	1110.37	1.653
11	1120.19	1.754	27	1171.62	1.531
12	1113.68	1.749	28	1160.62	1.597
13	1133.89	1.726	29	1158.38	1.603
14	1114.72	1.708	30	1128.33	1.563
15	1122.97	1.960	31	1149.54	1.564

Table 3.7: statistical analysis (mean and standard deviation) of channel output, sampled 1000 times in self-trigger mode, for all the channels and for the peaking time 4.

3.4.7 Temperature sensor measurements

In order to test the temperature sensor placed on the front-end board and to verify the correct communications between the sensor and the ASIC, the test board has been placed in a cooling chamber, where the temperature has been lowered from 20 °C to about 10 °C. The conversion factor from voltage to temperature is already described in section 3.1.1. In this type of measurement, the operating mode register is set to 000, whereas the bit "H" of the CSA reference adjustment register is set to 1. Using these settings it is possible to obtain the value of the temperature by using a "READ SENSOR TEMPERATURE" command. In fig. 3.29 the result obtained from this measurement is shown. As can be seen in this plot, the measured temperature decreases correctly with respect to the actual temperature, reaching almost 10 °C. The chamber does not have control of the humidity so the measurement was interrupted before the established temperature was reached to prevent condensation on the circuits. Further tests at lower temperatures, near the expected flight ASIC working temperature (−40 °C), will be carried out in future tests.

3.4.8 Leakage current measurements

The leakage current measurement circuit has been tested in order to demonstrate its correct behavior. In the real experiment, a leakage current is drawn by the detector connected to the channel input. Since in these characterization tests the detectors are not available, resistors have been connected between the channel input and ground in order to generate a constant current that simulates the detector leakage. The real detector leakage current is expected to be less than 50 nA at room temperature. Since the channel transconductor maintains a fixed voltage of 300 mV at the channel input, the value of the available resistor

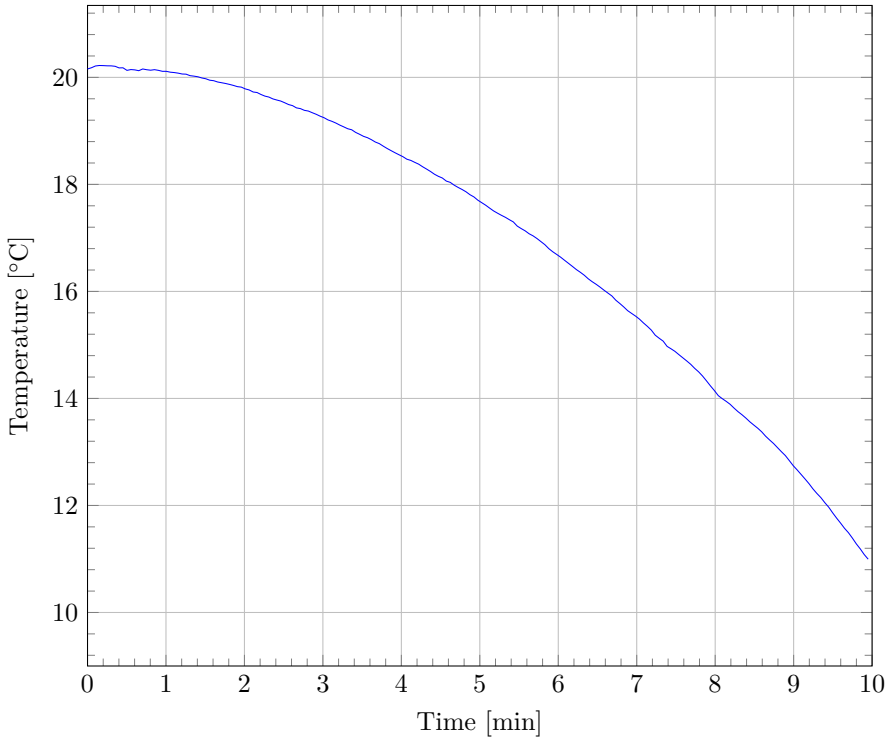

Figure 3.29: pSLIDER32 temperature sensor acquisition obtained for temperature variations from 20 °C to 10 °C.

that permits to obtain said current is 8.2 MΩ. This permits to generate a constant current of

$$i_{leak} = \frac{300\,\text{mV}}{8.2\,\text{M}\Omega} = 36.585\,\text{nA}.$$

These resistors have been soldered at the input of channels 15, 16 and 17. With the Leakage current mask register, described in section 3.1.3, it is possible to select from which channels the leakage current is read out.

The first test has been done with all the channels disabled. Ideally, the result from this measurement is 0 A. However, due to the non-ideality of the components of the leakage current measurement circuit, a very small current of 3.434 nA is read. This current offset is taken in consideration for the next analysis.

In table 3.8 the currents measured for the single tested channels are listed. The obtained values are higher than the ones expected from the i_{leak} calculated above. However, the difference between expected and measured current is lower than 10 % that is compliant with the application requirements.

In table 3.9 the expected and the acquired values of the leakage current, as obtained by varying the number of active channels, are reported. It is evident that the total current acquired by the leakage current measurement circuit does not increase linearly with the number of active channels. This behavior is evident in fig. 3.30, where the aggregated current and the sum of the individual current are compared with the expected value

ch	leak. current [nA]	leak. current (w/o offset) [nA]
15	46.188	42.754
16	45.236	41.802
17	43.467	40.033

Table 3.8: detected leakage current for pSLIDER32 channels 15,16 and 17 . Resistors of 8.2 MΩ have been used in order to generate these currents.

active channels	expected leak. current [nA]	measured (with offset) leak. current [nA]	measured (w/o offset) leak. current [nA]
-	0	3.434	0
15	36.585	46.188	42.754
15, 16	73.171	81.447	78.013
15, 16, 17	109.756	111.845	108.411

Table 3.9: aggregated detected leakage current for channels 15, 16 and 17.

in a single plot. In particular, the red line corresponds to the sum of the values of the currents acquired with only one active channel. This effect can be easily explained with the reduction of the output resistance of the PMOS current mirrors shown in fig. 3.5 when several channels are connected in parallel.

Further investigations will permit to improve the leakage current readout.

3.5 Six front-end boards measurements

Tests on 6 modules connected using 5 flex-rigid boards have been carried out in order to verify the correct behavior of the entire module chain. Preliminary checks were carried out to verify the correct operation of the system. More in detail, the bias distribution and the communication with the ASIC have been checked. SPI communication has been successfully demonstrated up to 24 MHz (delays have been introduced in the FPGA firmware) and the ADCs of all the 6 boards have been operated up to 24 MHz. The main measurements that have been carried out are:

- power supply level and consumption,
- waveform scan,
- input-output channel trans-characteristic.

3.5.1 Power supply level and consumption

As described in section 3.2.1, the 3 LDO mounted on the front-end board generate 3 voltages: 2 used to bias the ASIC and 1 to bias the 16-bit Calibration Voltage DAC. On the pSLIDER32 test board these 3 LDOs are powered by the same power supply. In the FEB case, these 3

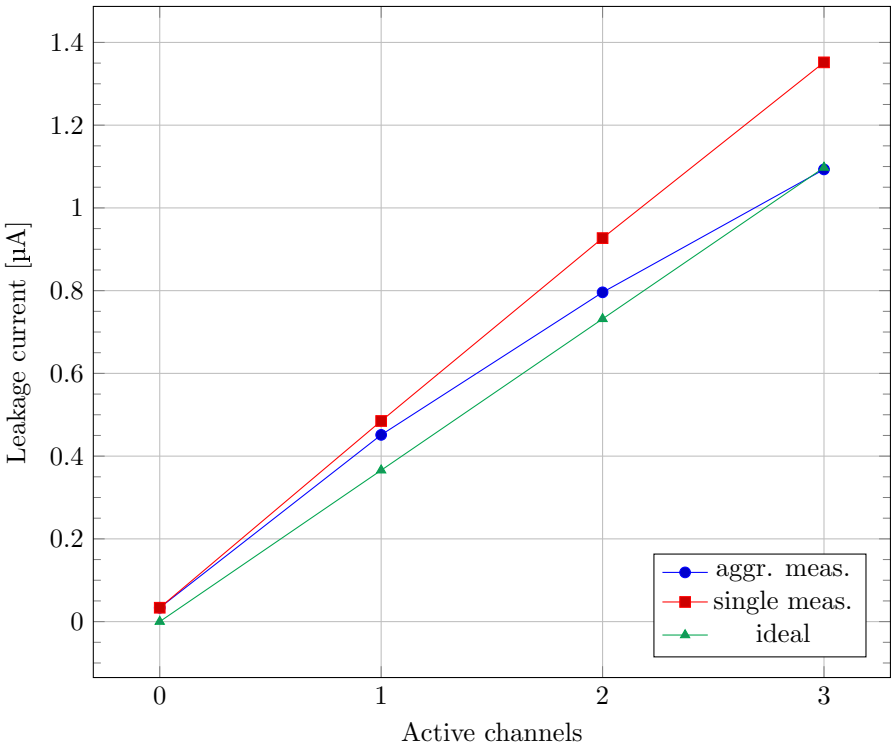

Figure 3.30: aggregated leakage current of the channels 15, 16 and 17. The green line corresponds to the expected value of the detected current. The blue line corresponds to the acquired value with more active channels. The red line corresponds to the sum of the currents acquired with only one channel active for each acquisition.

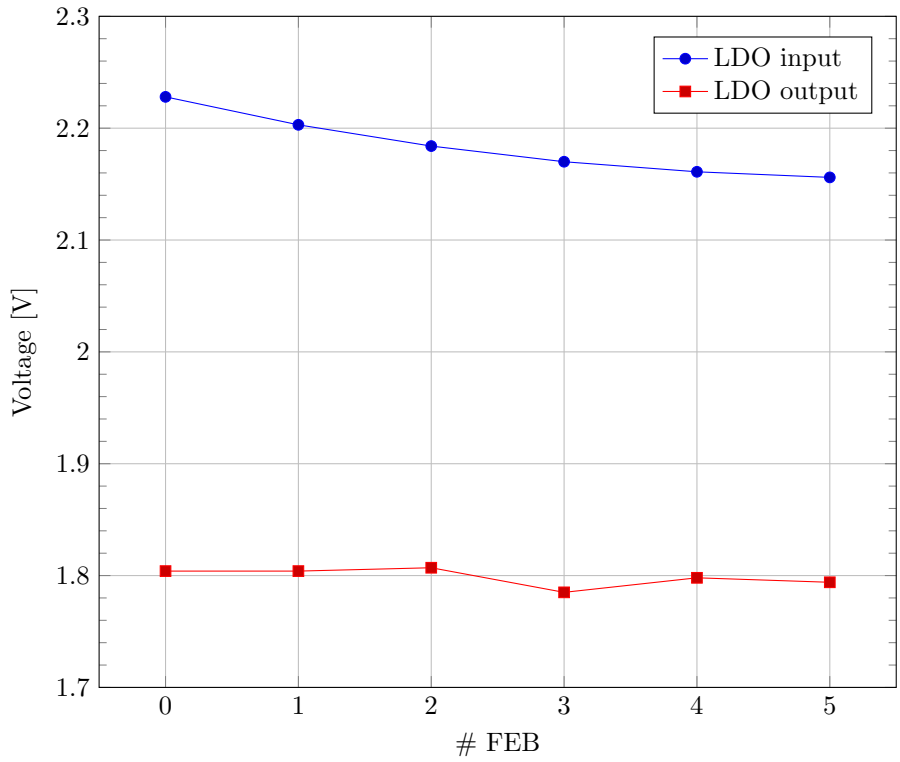

Figure 3.31: LDO inputs and outputs for all the 6 modules connected in series.

regulators are powered by three different power supplies. This permits to perfectly separate the analog section from the digital section. The three LDOs supply voltages are provided by an external source through the ERNI connector. The supply voltage for the LDO that requires more attention is the one used to generate the ASIC analog power supply. In fact, since each ASIC consumes a certain amount of power (235 mW to 270 mW required for each ASIC) and the PCB traces have a small but finite resistance value, the supply voltage decreases with the increasing of the trace length. The power supply-generated voltage is 2.4 V. In fig. 3.31 the value of the supply voltage at the input of the LDO is shown starting from the module nearer to the power source and ending with the module farther from the power source. All the modules are connected at the same time. As can be seen from this plot, the LDO is capable to generate a 1.8 V power supply. In future tests, the power supply voltage will be decreased to 2.1 V or 2.2 V. The digital and the 16-bit DAC power supplies do not have this problem since their section consumes less current than the analog part since all the 6 modules require about 50 mA (90 mW).

The second measurement regards the current consumption of each module (front-end board plus ASIC current consumption). Firstly, all 6 FEBs have been connected in order to evaluate the total current consumption. Secondly, each FEB has been removed one at a time from the entire chain in order to evaluate the current consumption of the single module. For each case, the current consumption has been evaluated for all the bias bits configurations (BBB, described in section 3.1.3). In fig. 3.32 the current consumption as obtained by varying the number of the connected FEBs and the bias bits is shown. The current consumption increases linearly with the number of modules connected in series.

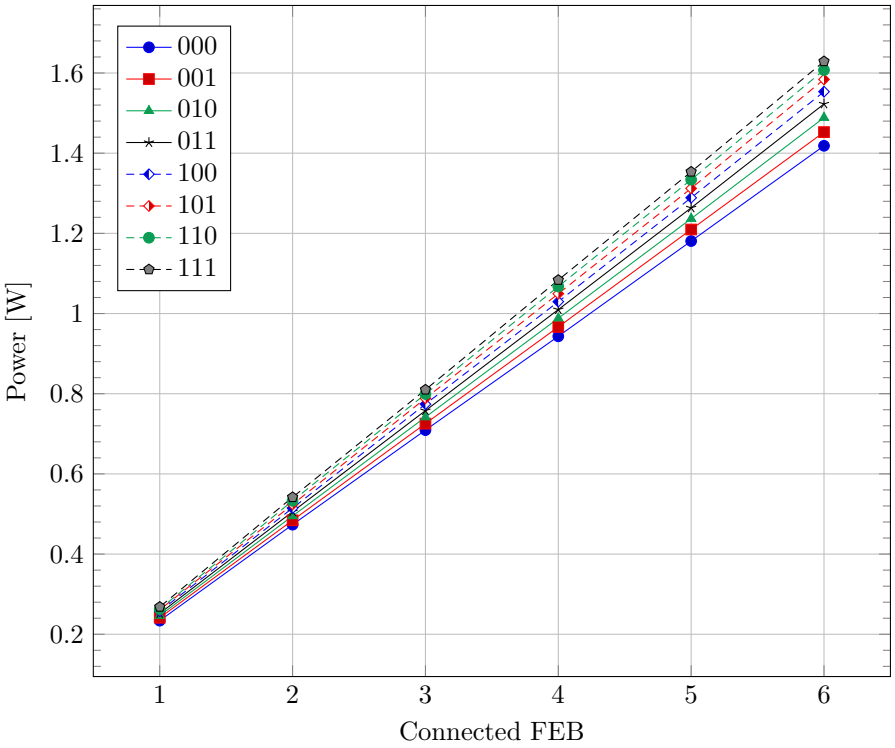

Figure 3.32: current consumption as a function of the number of connected modules and for all the bias register codes combinations.

Each module draws a power that ranges from 235 mW (BBB = 000, 7.31 mW/ch) to 270 mW (BBB = 111, 8.44 mW/ch) depending on the ASIC bias setting condition. These values respect the project requirement shown in table B.11.

3.5.2 Waveform Scan

Waveform scan measurements have been obtained for all the 6 ASICs connected in series. As an example, in fig. 3.33, channel 2 output of all the ASICs, for the peaking time 5, is shown. In table 3.10 the 6 measured peaking times are listed. The injected charge is 37 fC (841 keV). These values are very close to the ones obtained in the single FEB test (described in section 3.4.1). The main difference that can be noticed is the different gain of each channel. This behavior was already noted in the channels on the same ASIC (fig. 3.15). The amplitude of the channels response at the peak is reported in table 3.10.

3.5.3 Input-output transfer function

As pointed out in the previous subsection, the gain of each channel is a little bit different from each board in the chain. This behavior can be seen clearly in fig. 3.34 where the input-output trans-characteristic for channel 20 of each ASIC are shown for the peaking time 5.

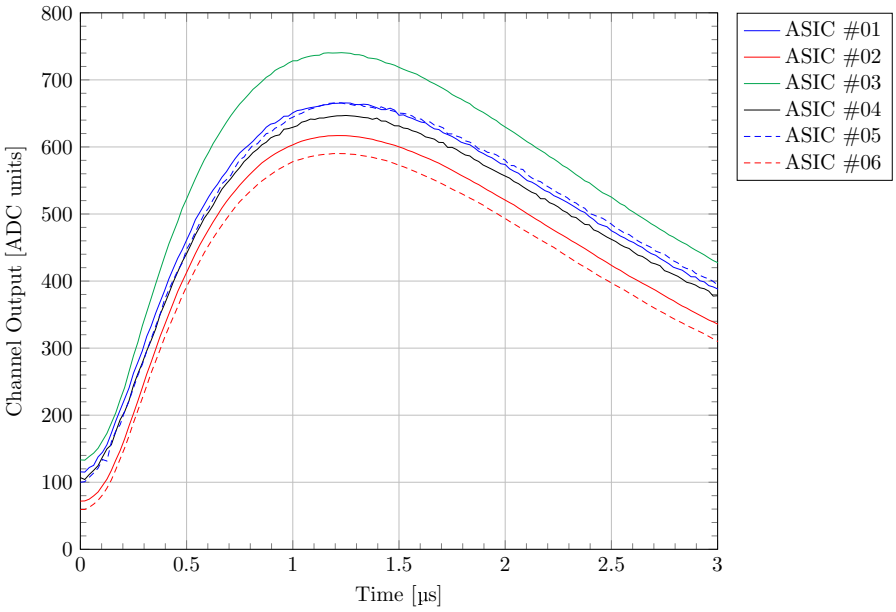

Figure 3.33: pSLIDER32 waveform scan for the channel 2 and peaking time 5 for all the 6 ASICs connected in series.

ASIC number	measured τ_p [µs]	Channel output [DAC units]
#01	1.25	665.60
#02	1.21	616.94
#03	1.23	740.59
#04	1.25	646.94
#05	1.21	666.06
#06	1.21	590.25

Table 3.10: pSLIDER32 measured peaking times, obtained from digital measurements, for the channel 2 and peaking time 5 for all the 6 modules connected in series.

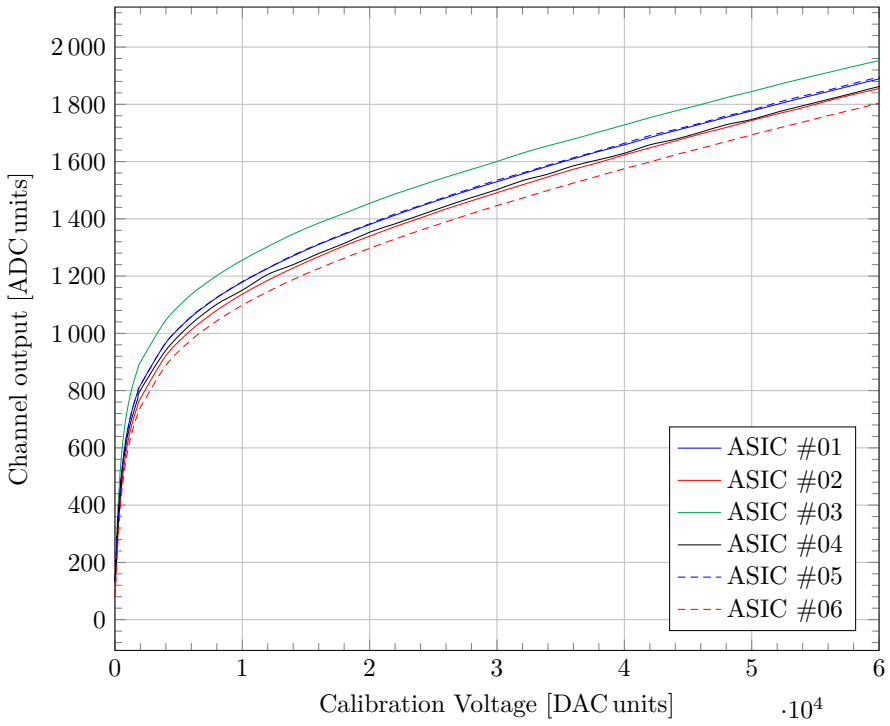

Figure 3.34: input-output channel trans-characteristics, obtained from digital measurements, for channel 20 and peaking time 5 for all the 6 modules connected in series.

Conclusions

GAPS (General Antiparticle Spectrometer) is an international experiment whose target is the detection of antideuterons and other low energy particles from cosmic rays. An Application Specific Integrated Circuit (ASIC) has been designed to read out the charge released by an incident particle in the GAPS Si(Li) detectors.

The main arguments discussed in this thesis work are relevant to the description of the design of some IP blocks used in the ASIC, the characterization of the analog readout channel and the characterization of three prototypes.

Two reduced versions of the final prototype (SLIDER4 and SLIDER8), composed respectively of 4 and 8 channels, provided helpful information about the behavior of the channel. SLIDER4 permitted to validate the functionality of all the main blocks included in the readout channel while SLIDER8 allowed the verification of the correct functionality of the back-end digital section.

The first prototype of the 32 channel flight ASIC, pSLIDER32, has been successfully tested both as a standalone device and mounted on a 6 layers PCB, the so called Front-End Board, with the same shape and built in functionality of the final flight hardware. The functionality of each block of the analog readout channel has been verified. As a final task of the activity, six front-end boards in series have been tested. The very promising results provided by these tests are of utmost importance since this multi-board structure represents the main building block toward the assembly of the entire flight tracker.

pSLIDER32 ASICs will be used in the assembly of a reduced version of the flight instrument, named GAPS Functional Prototype (GFP) starting from the beginning of 2021. The first balloon flight is scheduled in late 2022 from McMurdo Station in Antarctica.

Appendix

A The GAPS experiment

A.1 The Dark matter unsolved issue

A wide branch of modern physics is devoted to the study and the understanding of dark matter. Dark matter is an hypothetical component of the matter, that, unlike the known matter, does not interact with electromagnetic fields. As a consequence it does not absorb, reflect or emit electromagnetic radiation, making its detection very difficult. This is where the name "dark matter" comes from. The only effects that seem to be related to dark matter are the gravitational types, coming from astrophysical observations. In fact, there are some events that are not explainable by the common theories of gravity accepted by the scientific community, unless there is more matter with respect to what can be detected through all the other physical effects. In the standard Lambda-CDM (Cold Dark Matter) model, based on the Big Bang, dark matter has to exist because [18]:

- Galaxies and galaxy clusters could not be created in such a little time starting from the Big Bang calculated instant.
- In the present cosmological scenario (that has only the gravity as a cosmological force) galaxies behavior cannot be explained considering the visible matter only since it is not able to generate sufficient gravitational force.

Modern measurements indicate that dark matter accounts for 86 % of the total mass of the universe. Moreover, in the standard Lambda-CDM model, the total mass–energy of the universe is composed of [19]:

- 5% ordinary matter and energy,
- 26% dark matter,
- 69% dark energy.

Dark matter and dark energy are two different concepts. The sum of the dark matter and the dark energy account for 95% of the total mass–energy content.

Dark matter classification

One of the first questions scientists are trying to answer is: what is the possible composition of dark matter? Various hypotheses are being considered, the main two are:

- it could be made of, at least in part, by standard baryonic matter, such as protons or neutrons. These particles may compose astronomical bodies known as MAssive Compact Halo Objects (MACHOs) [19] whose detection is not easy. However multiple lines of evidence suggest the majority of dark matter is not made of baryons.

- It may be composed of a new type of fundamental particle. This is the dominant theory in the scientific community. Weakly Interacting Massive Particles (WIMPs) are among the most promising candidates for the composition of the non-baryonic dark matter [19, 20]. As described earlier, this type of matter does not interact like the other known particles, except for gravitational effects. However, non-baryonic matter presence can be revealed by indirect detection. In fact, if WIMPs are annihilated, they may produce other particles such as gamma rays and neutrinos.

Another type of classification that the scientific community uses to describe the particularities of dark matter, regards its velocity. In particular, this parameter indicates how far the dark matter moved in the first instants of the universe, before the cosmic expansion made it slow down. This distance is called *free streaming length* (FSL). Following this classification, dark matter can be divided into cold, warm, and hot. More precisely, this subdivision is done by comparing the dark matter FSL with respect to the size of a protogalaxy: if it is much smaller dark matter is classified as cold, if they have similar dimensions dark matter is called warm and, finally, if the FSL is larger than a protogalaxy dark matter is defined as hot.

The majority of scientists focus their research on the cold dark matter since this is the simplest explanation for most cosmological events. The constituents of cold dark matter range from large objects like MACHOs (baryonic type), to new particles such as WIMPs and axions (non-baryonic type) [19].

Dark matter identification

The identification of the matter is another of the main problems that researchers are trying to solve. Some experiments try to detect dark matter directly whereas others try to detect the products of its self-annihilation or decay.

- Direct detection experiments [19, 20]: this types of experiments try to observe the recoils, at very low energies, caused by the interaction of the dark matter, which is passing through the earth, with atomic nuclei. Special sensitive apparatus are designed in order to let the particles emit light (scintillators) or phonons (calorimeters) when dark matter passes trough them. Instruments must be able to distinguish background particles, which predominantly scatter off electrons, from dark matter particles that scatter off nuclei.

- Indirect detection experiments [19, 20]: this type of experiments try to detect the products of self-annihilation or decay of dark matter particles in outer space. In theory, two dark matter particles could annihilate in regions where the dark matter density is very high. In fact, there are regions, like the center of our galaxy, where the dark matter is expected to be present with a large concentration. The products of these events are supposed to be gamma rays, Standard Model particle–antiparticle pairs, or Standard Model particles. The main difficulty of this type of detection is distinguishing products of the annihilation of dark matter from products of other astrophysical sources [21]. Thus, different evidence is required for a conclusive discovery.

- Collider searches for dark matter [19, 20]: this types of experiments try to re-create dark matter particles in special colliders (like the Large Hadron Collider at CERN in

Geneva). All the discoveries obtained using colliders must be confirmed with other direct or indirect experiments in order to demonstrate that the newly found particle is really dark matter.

The detection of cosmic-ray antinuclei (antiprotons, antideuterons, and antihelium) can help researchers demonstrate or disprove a number of dark matter models because they offer unique sensitivity to annihilating and decaying dark matter. These indirect detections are very useful to evade or complement collider, direct, or other cosmic-ray searches, too. The search for cosmic antideuterons is a first-time type of experiment which offers a powerful new method of probing cosmic physics. The antideuteron peculiarity is its ultra-low astrophysical background, particularly at low energies. In fact, different dark matter models predict antideuteron flux in the energy range of a few GeV/n [21]. All the other types of dark-matter searches usually try to detect other types of particles, like the positron, in higher energy ranges (around 100 GeV). The main problem for these experiments is to distinguish the products of dark matter annihilation from other conventional sources that can produce positrons in this energy range.

The ultra-low astrophysical background for dark matter searches with antideuterons is a consequence of the kinematics of antideuteron formation. In standard cosmic-ray physics, antinuclei are produced when cosmic-ray protons or antiprotons interact with the interstellar gas [22]. High energy threshold for antideuteron production and the steep energy spectrum of cosmic rays mean that there are fewer particles with sufficient energy to produce an antinucleus, and those that are produced have relatively large kinetic energy. Therefore, low-energy antideuteron searches are virtually free from conventional astrophysical background. Meanwhile, low-energy antiproton measurements are crucial to these antideuteron searches, as any antideuteron detection must be consistent with antiproton search results. In principle, the production of antiprotons and heavier antinuclei in collisions of cosmic rays with the interstellar medium or dark matter annihilation or decay is tightly coupled, resulting in a degeneracy of the individual sensitivities to dark matter. However, the antinuclei formation processes have large uncertainties, and thus considerable freedom for the prediction of antideuteron and antihelium nuclei fluxes exists [21].

A.2 GAPS experiment

The General Antiparticle Spectrometer (GAPS) experiment main target is the indirect detection of low-energy (< 0.25 GeV/n) cosmic-ray antinuclei [23, 24, 25]. The experiment consists of ten planes of semiconducting Si(Li) strip detectors surrounded on all sides by a Time Of Flight (TOF) plastic scintillator system. The GAPS experiment relies on a novel particle identification technique based on exotic atom formation and decay [23]. Initially, a low-energy antiparticle, slowed down by the atmosphere, passes through the TOF. This permits to obtain some first information on the particle velocity and its energy. When the antiparticle passes through the detector, too, it loses further energy in the Si(Li) detector tracking system and, consequently, it slows down until it stop inside the instrument. If this happens, the antiparticle replaces a silicon shell electron and creates an exotic atom in an excited state with a probability near to one. The exotic atom de-excites through auto-ionization and radiative transitions emitting X-rays and, finally, annihilates with the silicon nucleus, producing a nuclear star of pions and protons [26]. The X-ray energies are uniquely determined by the antiparticle and silicon reduced mass and atomic

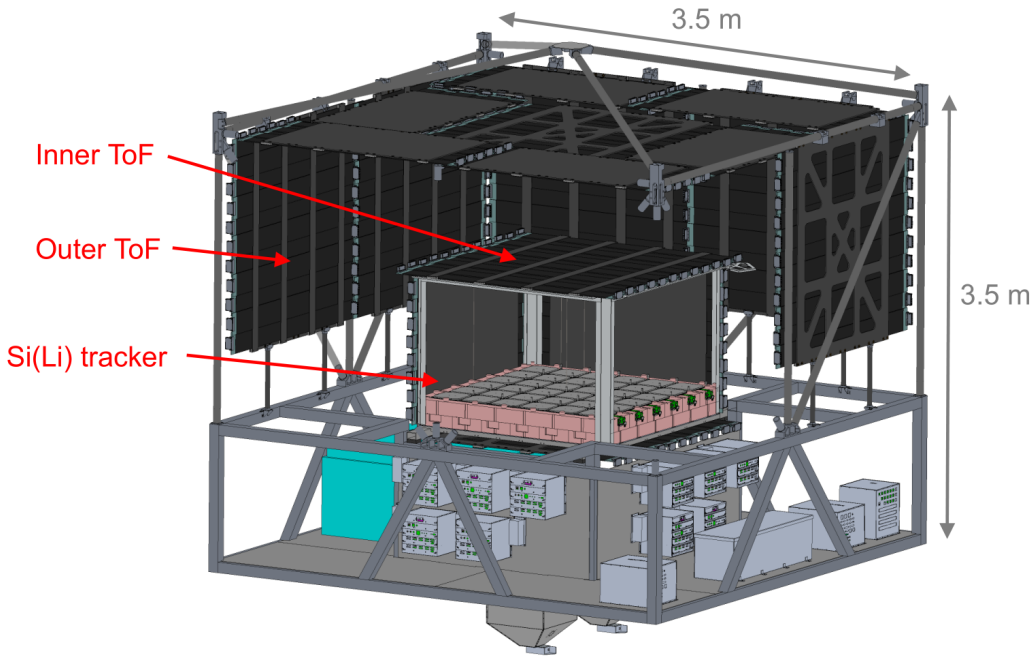

Figure A.35: entire final GAPS tracking system.

numbers. The main challenge for identifying antideuterons is the rejection of the dominant antiproton background. However, the GAPS detector design allows for the identification of either antiproton or antideuteron cosmic rays [27]. Even if the instrument is optimized for antideuteron detection, antihelium signatures can be easily detected, too. Due to the higher charge of the antihelium with respect to antideuterons and antiprotons, its analysis is much easier than the antideuterion-antiproton one.

GAPS is scheduled for its first Antarctic long-duration balloon (LDB) flight in late 2021, with the baseline sensitivity to antideuterons projected after a total of three Antarctic LDB flights.

A.3 GAPS tracking system

The GAPS instrument, shown in fig. A.35, is mainly composed of [28]:

- Two external layers of TOF plastic scintillators that surround the inner tracker. The outer TOF dimension are 3.5×3.5 m^2, with an height of 1.5 m. The inner TOF dimension are 1.5×1.5 m^2, with height of 1 m. The distance between the outer TOF and the inner TOF is 1 m. The entire TOF time resolution is about 300 ps [21].

- The inner tracker, that is subdivided in 10 layers with 10 cm separation in order to achieve 3D particle tracking. Each layer is composed of 12×12 Si(Li) detectors [29, 30]. Each detector has a diameter of 10 cm and a thickness of 2.5 mm. Moreover, each detector is segmented in eight strips in order to improve the spatial resolution enough to distinguish tracks from incident particles and exotic atom annihilation products [27]. Each strip is then connected to a front-end channel which processes the charge released by the passing particle. The GAPS detectors are capable to detect X-rays ranging from 20 keV to 80 keV and charged particles up to 50 MeV, at an

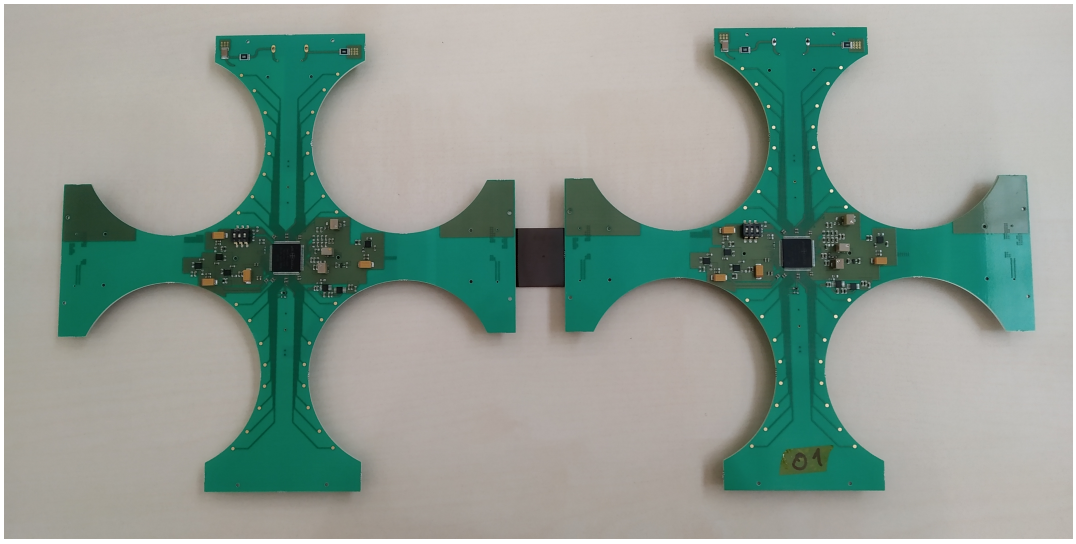

Figure A.36: two front-end boards, with a mounted ASIC, connected via one flex-rigid board.

operating temperature of −40 °C, with a FWHM energy resolution lower than 4 keV. In-flight, the cooling operation will be executed by a passive oscillating heat pipe approach, tested on two prototype test flights [31].

- As regards the electronics, each layer of the inner tracker is composed of 6×6 modules. Each module is made of one readout ASIC and one front-end board. 4 detectors are connected to one module. Each ASIC consists of 32 front-end channels capable to process the signals coming from 32 strips. The front-end board includes all the components used to guarantee the correct functionality of the ASIC. Two front-end boards can be connected with a flex-rigid board, specifically designed for this task, for a maximum of six front-end boards connected on the same line. Two front-end boards, with a mounted pSLIDER32 ASIC and connected via one flex-rigid board, are shown in fig. A.36.

B GAPS front-end

The final ASIC for the GAPS experiment will have 32 channels. Each channel will be connected to one strip of the detector. When an antiparticle passes through one strip of the GAPS instrument, it loses energy in each layer of the Si(Li) detectors. When it has lost enough energy, it stops and forms an exotic excited atom. Finally, the atom de-excites and emits X-rays. The remaining nucleus annihilates, emitting pions and protons. When an antiparticle passes through a strip of the detector, it releases a certain amount of charge. The product of the antiparticle annihilation release a certain amount of charge in the detector strips. The channel front-end main goal is to evaluate this amount of charge, coming from the corresponding strip of the detector. This is obtained by collecting the current pulses, at the input of the channel, and converting them into an analog voltage, which is subsequently digitized by an analog-to-digital converter. From these digitized values it is possible to understand which particle passed through the detector.

Requirements	value
Temperature	−40 °C
Power consumption	< 10mW/channel
input dynamic range	10 keV-50 MeV
Maximum ENE	4 keV (FWHM)
Minimum threshold	10 keV
Detector leakage current	max 50 nA @ 27 °C

Table B.11: GAPS ASIC requirements.

The GAPS front-end channel has been designed with a 180 nm CMOS technology [32]. Its schematic is shown in fig. B.37. The design has been carried out to target the experiment requirements reported in table B.11 [33, 34].

Injection circuit

The injection circuit generates a current pulse, whose amplitude is decided by the user, in order to simulate the release of charge due to the passage of particles through the GAPS Si(Li) detector. This block is used only during the test phase, because in the real experiment, the channels will be connected to the detector stripes. An injection capacitor C_{inj}, shown in fig. B.37, is integrated in each channel to generate the current pulse emulating the charge released in the detector. For each GAPS prototype (SLIDER4, SLIDER8 and pSLIDER32), a specific injection circuit has been designed. Each one of these is described in its corresponding section.

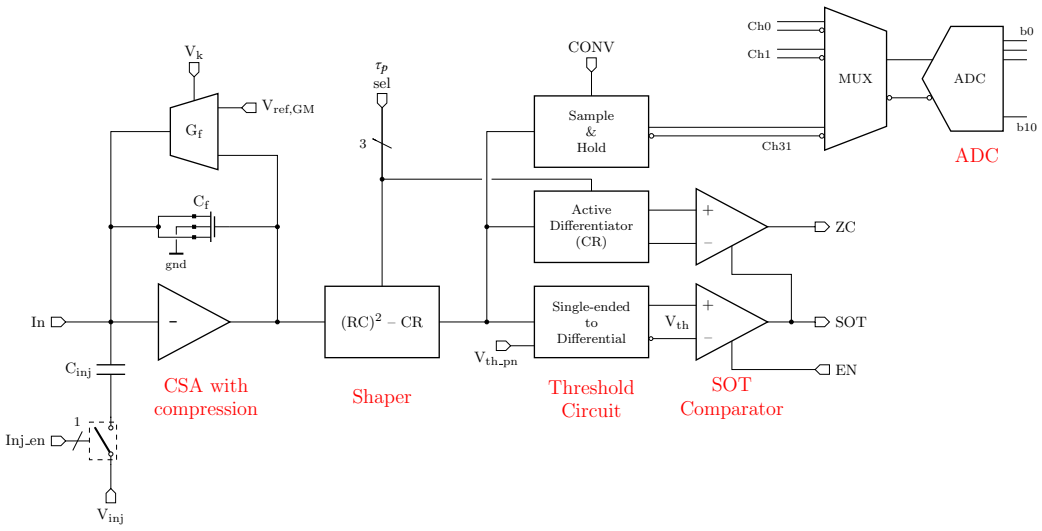

Figure B.37: front-end channel schematic.

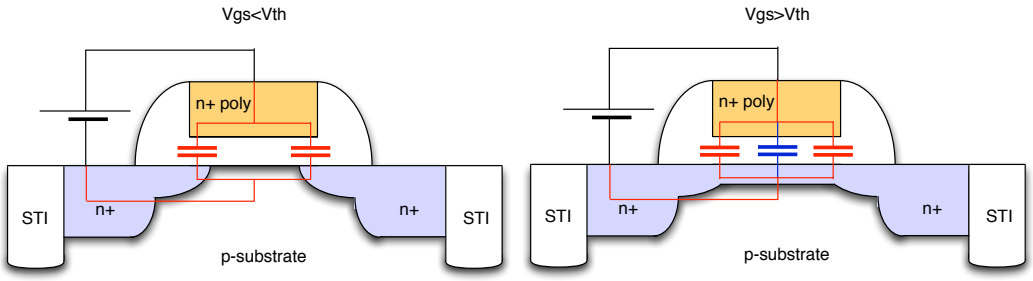

Figure B.38: nMOS capacitance variation. In the left image ($V_{gs} < V_{nMOS,th}$) only the *overlap* capacitors compose the nMOS capacitance. In the right image ($V_{gs} < V_{nMOS,th}$) the nMOS capacitance is composed of the sum of the *overlap* and the channel capacitors.

Charge Sensitive Amplifier with dynamic signal compression

The first block of the channel is the Charge Sensitive Amplifier. The aim of this block is to convert the current pulses coming from the detector into a voltage step, whose amplitude is proportional to area of the current pulse. The main feature of this block is its input-output trans-characteristic, which is characterized by signal dynamic compression. This a very important feature of the CSA because, in order to cover the large energy dynamic range required by the project specifications and to maintain a high resolution in the low energy range, a linear gain was not an option due to the high supply voltage and large number of bits required for this solution [14, 35].

The CSA has been designed with an active folded cascode (with a local feedback) loaded by an active cascode architecture. The reset is performed by a continuous time feedback implemented with a Krummenacher network. The dynamic compression has been performed using the nMOS capacitor C_f. In order to obtain an nMOS capacitor, the bulk is connected to ground, whereas the drain and source are short-circuited. The source-drain node and the gate node compose the two capacitor terminals.

This nMOS configuration permits to obtain a capacitor that changes its value according to the voltage applied to its gate. For low applied voltages ($V_{gs} < V_{nMOS,th}$) the nMOS capacitance is given by the *overlap* capacitors, namely the small capacitors that are formed between gate and the source and drain diffusions respectively. For high applied voltages ($V_{gs} > V_{nMOS,th}$), the nMOS capacitance is given by the *overlap* capacitors plus the capacitor between the generated channel and gate [14]. This behavior is shown in fig. B.38.

The CSA gain is inversely proportional to the nMOS feedback capacitance. This behavior is clearly visible in fig. B.39. So, the CSA transfer function can be considered bilinear, with a high gain for low energies and a low gain for high energies.

In the CSA architecture there is a transconductor, whose aim is to compensate the detector leakage current and to restore the nMOS capacitance after a certain amount of time after charge injection. The transconductor is designed using a Krummenacher network architecture. Moreover, a leakage current redout circuit has been implemented in order to measure the detector leakage current.

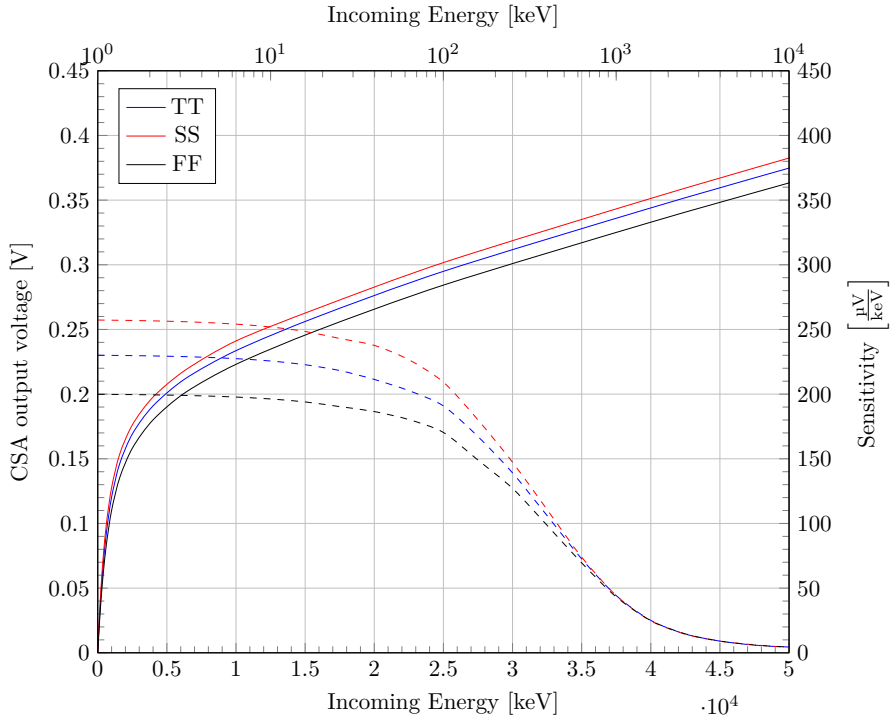

Figure B.39: the continuous lines represent the CSA output as a function of the charge injected (x-axis on the lower part of the image, y-axis on the left part). The dashed lines represent the CSA output sensitivity function of the incoming energy (x-axis on the upper part of the image, y-axis on the right part).

Time-invariant filter (CR-(RC)^2)

The second block of the GAPS channel is the shaper. This block's main goal is to improve the Signal-to-Noise ratio in order to obtain the required high energy resolution. It is composed of two stages: one CR stage (high-pass filter) and two RC stage (low-pass filter). Its shape permits to obtain a quicker return to the baseline than simpler architectures. In this way the typical $pile - up$ effect is avoided, where a subsequent signal sums to the residuals of the present signal. The Transfer Function of this block is

$$H(s) = \frac{R_2}{R_1} \cdot \frac{1}{1+s\tau} \cdot \frac{C_2}{C_1} \cdot \frac{s\tau}{(1+s\tau)^2} \tag{.27}$$

The shaper output is a unipolar semi-Gaussian function, characterized by a peaking time $t_p = 2 \cdot \tau$, where τ is the time constant of the circuit. The peaking time selection (3 bit) is obtained by switching four capacitors C_1, C_2, C_p and C_i. The Shaper output introduces a gain of 1.5 almost independent of the peaking time.

Threshold Generator and SOT comparator

The shaper output is connected to the threshold generator. The other two inputs are two threshold voltages called V_{tp} and V_{tn}. This block converts the single-ended signal at the output of the shaping stage to a differential signal. A differential threshold voltage is used to avoid crosstalk. The two output signals of the threshold generator are:

$$V_{th,out1} = v_{s0} + V_{tp} - \frac{V_{sh}}{2} \tag{.28}$$

$$V_{th,out2} = v_{s0} + V_{tn} + \frac{V_{sh}}{2} \tag{.29}$$

where V_{sh} is the shaper output voltage and v_{s0} is a threshold generator bias voltage. The differential signal obtained is

$$V_{th,out1} - V_{th,out2} = (v_{s0} + V_{tp} - \frac{V_{sh}}{2}) - (v_{s0} + V_{tn} + \frac{V_{sh}}{2}) \tag{.30}$$

$$= V_{tp} - V_{tn} - V_{sh}. \tag{.31}$$

The difference $(V_{tp} - V_{tn})$ can be expressed as V_{th}, which is the SOT comparator threshold. The two generated voltages are, in fact, connected to the SOT comparator. Its main goal is to suppress false event caused by noise or disturbances. The comparator fires when

$$V_{th,out2} > V_{th,out1}, \tag{.32}$$

or, more easily, when

$$V_{sh} > V_{th}. \tag{.33}$$

The behavior just explained is shown in fig. B.40, where:

- in the left images, the SOT comparator does not fire since its threshold is higher than the shaper output voltage ($V_{sh} < V_{th}$);
- in the right images, the SOT comparator has its output at logic 1 when the shaper output is higher than the SOT threshold ($V_{sh} > V_{th}$).

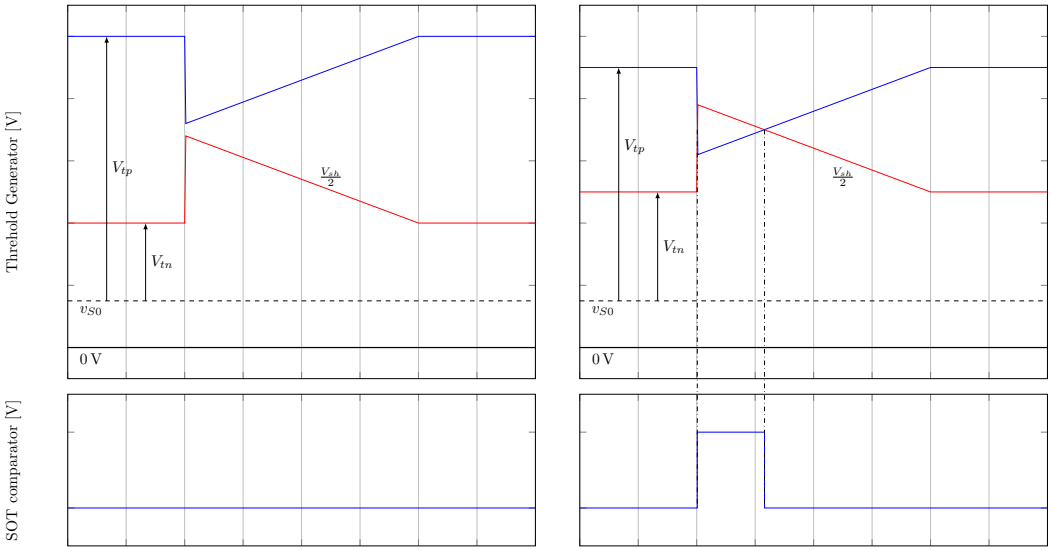

Figure B.40: examples of threshold generator and SOT comparator outputs as obtained by varying the threshold voltages V_{tp} and V_{tn}. In the diagrams on the left, the SOT comparator does not fire since $V_{sh} < (V_{tp} - Vtn)$. Otherwise in the diagrams on the right, the SOT comparator is at logic 1 when $V_{sh} > (V_{tp} - Vtn)$.

In the final ASIC, V_{tp} and V_{tn} are generated by means of an 8-bit DAC external to the channels. These voltages are then connected to the threshold generator of each channel. In order to compensate for process parameter variations of each channel threshold, in each one of these a 3-bit DAC for fine threshold trimming is added.

The *EN* signal visible in fig. B.37 permits to disable this block and, as a consequence, the SOT comparator output is always at logic 1.

Active CR differentiator and Zero Crossing comparator (ZC)

The differentiator task is to derive the shaper output, with a CR filter, in order to detect the exact shaper peaking time. When the shaper signal derivative is equal to zero, the shaper output is at its maximum voltage, namely its peaking time. The differentiator output is negated by this block and, in this process, a continuous voltage of $V_{dd}/2$ is added to the derivative signal. This voltage addition prevents that, if the derivative is less than 0 V, the differentiator output will be always at 0 V. The output of this block is then connected to the ZC comparator and compared with $V_{dd}/2$ voltage: when its voltage is greater than $V_{dd}/2$, the ZC output turns into a logic 1. This is the time when the shaper output has to be sampled, throughout the CONV signal, in order to retrieve the exact injected charge.

The ZC comparator works only if the SOT comparator voltage is at logic 1. This is done in order to easily discard false events caused by noise or external disturbances.

Single-ended to differential S&H

This block holds the shaper output voltage value when the signal CONV passes from logic 0 to logic 1. The CONV signal is equal to ZC when the front-end operates in self-trigger mode, instead, when it operates in non self-trigger mode, the CONV signal must be provided

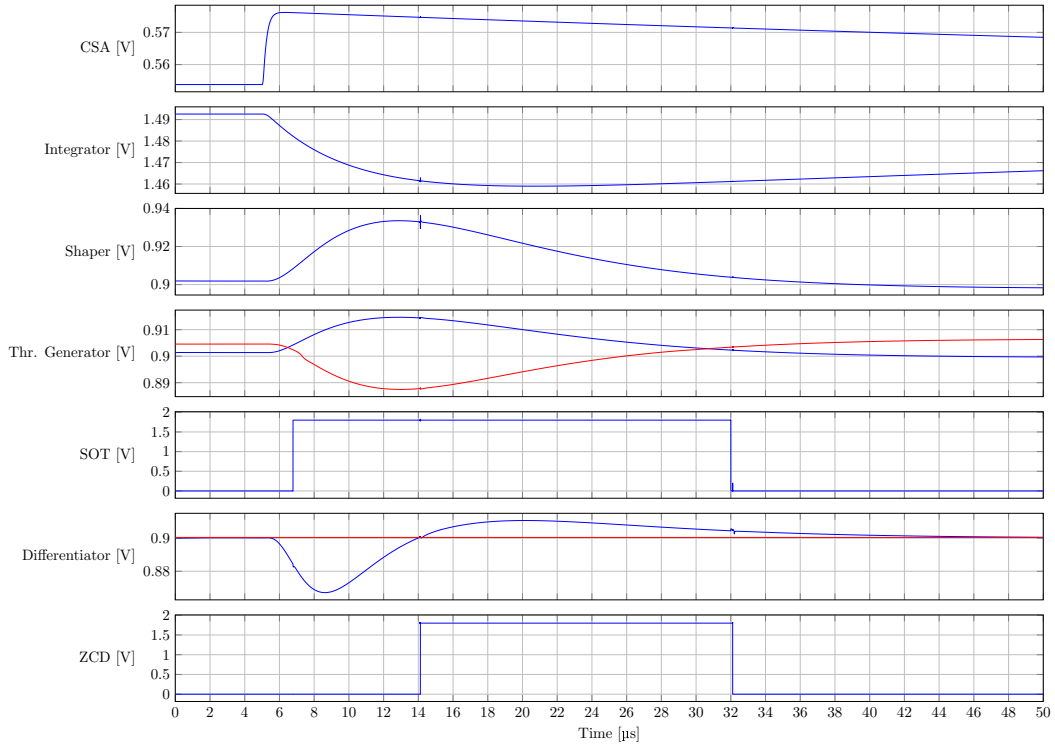

Figure B.41: all channel blocks signals for an incoming energy of 100 keV at −40 °C.

from an external source. This block introduces an additional 3.23 gain in SLIDER8 and 5.14 in pSLIDER32.

The sample & hold output is then connected to a multiplexer, and finally to an ADC used to digitize to voltage stored in it.

All the blocks signals are shown in fig. B.41 for an incoming energy of 100 keV at −40 °C.

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