Journal of Instrumentation

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To cite this article: G Aglieri *et al* 2013 *JINST* **8** C12041

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *November 15, 2013*
ACCEPTED: *December 3, 2013*
PUBLISHED: *December 23, 2013*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2013,
23–27 SEPTEMBER 2013,
PERUGIA, ITALY

Monolithic active pixel sensor development for the upgrade of the ALICE inner tracking system

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doi:10.1088/1748-0221/8/12/C12041

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ABSTRACT: ALICE plans an upgrade of its Inner Tracking System for 2018. The development of a monolithic active pixel sensor for this upgrade is described. The TowerJazz 180 nm CMOS imaging sensor process has been chosen as it is possible to use full CMOS in the pixel due to the offering of a deep pwell and also to use different starting materials.

The ALPIDE development is an alternative to approaches based on a rolling shutter architecture, and aims to reduce power consumption and integration time by an order of magnitude below the ALICE specifications, which would be quite beneficial in terms of material budget and background. The approach is based on an in-pixel binary front-end combined with a hit-driven architecture. Several prototypes have already been designed, submitted for fabrication and some of them tested with X-ray sources and particles in a beam. Analog power consumption has been limited by optimizing the Q/C of the sensor using Explorer chips. Promising but preliminary first results have also been obtained with a prototype ALPIDE. Radiation tolerance up to the ALICE requirements has also been verified.

KEYWORDS: VLSI circuits; Analogue electronic circuits; Radiation-hard electronics; Electronic detector readout concepts (solid-state)

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1 Introduction

For the upgrade of the Inner Tracking System [1] of ALICE at CERN a monolithic active pixel sensor is under development. The objectives of the upgrade are to record Pb-Pb collisions at 50 kHz and proton-proton collisions at 1 MHz, while improving the impact parameter resolution by a factor 3, and the standalone tracking efficiency and pT resolution. Fast insertion and removal is necessary to allow yearly maintenance. To achieve these objectives a new ITS layout is foreseen with 7 layers instead of 6, all equipped with monolithic sensors, while reducing:

1. The material budget or the radiation length per layer X/X_0 from 1.14 to 0.3 %
2. The pixel size from 425×50 to between 20×20 to 30×30 μm^2.
3. The radius of the first layer from 39 to 22 mm.

To reduce the radius of the first layer a beam pipe with outer radius of 19.8 mm is foreseen. Installation is planned for the Long Shutdown 2 of LHC currently foreseen for 2017–2018.

Important specifications (table 1) are integration time (<30 μs) and power consumption density (< 300 mW/cm^2). The ULTIMATE chip designed in a 0.35 μm CMOS process for the STAR experiment [2] achieves with a rolling shutter architecture 190 μs and 130 mW/cm^2 for a 20×20 μm^2 pixel. Splitting the pixel matrix in N equal sectors being read out in parallel in this architecture both reduces integration time and increases power density by a factor N. Therefore the product of power density and integration time is a good figure of merit. The ULTIMATE chip with 130 mW × 190 μs = 24700 nJ does not quite reach 300 mW/cm^2 × 30 μs = 9000 nJ. Also its radiation tolerance of 150 krad and a few 10^{12} 1MeV n_{eq}/cm^2 is below ALICE specifications

Table 1. Overview of the main specifications.

	Inner Barrel	Outer Barrel
Silicon thickness	50 µm	
Material thickness	0.3% X_0	0.8% X_0
Chip Size	15 mm x 30 mm	
Pixel Size	O(30 x 30) µm^2	O(30x30) ÷ O(50x50) µm^2
Integration Time	< 30 µs	
Power density	< 300 mW / cm^2	
Hit density (Pb-Pb)	~ 115 / cm^2	~ 1.5 / cm^2
Radiation Load (TID)	< 700 krad	< 10 krad
1 MeV n_{eq} fluency	1.1 x 10^{13} cm^{-2}	3 x 10^{10} cm^{-2}
Data throughputs	~1 Gbit sec^{-1} chip^{-1}	16 Mbit sec^{-1} chip^{-1}

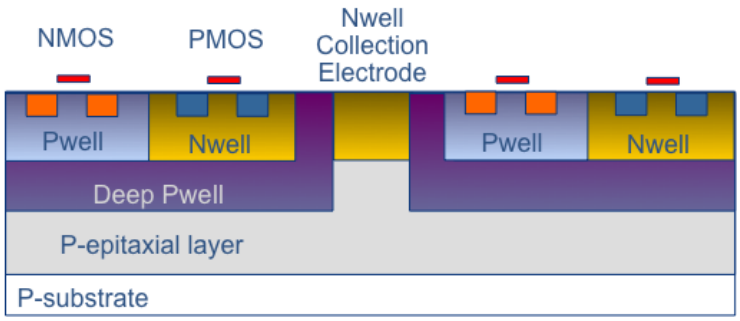

Figure 1. The deep pwell prevents the nwell containing PMOS transistors from collecting signal charge from the epitaxial layer and therefore allows full CMOS within the pixel.

(table 1). Therefore a deeper submicron CMOS technology was chosen for the ALICE ITS upgrade for improved transistor radiation tolerance [3], and development was started to also meet the other specifications. The TowerJazz 180 nm CMOS imaging sensor process [4] has been chosen as it is possible to use full CMOS in the pixel due to the offering of a deep pwell and also different starting materials. The deep pwell (figure 1) shields the nwell containing the PMOS transistors from the epitaxial layer and prevents it from collecting signal charge from the epitaxial layer instead of the nwell intended as charge collection electrode. The foundry also provides stitching to implement die larger than the reticle size. Transistor radiation tolerance well beyond ALICE requirements has been verified [5]. Figure 2 shows the drain current versus gate to source voltage before and after irradiation using 10 keV Xrays for a minimum size 1.8 V NMOS transistor. Only very small radiation-induced shifts can be observed up to a 10 Mrad(SiO_2) dose, which is well beyond the ALICE specification.

R&D on the monolithic sensor will be pursued during 2013–2014, with a full conceptual demonstration towards the end of 2013 and a production-ready prototype towards the end of 2014. Several developments based on rolling shutter architectures have been started, Mistral and Astral [6], and a continuation of the Cherwell development [7], and while they are expected to meet the ALICE specifications of integration time and power consumption, it would be very beneficial if the integration time could be reduced to only a few microseconds to obtain much less background, and if the power density could be reduced well below 100 mW/cm^2 to further reduce the material

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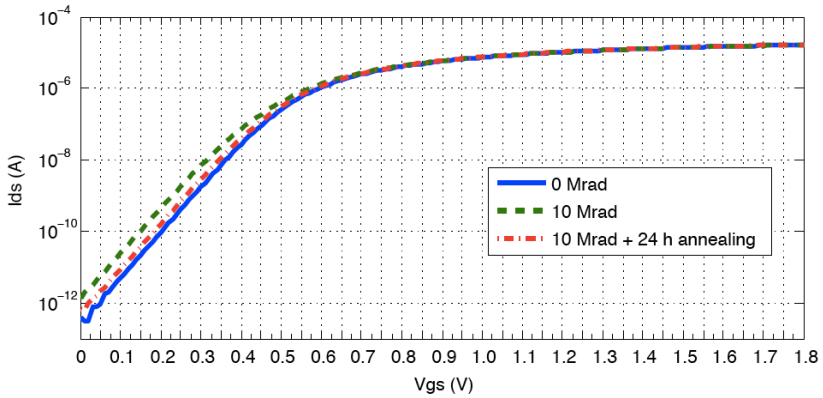

Figure 2. Log (ID) versus V_{gs} characteristic of a minimum size 1.8 V NMOS transistor before and after a 10 Mrad(SiO_2) 10 keV Xray irradiation.

in the detector. The ALPIDE (ALICE PIxel DEtector) development described further in this paper was started in an effort to lower integration time and power consumption down to these values. It is based on a low power front end (20.5nA/pixel) with data-driven readout. The integration time of only a few microseconds is determined by the shaping time of the front end.

Prototypes of several types of pixel matrices have been submitted and tested. The EXPLORER series has been designed to optimize the pixel sensor, which has a direct impact on the analog power consumption. The pALPIDE chip contains a first version of the low power front end and data-driven readout to validate the ALPIDE approach. In the following these prototypes will be described together with measurement results.

2 Explorer chips to optimize the sensor

2.1 Chip design

Analog power consumption is determined by the collected charge over capacitance (Q/C) ratio, requiring pixel sensor optimization [8]. An early prototype implemented on an 18 μm thick $>$1 kΩcm epitaxial layer in the chosen TowerJazz technology showed that changing the reset voltage of the detecting diode over a $\sim$1 V range drastically affects this Q/C ratio. A new prototype, the Explorer0 (figure 3), was submitted and measured [10], and allows reverse substrate bias similar to earlier ones in another technology [9]. It contains two matrices, a 90$\times$90 matrix of 20$\times$20 μm pixels and a 60$\times$60 matrix of 30$\times$30 μm pixels. Each matrix is divided in 9 sectors, equipped with pixels with varying size and geometry of the collection electrode and/or varying distance to the surrounding pwell as detailed in table 1. Each pixel is equipped with two analog storage elements. After resetting the pixel, the analog level of each pixel is stored in its first memory cell, and then after some time, the integration time, the analog level of each pixel is stored in its second memory cell. Thereafter a readout can be initiated to sequentially read all analog storage elements. This architecture allows correlated double sampling and also to decouple integration time from the readout time.

2.2 Explorer0 measurement results

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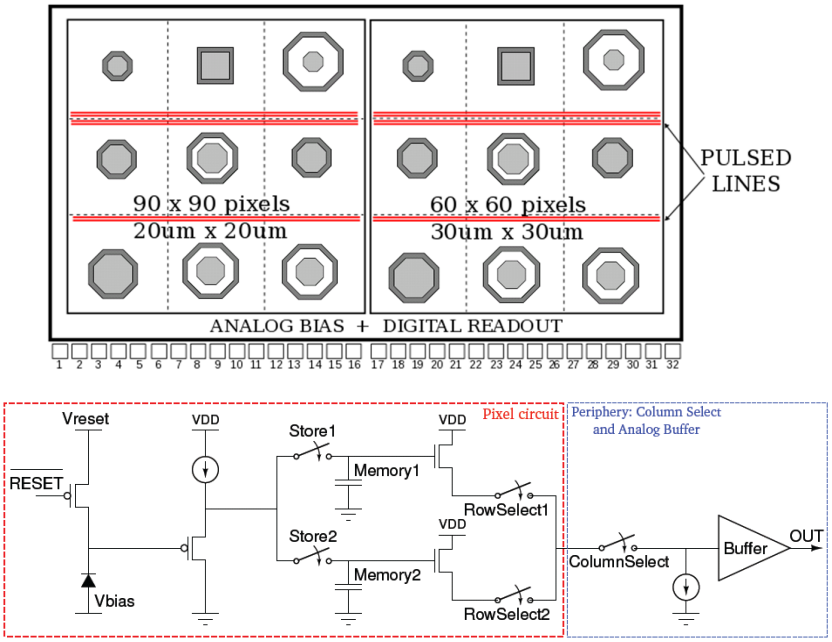

Figure 3. Floorplan (top) and schematic overview (bottom) of the Explorer prototype.

Table 2. Overview of the different sectors in the matrices in Explorer0.

Explorer0				Explorer1			
Sector	Shape	Diameter [µm]	Spacing [µm]	Sector	Shape	Diameter [µm]	Spacing [µm]
1		2	0	1		1.13	3.035
2		3	0	2		2	2.6
3		4	0	3		3	2.1
4		3	0	4		1.13	3.035
5		3	0.6	5		2	2.6
6		3	1.04	6		3	2.1
7		2	1.54	7		1.13	0.635 (top)
8		3	0	8		1.13	0.635 (top)
9		3	1.04	9		2	2.6

Measurements showed [10] reverse substrate bias reduces input capacitance and average cluster size, and increases efficiency for a certain charge threshold. Figure 4 shows the cluster signal for single pixel clusters and all clusters from a ^{55}Fe source and illustrates the influence of reverse substrate bias and also that some degradation in signal occurs after a 10^{13} n_{eq}/cm^2 radiation, but that the signal remains well separated from the noise. This was also further confirmed in a beam test with 4–6 GeV/c electrons.

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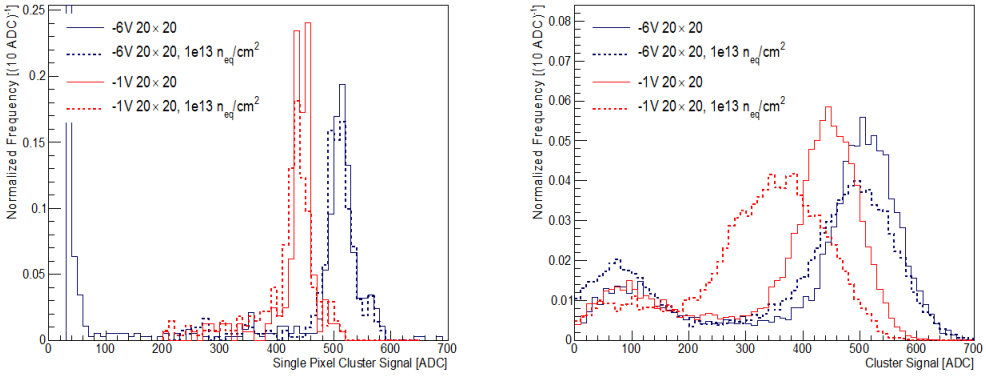

Figure 4. Signal for (a) single pixel clusters only and (b) for all clusters before and after irradiation.

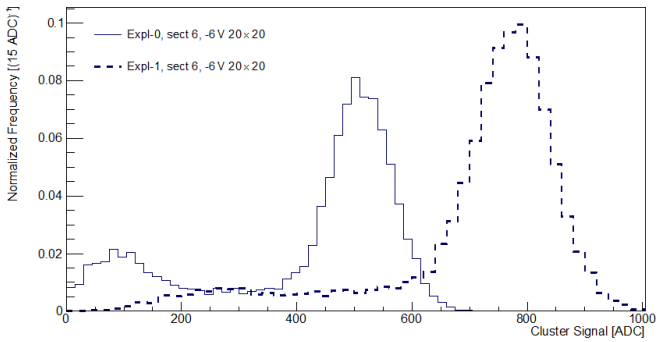

Figure 5. ^{55}Fe spectrum obtained by Explorer0 and Explorer1.

Analysis showed further sensor optimization could be done, both through design but also using different starting materials. It was also observed that Explorer0 was penalized by too large a circuit input capacitance, which was reduced from ∼5fF down to ∼2fF in a new version, the Explorer1, which came back from fabrication recently.

3 Explorer1 measurement results and comparison with Explorer0

Figure 5 shows the ^{55}Fe spectrum obtained by one of the best sectors in Explorer0 and in Explorer1, and illustrates the signal increase. Measurements confirmed no significant change in noise, therefore effectively increasing the signal-to-noise ratio with the same factor.

The improvement is further illustrated in figure 6 comparing efficiencies between Explorer0 and Explorer1, measured both in a 6 GeV/c electron beam. For Explorer0 the result is plotted for one of the sectors with the best performance, sector 6, with an octagonal collection electrode of 3 μm diameter and about 1 μm spacing to the surrounding pwell. For Explorer1 all sectors have been included, and the fake hit rate has been plotted as well. For Explorer1 about 1% of the pixels affected by random telegraph noise were masked. This has only a very limited effect on the efficiency since clusters typically consists of more than one pixel. The horizontal axis plots the charge threshold expressed in multiples of the measured rms value of the noise and it can be seen that the efficiency remains near 100% for Explorer1 up to much larger threshold values. The positive influence of reverse substrate bias can also be observed.

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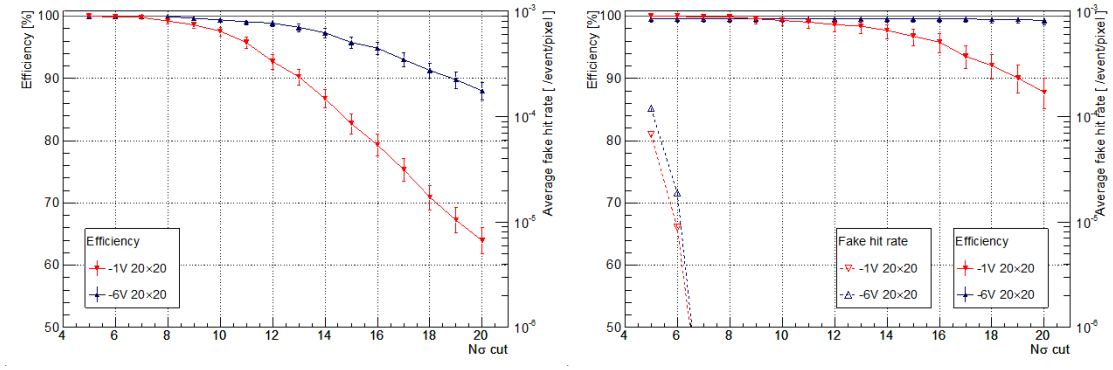

Figure 6. Efficiency in Explorer0 (left) and Explorer1 (right) in a 4–6 GeV/c electron beam.

4 ALPIDE development

4.1 General approach

The ALPIDE development is motivated by the benefits of reducing integration time and power consumption well beyond the ALICE specifications. As mentioned in the previous section, analog power consumption is significantly influenced by the Q/C ratio and thus by sensor optimization. Digital power consumption depends on the on-chip architecture and also on cluster size. As an alternative to the traditional rolling shutter architecture, the ALPIDE development investigates the use of a low-power in-pixel binary front-end in combination with a hit-driven readout. The binary front end is non-linear with a shaping time around 1–2 μs (for measured pulse shapes see figure 9). It is possible to send a trigger signal to the chip within that time after the event took place to allow hit pixels to write a 1 into their memory. After this hits can be read out sequentially by means of a priority encoder circuit, which provides the address of the first hit pixel in a sector, and subsequently resets it, so that during the next clock cycle the address of the next hit pixel is made available. This continues until all hits in the sector have been read out. Digital power is minimized as power is consumed only if hits are present. Very preliminary digital power estimates using this architecture are about 10 mW/cm^2 or less. Currently a full-scale prototype is under study, which should allow us to obtain a more precise number. The encoder is fully combinatorial and is structured as a tree where an element at one level implements the priority for four cells of the level below. A specific level therefore corresponds to two bits in the address, with the lowest level implementing the priority for four pixels and corresponding to the two least significant bits.

Figure 7 shows schematically how a full scale ALPIDE chip would be built: pixels are arranged in double columns, with a priority encoder per double column. This allows space to be used more efficiently for the priority encoder as it is routing dominated and several routing lines can be shared between the two columns. In fact, the pALPIDE prototype discussed below contains one priority encoder per column and figure 8 shows significant space is spent on routing. This guided the decision to opt for a priority encoder per double column in the full-scale chip. The pixel front end includes a storage element for hit information. At the periphery the chip is equipped with cluster information compression circuitry and a multi event memory. The final chip will also include a serializer to send the data off-chip.

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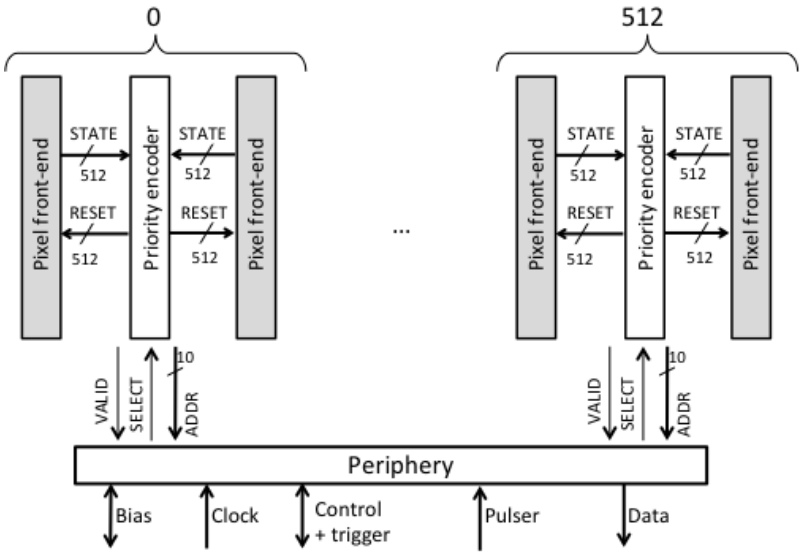

Figure 7. Schematic block diagram of a full scale ALPIDE chip.

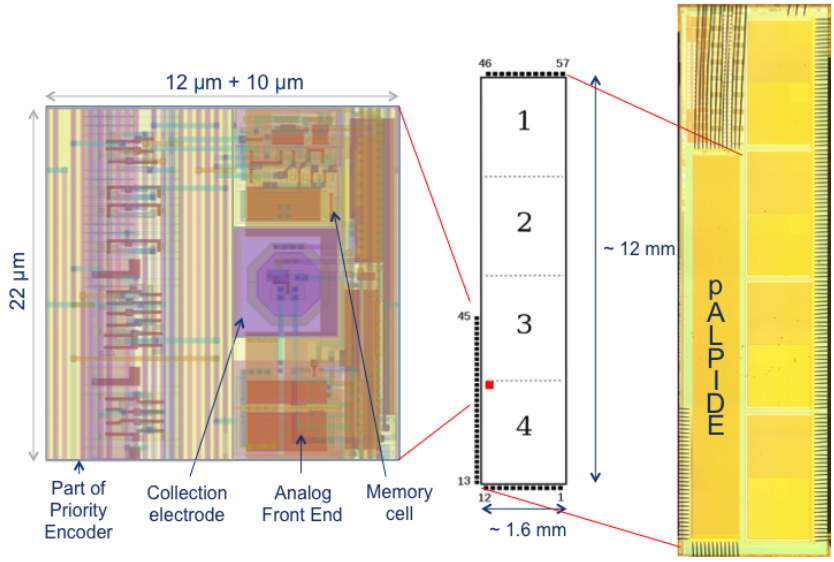

Figure 8. Die photograph of the pALPIDE with an illustration of its division in four sectors and a layout of a single pixel.

4.2 Prototype ALPIDE or pALPIDE

A prototype matrix with 64 columns and 512 rows, the pALPIDE, was submitted for fabrication. It is equipped with the ∼40nW in-pixel binary front-end circuit and a priority encoder per column, generated using a standard digital design flow with automated place and route. To fit the digital part into the pixel using this approach, the pixel size was slightly increased to 22 μm×22 μm. The prototype is divided in four sectors: sectors 1 and 2 contain a square collection electrode, and 3 and 4 an octagonal collection electrode. Both collection electrodes are of minimum size still fitting

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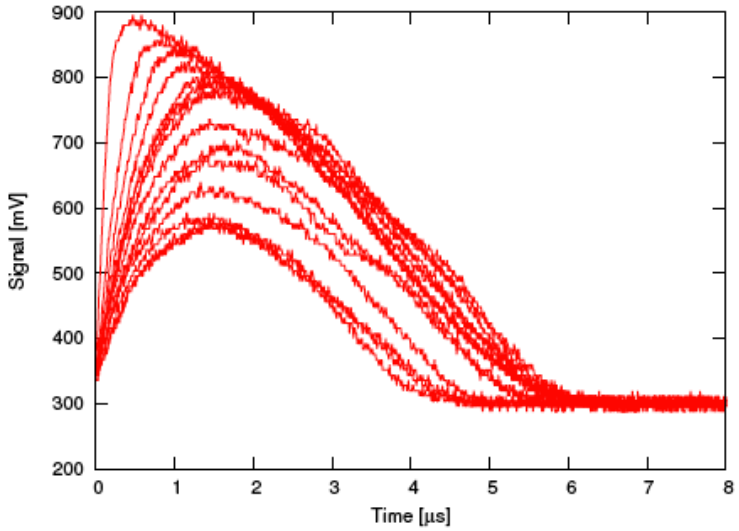

Figure 9. Analog output of the front end of one pixel under ^{55}Fe X-ray exposure.

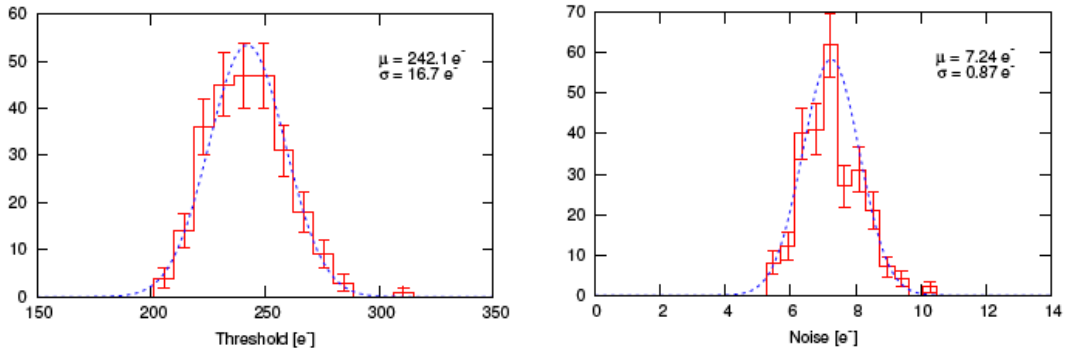

Figure 10. Measured threshold (left) and noise (right) distributions for the pixels in the pALPIDE.

input transistor and resetting diode. Pixels in sectors 2 and 3 are equipped with charge injection capacitors, but only for 4 rows these are connected to a pad allowing an external pulse, for all other rows the injection capacitor is grounded.

Figure 9 shows the analog output of the front end of one pixel under ^{55}Fe exposure. The response is non-linear, with a decreasing peaking time with increasing signal amplitude. The minimal detectable charge has been measured to be about 130 electrons. At nominal bias and threshold setting (20.5nA/pixel), pixel threshold and noise distributions were measured (figure 10). The measured threshold spread is 17 electrons and the average pixel noise is 7 electrons. These measurement results are preliminary and many things still need to be fully understood. One example is that simulated noise values, obtained by Monte Carlo simulations in the time domain, are a factor 2 higher than measured. No issue with random telegraph noise was observed on the pALPIDE.

4.3 Serializer and LVDS driver

The ALPIDE chip also needs to be equipped with a serializer and LVDS driver to send the data off-chip. Prototypes of the LVDS driver were submitted for fabrication, and first measurement results

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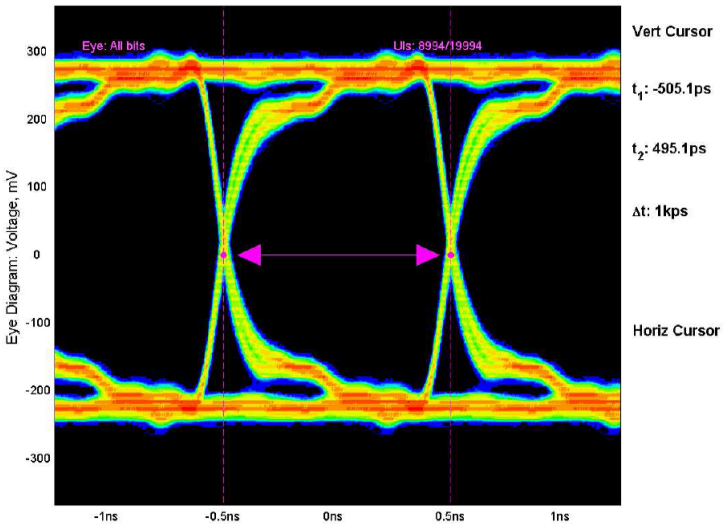

Figure 11. Eye-diagram obtained with an LVDS driver prototype.

have become available. Figure 11 shows an eye-diagram at 1 Gb/s of the output applying a pseudo random binary sequence for a bias current of 2 mA. A jitter below 10% of the unit interval has been measured illustrating the driver can exceed 1 Gb/s. The LVDS driver still needs to be combined with a serializer. Recent investigation has shown data rate requirements should not exceed 1 Gb/s.

5 Conclusions

The ALPIDE development towards a monolithic pixel sensor for the upgrade of the ALICE Inner Tracking System is described. As an alternative to approaches based on a rolling shutter architecture, this development aims to reduce power consumption and integration time by an order of magnitude below the ALICE specifications, which would be quite beneficial in terms of material budget and background. The approach is based on an in-pixel binary front-end combined with a hit-driven architecture. Analog power consumption ($\sim 40\,\mathrm{nW/pixel}$ or $< 10\,\mathrm{mW/cm^2}$) has been limited by optimizing the Q/C of the sensor. Digital power consumption is minimized using a priority encoder for reading the hit pixels. Preliminary first estimates of an upper limit on digital power are around $10\mathrm{mW/cm^2}$. If the ALPIDE approach is successful, data transmission off-chip could be the dominant power contributor, but if data rates can remain well below 1Gbit/s for a 1.5×3 cm^2 pixel sensor, this may no longer be the case. Explorer chips were designed to optimize the sensor, and measurements illustrate progress from one iteration to the next, and promising but preliminary results have also been obtained with a prototype ALPIDE. Radiation tolerance of sensor and transistors up to ALICE specifications has also been verified.

References

[1] L. Musa et al., *Conceptual design report for the upgrade of the ALICE ITS*, CERN-LHCC-2012-013 (2012).

[2] L. Greiner et al., *A MAPS based vertex detector for the STAR experiment at RHIC*, *Nucl. Instrum. Meth.* **A 650** (2011) 68.

2013 JINST 8 C12041

[3] G. Anelli et al., *Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects*, *IEEE Trans. Nucl. Sci.* **NS-46** (1999) 1690.

[4] S. Senyukov et al., *Charged particle detection performances of CMOS pixel sensors produced in a* 0.18 μ*m process with a high resistivity epitaxial layer*, *Nucl. Instrum. Meth.* **A 730** (2013) 115.

[5] H. Hillemans et al., *Total ionizing dose effects in* 180 *nm CMOS structures for Monolithic Active Pixel Sensors for the ALICE Inner Tracker System detector upgrade*, accepted for presentation at the *2013 Nuclear Science Symposium*, Seoul, Korea (2013).

[6] C. Hu et al., *MISTRAL & ASTRAL: two CMOS pixel sensor architectures dedicated to the Inner Tracking System of the ALICE experiment*, in *Topical Workshop on Electronics for Particle Physics 2013*, September 23–27, Perugia, Italy (2013).

[7] T. Nooney, *First results from Cherwell, a monolithic active pixel sensor for particle physics*, talk given at *EPS2013*, July 1–5, Finldand (2013)..

[8] W. Snoeys, *Monolithic pixel detectors for high energy physics*, *Nucl. Instrum. Meth.* **A 731** (2013) 125.

[9] S. Mattiazzo et al., *LePIX: First results from a novel monolithic pixel sensor*, *Nucl. Instrum. Meth.* **A 718** (2012) 288.

[10] C. Cavicchioli et al., *Design and characterization of novel monolithic pixel sensors for the ALICE ITS upgrade*, presented at the 9^{th} *international "Hiroshima" symposium on the development and application of semiconductor tracking detectors*, September 1–5, Hiroshima, Japan (2013), and submitted to *Nucl. Instrum Meth. A*.

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