Dynamic Compression of the Signal in a Charge Sensitive Amplifier: from Concept to Design

Massimo Manghisoni, *Member, IEEE,* Daniele Comotti, Luigi Gaioni, Lodovico Ratti, *Senior Member, IEEE,* and Valerio Re

***Abstract*—This work is concerned with the design of a low-noise Charge Sensitive Amplifier featuring a dynamic signal compression based on the non-linear features of an inversion-mode MOS capacitor. These features make the device suitable for applications where a non-linear characteristic of the front-end is required, such as in imaging instrumentation for free electron laser experiments. The aim of the paper is to discuss a methodology for the proper design of the feedback network enabling the dynamic signal compression. Starting from this compression solution, the design of a low-noise Charge Sensitive Amplifier is also discussed. The study has been carried out by referring to a 65 nm CMOS technology.**

***Index Terms*—Front-end, CMOS, dynamic signal compression.**

I. Introduction

SINCE many years, Charge Sensitive Amplifiers (CSAs) have been used extensively in reading out capacitive sensors such as particle and X-ray detectors. In a front-end system, the amplifier is followed by a shaping stage and a further processor which depends on the particular function the system needs to implement. In order to retain the charge information, the electrical signal at the output of the front-end channel is digitized to finally produce a digitally encoded measurement of the energy released in the detector by the incident radiation. The resolution of this system is limited by the noise of the charge preamplifier, as the first stage of the analog processing chain, and by the number of bits of the analog-to-digital converter (ADC). In applications where a high resolution is required, suitable noise performance must be implemented in the charge preamplifier. On the other hand, such a high resolution cannot be preserved over the entire input signal range, since an excessively high number of bits would be necessary. The solution typically adopted consists of providing the system with a non-linear input/output characteristic, resulting in a change of the channel sensitivity with the input signal amplitude. The way in which this is achieved is not trivial. As an example, in the AToM chip developed for the readout of the silicon strip detector of the BaBar experiment, the Time-over-Threshold (ToT) technique has been adopted with the purpose of retaining the information of the charge induced on each strip with a limited number of bits [1]. This is a compression-type, non-linear transformation of the amplitude at the shaper output into a time variable, represented by the duration of the signal at the output of a discriminator. Such duration is converted into a number by classical techniques of time-to-digital conversion.

A compression technique is mandatory, in particular, in the design of front-end electronics developed for Free Electron Laser (FEL) experiments. In this application, covering the wide (1 to 10^4 photons @ 1 keV to 10 keV) input dynamic range while preserving single photon resolution at small signals is one of the most challenging tasks. In order to fit this dynamic range into a reasonable output signal swing, a strongly non-linear characteristic is required. Several systems are currently under investigation for applications to the experiments at the Eu-XFEL [2]. In the DEPFET Sensor with Signal Compression (DSSC) [3] the non-linear characteristic is achieved at sensor level by exploiting the feature of the DSSC device. In the frame of the DSSC collaboration, other solutions, in which the signal compression is obtained at front-end level, have been recently proposed in [4], [5]. In the LPD (Large Pixel Detector), project three channels with different gains are read out in parallel. The one with the highest gain and not saturated is then selected offline [6]. In the AGIPD (Adaptive Gain Integrating Pixel Detector) front-end channel, a dynamic gain switching technique is used [7]. In the Percival (Pixellated Energy Resolving CMOS Imager, Versatile and Large) detector, based on CMOS monolithic sensor technology, a dynamic gain switching is implemented in each channel [8].

In this work an alternative solution, based on the non-linear features of a MOS capacitor [9] in the feedback loop of a charge-sensitive preamplifier, is proposed. Starting from this compression solution, a complete analog readout channel, suitable for application at the next generation FEL experiments, has been developed in the framework of the PixFEL Project [10]. The study has been carried out by considering a 65 nm CMOS technology, since this node appears to be the more robust and promising solution to cope with the unprecedented requirements set by silicon vertex trackers in High Energy Physics experiments upgrades and future colliders as well as by imaging detectors at light sources and free electron lasers [11].

The paper is organized as follows. In Section II, some details of the study are introduced. Section III treats the way in which a CSA feedback network featuring signal compression is designed. Finally, in Section IV, the design of a low-noise CSA for FEL applications is discussed.

Massimo Manghisoni, Luigi Gaioni and Valerio Re are with Università di Bergamo, Dipartimento di Ingegneria e Scienze Applicate, Viale Marconi 5, I-24044 Dalmine (BG), Italy and INFN, Sezione di Pavia, Via Bassi 6, I-27100 Pavia, Italy, (phone: +39 035 2052359; email: massimo.manghisoni@unibg.it).

Daniele Comotti and Lodovico Ratti are with Università di Pavia, Dipartimento di Ingegneria Industriale e dell'Informazione, Via Ferrata 1, I-27100 Pavia, Italy and INFN, Sezione di Pavia, Via Bassi 6, I-27100 Pavia, Italy.

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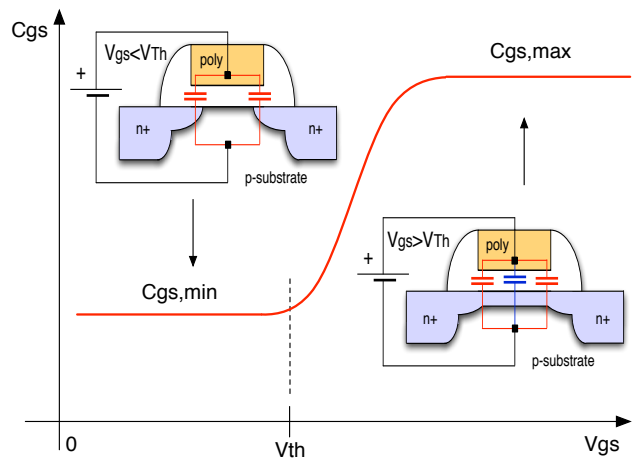

Fig. 1. Qualitative behaviour of the C_{gs} capacitance as a function of the V_{gs} voltage for an inversion-mode NMOS capacitor with fixed gate width W. The substrate contact (not shown) is at GND.

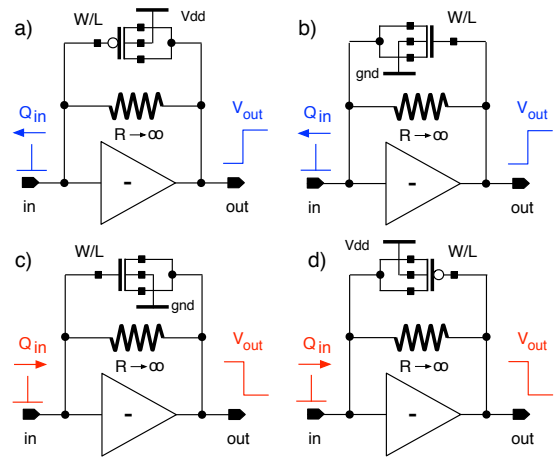

Fig. 2. Charge sensitive preamplifier with MOS non-linear feedback capacitor. The device type (NMOS or PMOS) is determined by the gate connection and by the detector signal polarity.

II. Design details

The study discussed in this work has been carried out by referring to a Low Power (LP) 65 nm CMOS process developed for mixed-signal and RF applications and provided by Taiwan Semiconductor Manufacturing Company (TSMC). It features a high-resistivity epitaxial substrate, shallow trench isolation (STI), two gate oxide options for core and I/O devices, n+ and p+ polysilicon gate materials. The process supports deep n-well devices, as well as low (LVT), standard (SVT), and high (HVT) threshold voltage options. The back-end of line offers 4 to 9 metal layers. With respect to the other flavors commonly available for CMOS technologies, such as the General Purpose (GP) and High Speed (HS), the LP variant shows an increased supply voltage V_{DD}=1.2 V and a higher equivalent oxide thickness t_{ox}≈2 nm for the core devices we have considered, which leads to a reduced gate leakage current. The study has been performed by considering operation at room temperature, T=27°C.

III. Dynamic compression with MOS capacitor

A. Inversion-mode MOS capacitor

In the design of microelectronic circuits, MOS transistors may be used for the implementation of capacitive elements. For this purpose, drain and source of the device are shorted together to form one capacitor terminal whereas the gate forms the other. The value of the resulting capacitance, denoted here as C_{gs}, depends on the voltage between the gate and the source-drain terminal V_{gs} and varies non-linearly as the MOSFET is biased through accumulation, depletion and inversion region. One way to obtain a monotonic function of C_{gs} is by ensuring that the transistor does not enter the accumulation region for all the values of V_{gs}. This is accomplished by connecting the bulk to the lowest voltage available in the circuit (the GND reference) for an NMOS device or the n-well to the highest voltage (the power supply V_{DD}) for a PMOS. In this way, the device can only operate in inversion mode and yields the qualitative C_{gs}-V_{gs} characteristic shown in Fig. 1. This characteristic is non-linear and monotonic with a relatively sharp transition occurring for V_{gs} values approaching the threshold voltage V_{Th} of the device. For $0<V_{gs}<< V_{Th}$ the value of C_{gs} is set at its minimum and it is mainly due to the overlap of the gate dielectric with the source and drain diffusions. For $V_{gs}>>V_{Th}$ a conductive channel appears under the gate oxide and C_{gs} shows a maximum value which is mainly given by the gate-to-channel C_{gc} capacitance. The values of $C_{gs,min}$ and $C_{gs,max}$ depend on the device geometry, whereas the V_{gs} value at which the transition occurs depends on the threshold voltage V_{Th} [12].

B. Dynamic signal compression

In response to a delta-like current signal, a CSA with a capacitive feedback network generates an output voltage step whose amplitude is proportional to the input charge and with a sensitivity given by the inverse of the feedback capacitance. Therefore, the non-linear feature of the inversion-mode MOS capacitor can be exploited to dynamically change the gain of a CSA with the input signal amplitude, thus providing a dynamic signal compression. For this purpose, the MOS capacitor is used as the feedback network of the charge sensitive amplifier, as shown in Fig. 2. In the preliminary stage of this discussion, an ideal block is considered. Moreover, a large resistance is included in the feedback network for DC restoration, setting to zero the gate-to-source voltage of the feedback device when no input signal is applied.

In principle, either a PMOS or an NMOS can be used as the feedback device. Also the gate terminal can be connected either to the input or to the output of the gain stage. Device polarity and orientation must be chosen in relation with the detector characteristics to obtain a capacitance which increases with the input signal amplitude, then leading to a reduced gain for the larger values of detected charge. For a detector collecting electrons, a positive voltage step is expected at the amplifier output in response to an input pulse charge. For this type of detector, either a PMOS with the gate terminal connected to the amplifier input, Fig. 2.a), or an NMOS with

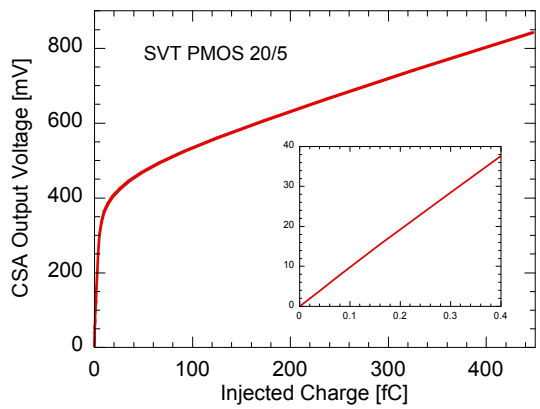

Fig. 3. Simulated input-output trans-characteristic of a CSA with a W/L=20 μm/5 μm SVT PMOS feedback device. The inset shows the initial, high gain portion of the characteristic.

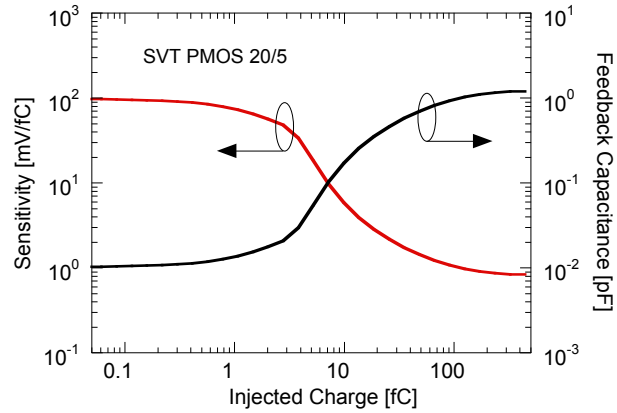

Fig. 4. Simulated Charge Sensitive Amplifier sensitivity and equivalent feedback capacitance as a function of the injected charge for a CSA with a W/L=20 μm/5 μm PMOS feedback device.

the gate connected to the amplifier output, Fig. 2.b), can be used. On the contrary, since a detector collecting holes generates a negative voltage step at the amplifier output, either an NMOS with the gate terminal connected to the amplifier input, Fig. 2.c), or a PMOS with the gate connected to the amplifier output, Fig. 2.d), is needed. With these choices, the gate connection of the feedback device is always at a higher, for NMOS, or lower, for PMOS, potential with respect to the source-drain one. It is worth noting that, to fully exploit the output dynamic range of the CSA, the input voltage must be properly fixed: close to GND for PMOS and close to V_{DD} for NMOS feedback devices. For this purpose, the polarity of the preamplifier input device must be chosen accordingly. A PMOS is needed for a detector collecting electrons, whereas an NMOS is used for one collecting holes. For the sake of simplicity, in the following discussion we consider only the solution proposed in Fig. 2.a). However, the results can be easily extended to the other proposed configurations.

As an example, the simulated input-output trans-characteristic of a CSA with an SVT PMOS feedback device with W/L=20 μm/5 μm is shown in Fig. 3. The CSA output voltage V_{out} is the amplitude of the voltage step occurring at the amplifier output in response to a delta-like input current signal. The inset shows the initial, high gain portion of the characteristic. The transfer function is almost bilinear with a higher sensitivity region for low values of the injected charge and a lower sensitivity for higher values of the injected charge. The transition starts to occur for values of the output voltage approaching the threshold voltage of the feedback MOS.

The gain of the Charge Sensitive Amplifier is not constant any more and depends on the value of the injected charge Q_{inj}. By referring to the definition of charge sensitivity

$$S_q(Q_{inj}) = \frac{dV_{out}}{dQ_{inj}} \tag{1}$$

an equivalent feedback capacitance C_{ef} can be derived as the inverse of the CSA gain

$$C_{ef}(Q_{inj}) = S_q(Q_{inj})^{-1}. \tag{2}$$

The plots of the amplifier charge sensitivity and of the relevant equivalent feedback capacitance, obtained for the transfer function of Fig. 3, are reported in Fig. 4. For low values of the injected charge, the feedback device exhibits an equivalent capacitance of 10 fF with an amplifier sensitivity of 100 mV/fC. At the highest values of the injected charge, the capacitance reaches a maximum value of 1 pF and the sensitivity of the amplifier falls to 1 mV/fC.

C. Feedback network design methodology

In the design of a charge amplifier, the input-output transfer function must be chosen to comply with the requirements of the specific application. These requirements concern:

- the sensitivity for low values of the injected charge;
- the maximum input dynamic range;
- the maximum voltage headroom at the amplifier output.

To comply with these specifications, the feedback device dimensions, W and L, must be properly chosen. Moreover, the more suitable threshold voltage, V_{Th}, must be selected among the ones commonly available for nanoscale CMOS technologies. In what follows, we provide a methodology for the proper choice of these values and for the design of a more sophisticated feedback network.

1) Sensitivity for low input charge (S_{lq}): If we assume that low values of the injected charge generate an output voltage step with amplitude V_{out} much lower than the device threshold V_{Th}, then the equivalent feedback capacitance C_{ef} is set at its minimum and it is mainly due to the parallel of the overlap gate-to-source $C_{gs,ov}$ and gate-to-drain $C_{gd,ov}$ capacitances:

$$C_{ef,min} \approx C_{gs,ov} + C_{gd,ov} = 2W\Delta L C_{ox} \tag{3}$$

where W is the channel width, ΔL is the extension of the overlap region and C_{ox}=ε_{ox}/t_{ox} is the gate oxide capacitance per unit area. According to (2), the relevant sensitivity of the amplifier for low values of the input charge S_{lq} is given by the following equation:

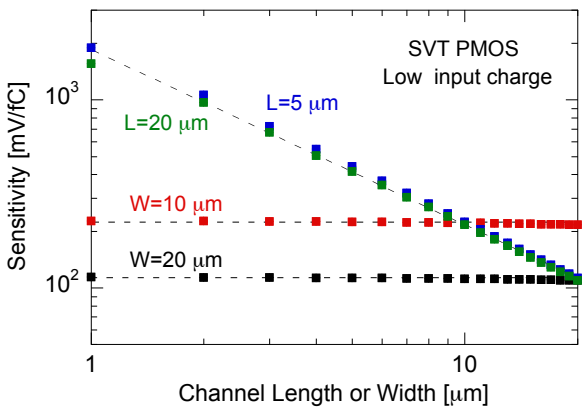

Fig. 5. Simulated sensitivity at low input charge, for SVT PMOS feedback devices, as a function of the channel length (for a fixed width) and as a function of the channel width (for fixed lengths).

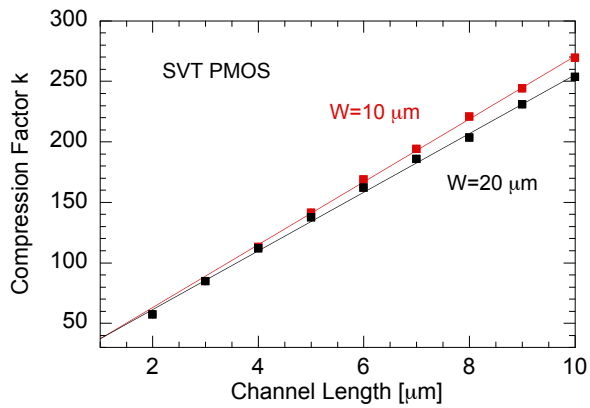

Fig. 7. Simulated signal compression factor k as a function of the channel length for two PMOS feedback devices with different channel widths W=20 μm and W=10 μm.

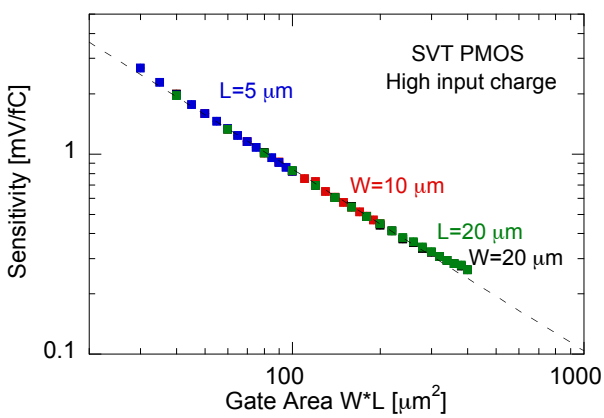

Fig. 6. Simulated sensitivity at high input charge, for SVT PMOS feedback devices, as a function of the device gate area for different values of the device channel length and widths.

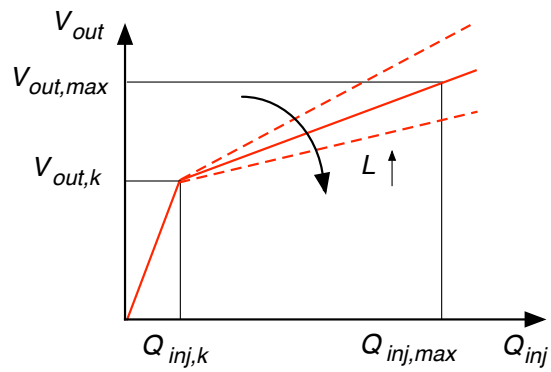

Fig. 8. Piecewise linear approximation of the transfer function. Once W has been properly chosen to set the sensitivity at low input charge, the gain for high values of the injected charge depends only on the channel length L and decreases with the increase of L.

$$S_{lq} = \frac{1}{2\Delta L C_{ox}} \frac{1}{W}. \tag{4}$$

Therefore, in this region, the gain of the preamplifier is independent of the MOS channel length L and can be adjusted by carefully choosing the channel width W. Fig. 5 shows the simulated S_{lq} sensitivity, for SVT PMOS feedback devices, as a function of the channel length (for a fixed width) and as a function of the channel width (for fixed lengths). As expected, the gain is independent of the channel length, whereas it is proportional to the inverse of the channel width.

2) Sensitivity for high input charge (S_{hq}): For high values of the injected charge, the amplitude of the output voltage step is expected to exceed the threshold, thus showing a maximum of C_{ef} which is mainly given by the gate-to-channel C_{gc} capacitance

$$C_{ef,max} \approx C_{gc} = WLC_{ox}. \tag{5}$$

The relevant amplifier sensitivity is given by

$$S_{hq} = \frac{1}{C_{ox}} \frac{1}{WL}. \tag{6}$$

Therefore, for high values of the injected charge, the gain depends on the MOS gate area WL and can be set with a suitable design of the MOS channel length L, once W has been properly chosen to set the sensitivity at low input charge. In Fig. 6 the simulated gain for SVT PMOS feedback devices is reported as a function of the device gate area for different values of the channel length and width. In agreement with the behaviour predicted by equation (6) the gain is proportional to the inverse of the device gate area. It is useful to define a signal compression factor k as the ratio of the sensitivity at small and large values of the input signals:

$$k = \frac{S_{lq}}{S_{hq}} = \frac{L}{2\Delta L}. \tag{7}$$

According to the definitions of S_{lq} and S_{hq}, provided by (4) and (6) respectively, k depends only on the channel length L. This is confirmed by the results shown in Fig. 7 where the simulated signal compression factor k is reported as a function of the channel length for SVT PMOS feedback devices with different channel widths. It is worth noting that if

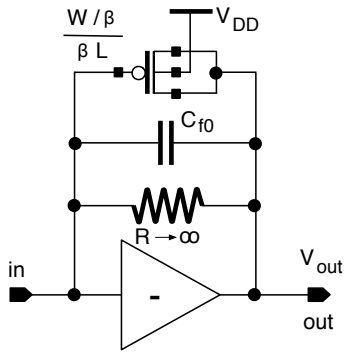

Fig. 9. Improved feedback network with a MOS device, scaled by a factor of β, and an additional fixed capacitance C_{f0}.

we approximate the transfer function with a piecewise linear characteristic, with S_{lq} and S_{hq} slopes, as shown in Fig. 8, the signal compression factor must be fixed according to the following equation to comply with the input and output dynamic range requirements:

$$k = \frac{Q_{inj,max} - Q_{inj,k}}{V_{out,max} - V_{out,k}} S_{lq} \approx \frac{Q_{inj,max}}{V_{out,max} - V_{Th}} S_{lq} \quad (8)$$

where $V_{out,max}$ is the voltage headroom at the CSA output, $V_{out,k} \approx V_{Th}$ is the voltage at which the kink, i.e., the change in slope, occurs, $Q_{inj,max}$ is the input dynamic range and $Q_{inj,k}$ is the value of the input charge at the kink ($Q_{inj,k} << Q_{inj,max}$). As a consequence, once S_{lq} has been fixed to comply with the required sensitivity, S_{hq} must be fixed in agreement with the following equation:

$$S_{hq} = \frac{V_{out,max} - V_{Th}}{Q_{inj,max}}. \quad (9)$$

3) A remark about the gain accuracy: Since the sensitivities, S_{lq} and S_{hq}, depend on W, L and t_{ox}, the gain might be affected by mismatch parameter variations. This effect is critical, in particular, for the sensitivity at low input charge S_{lq}. In applications where this variation might be a concern, such as in multielectrode semiconductor detectors, an additional capacitance C_{f0} in parallel to the feedback MOS can be introduced, as shown in Fig. 9. Among the different passive capacitances available in nanoscale processes, the one adopted for the implementation of C_{f0} must be of a type which is less sensitive to mismatch variations with respect to the MOS capacitance. Its value can be chosen in agreement with the following equation

$$C_{f0} = \left(1 - \frac{1}{\beta}\right) C_{ef,min} \quad (10)$$

where β>1 is a free parameter to be set by the designer considering that the higher the value of β, the larger the additional capacitance C_{f0} and the lower the inaccuracy due to the feedback MOS. Moreover, to preserve the value of the sensitivity in both the high and low gain regions, the

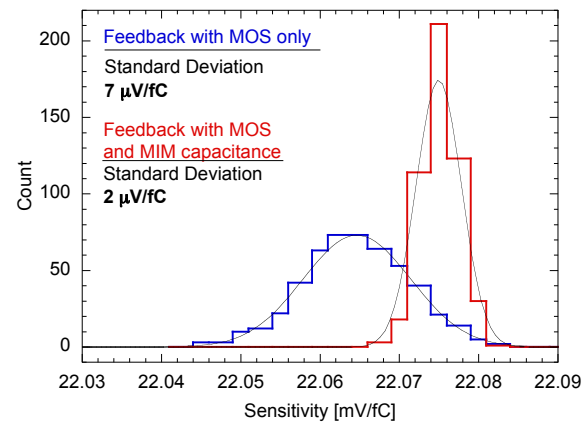

Fig. 10. Dispersion of the sensitivity at low injected charge, for a feedback SVT PMOS with W/L=100 μm/1 μm and for an improved network with an additional C_{f0}=35 fF MIM capacitor and a scaled MOS with W=20 μm and L=5 μm.

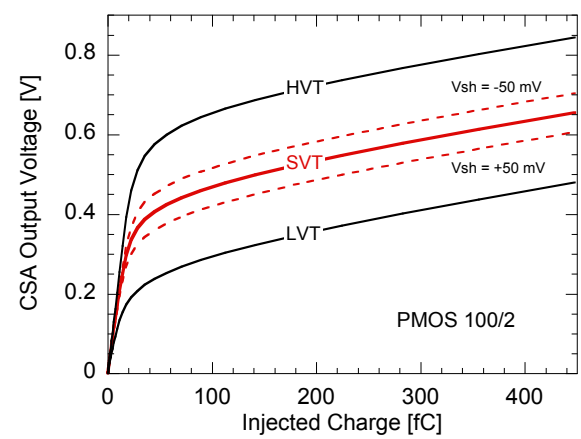

Fig. 11. Simulated trans-characteristic of a CSA with a W/L=100 μm/2 μm PMOS feedback device. Results for low, standard and high threshold voltage devices are reported. The effect of a ±50 mV voltage shift applied by a transconductor is also shown for the SVT device.

dimensions of the feedback MOS must be scaled according to the following rules:

$$W \rightarrow \frac{W}{\beta} \quad \text{and} \quad L \rightarrow \beta \cdot L \quad (11)$$

As an example, Fig. 10 shows the mismatch occurring for a feedback network realized with a SVT PMOS only with W/L=100 μm/1 μm and the one obtained for an improved version designed with β=5, that is with an additional C_{f0}=35 fF MIM capacitor and a scaled MOS with W=20 μm and L=5 μm. While the mean value of the gain is almost unchanged, the dispersion on the simulated sensitivity is improved by about a factor of 4.

The passive capacitance provides an additional benefit. Since C_{f0} is insensitive to the bias conditions, it is not the case for the MOS capacitance, it improves the linearity of the transfer function in the low input charge region where C_{f0} is dominant on the overall feedback capacitance.

4) Transition between high and low sensitivity region: The transition between the high and the low sensitivity region

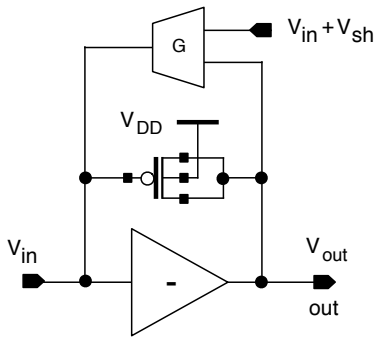

Fig. 12. Feedback network with additional transconductor for continuous time reset. One terminal of the device can be used to apply a voltage shift on the feedback MOS. This shift enables a precise variation of the voltage at which the kink occurs.

starts to occur for values of the output voltage approaching the threshold of the device. V_{Th} is a parameter which, apart from the slight dependence on the channel length, is almost constant. Nonetheless, for nanoscale CMOS technology, manufacturers usually supply MOS transistors with low, standard and high threshold voltage. This feature provides an additional degree of freedom in the choice of the feedback device, which can be exploited, in particular, in the shift of the value of the input charge at which the kink between high and low sensitivity occurs. This is shown in Fig. 11, where the simulated transfer function of a CSA with a W/L=100 μm/2 μm PMOS feedback device is reported for LVT, SVT and HVT options.

In addition, for such applications where the reset of the feedback capacitance is performed by a continuous time network implemented with a transconductor, as shown in Fig. 12, an additional voltage shift can be applied to the feedback MOS which enables a precise variation of the voltage at which the kink occurs. As an example, the effect of a $\pm$50 mV shift is shown in Fig. 11 for the SVT device.

As a last remark, the threshold voltage of a MOS device is strongly affected by temperature variations. Therefore, the design of the feedback device should take into account the temperature conditions foreseen for the envisioned application. Alternatively, a solution for temperature compensation must be implemented.

5) Some remarks about the feedback MOS orientation: As shown in Fig. 2 the gate terminal of the feedback MOS can be connected either to the input or to the output of the gain stage. A thorough evaluation of the best solution to be adopted should take into account the specific application. However, the following remarks must be borne in mind.

The switching of the gate connection forces to change also the device polarity. PMOS and NMOS exhibits slightly different values of the threshold voltage, the gate oxide thickness and the overlap region extension. These differences impact on the transfer function.

The source-to-body voltage V_{SB}, affects the threshold V_{Th} and, in turn, the voltage at which the transition between the high and low sensitivity starts to occur. It exhibits a different behaviour in the two orientations. It is fixed, and lower, if the gate of the feedback MOS is connected to the amplifier output, whereas it is higher and dependent on the injected charge, if the gate is connected to the amplifier input.

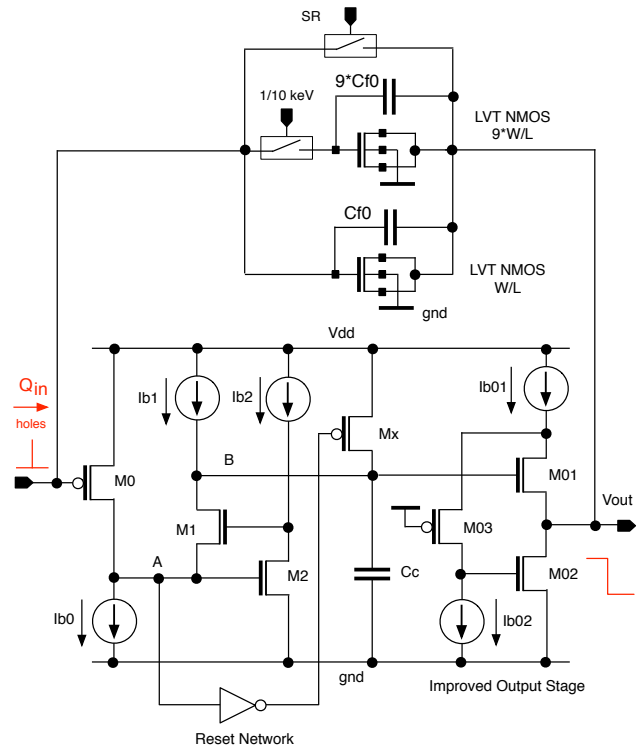

Fig. 13. Schematic diagram of the Charge Sensitive Amplifier with dynamic signal compression.

One last remark also concerns the different capacitors affecting the MOS device. Source-to-substrate C_{JSB} and drain-to-substrate C_{JDB} junction capacitances as well as the gate-to-substrate C_{GB} capacitance may shunt either the input or the output node of the amplifier, depending on the adopted configuration. Therefore, they might impact in different ways on the stability and, most important, on the noise performance of the amplifier.

IV. Low-noise CSA for FEL applications

A low-noise Charge Sensitive Amplifier with dynamic signal compression has been designed for application at future X-ray FEL experiments. This work has been carried out in the frame of the PixFEL Project [10] funded by the Istituto Nazionale di Fisica Nucleare (INFN), Italy. In the envisioned application, the device will be connected via bump-bonding to a fully depleted planar active edge P-on-N silicon detector [13], with a pixel pitch of 100 μm and delivering a signal ranging from 1 to 10^4 photons with energies from 1 keV to 10 keV. The simplified schematic diagram in Fig. 13 shows that the circuit is designed around a forward gain stage consisting of an active folded cascode, with a local feedback, loaded by an active load. The hole collecting pixel sensor forces the polarity of the input device M_0 to be of the P-channel type, as explained in Section III-B. It features gate dimensions of W_0/L_0=40 μm/0.15 μm and a standing

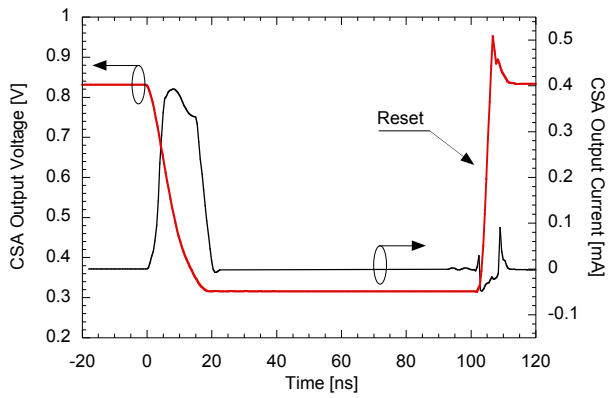

Fig. 14. Simulated transient response of the CSA output voltage and output current for an input signal of 10^4 photons at 10 keV collected in 15 ns. A reset signal is applied 100 ns after the input pulse.

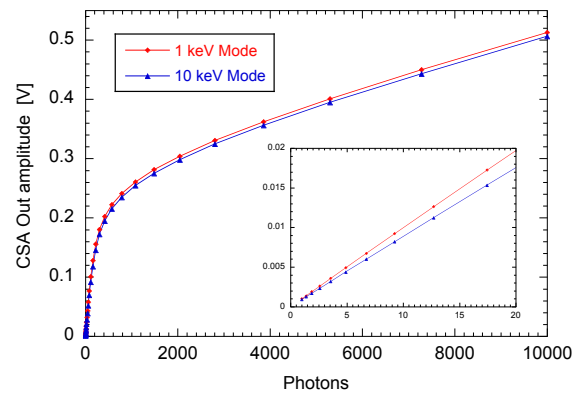

Fig. 15. Simulated input-output trans-characteristic of the CSA with dynamic compression. The inset shows the initial, high gain portion of the characteristic.

current of 45 μA, because of which it can be considered to work in a condition of moderate inversion with a channel transconductance of g_{m1}=0.90 mA/V. It has to be noted that operating the device in the weak-inversion region would provide an enhanced g_m/I_D ratio, whose potential benefit is a smaller channel thermal noise. However, this choice is not completely free since the DC gate voltage of the input device M_0 fixes the bias point of the amplifier output node, and, as a consequence, the one of the high impedance node B of the folded cascode.

An LVT NMOS with the gate connected to the amplifier input has been used as the non-linear feedback element. Starting from the compression idea proposed above, a more complex network has been worked out in which the MOS is split in two devices with the same channel length L=4 μm and with a channel width which is W=10 μm in one transistor and 9 times larger in the other. Such a feature has been introduced to make the channel capable of processing photon signals at 1 keV and 10 keV. Moreover, two additional capacitances C_{f0}=30 fF and 9·C_{f0} have been included to allow for precise setting of the sensitivity in the high gain region. These dimensions have been chosen to get a sensitivity of 1 mV/ph for a low number of incoming photons (with1 photon at 1 keV generating a charge of 277 electrons) and to fit the wide input dynamic range into an output voltage swing of 500 mV.

An improved output stage follows the complementary cascode. The large capacitive value reached by the feedback element, as high as 20 pF for 10^4 photons at 10 keV, together with the relatively short collection time in which the energy is deposited in the sensor, as low as 15 ns [14], leads to very large current pulses to be sunk by the amplifier during the maximum negative transient response. This sets very demanding requirement for the design of the output stage. The standard PMOS source-follower, indeed, is not adequate since its gate-to-source voltage would severely limit the negative output voltage swing. Therefore, an improved output stage has been adopted as shown in Fig. 13 [15]. Transistor M_{01} acts as a source-follower, whereas M_{02} acts as a controlled current sink providing a path for the current from the feedback capacitance to ground. The current provided by M_{02} is controlled by the negative feedback loop given by M_{01}, M_{02} and M_{03}.

An additional challenge we faced in the design of the proposed amplifier is represented by the circuit limitations in the reset phase. Charge restoration is accomplished by a voltage controlled switch in parallel with the feedback MOS. During the reset phase following a large input current pulse, the input voltage of the source follower has the same large positive swing as the amplifier output. The charge of the compensation capacitance C_c is slew rate limited by the standing current in the complementary cascode active load I_{b1}, with this current usually kept at a minimum to increase the DC gain of the stage. Since in applications at future FEL facilities the fixed operation timing implies a reset time in the range of few ns, a dynamic slew rate correction circuit, inverter and transistor M_X in Fig. 13, has been introduced [16] to overcome this limitation. During the signal integration phase, the low voltage at node A keeps the inverter output at V_{DD} and the transistor M_X in the off state. During a slew limited operation, the standing current of the load transistor is entirely fed to node B to charge up the compensation capacitance. As a consequence, while the cascode transistor carries minimal current, the voltage at node A rises thus switching on the transistor M_X and providing extra current to charge up the compensation capacitance.

The forward gain stage of the amplifier features an open-loop DC gain of 60 dB and a gain-bandwidth product (GBP) of 140 MHz with a power consumption of 100 μW at V_{DD}=1.2 V. The phase margin has been evaluated for zero detector capacitance and considering the full range of capacitive values assumed by the feedback MOS. The worst case, in terms of stability, is given by the highest value of the capacitance, corresponding to about 20 pF for a 10^4 photons at 10 keV, for which a value of 70 degrees is obtained, thus ensuring the stability of the system over the entire input range.

The performance of the amplifier has been evaluated for the overall input range of 10^4 photons at 1 keV and 10 keV. Fig. 14 depicts the simulated transient response of the stage for a detector signal collected in 15 ns and with a pulse amplitude of 10^4 photons at 10 keV. Moreover, a reset signal is applied 100 ns after the input pulse. The transition time of

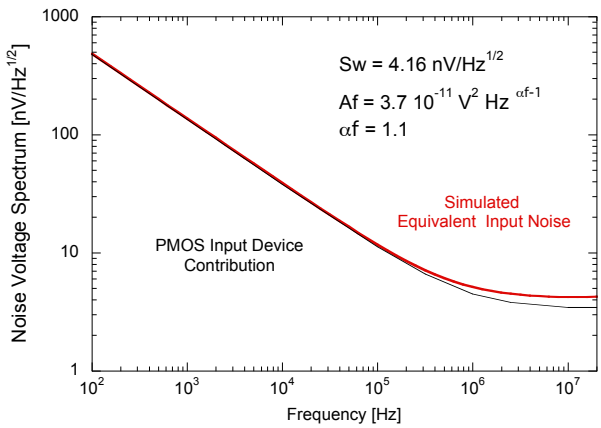

Fig. 16. Simulated equivalent input noise voltage spectrum of the charge sensitive amplifier.

the amplifier, intended here as the time taken by the signal to change from the 10% to the 90% of the voltage step, is in the order of 12 ns. Moreover, the amplifier comes to a complete reset in less than 20 ns thus proving the effectiveness of the dynamic slew correction circuit. In the same plot, the current sunk by the output stage is shown. The short collection time and the full voltage swing of 500 mV translate into a total sunk current of about of 0.4 mA, which proves the functionality of the improved output stage.

Fig. 15 shows the input-output trans-characteristic of the CSA for 1 keV and 10 keV photons operation mode. As expected, it exhibits a bilinear shape with a transition of the sensitivity occurring at an output voltage of about 250 mV and corresponding to a collected charge of about 500 ph. The sensitivity for the first 20 photons is about 1 mV/ph, as shown in the inset, and decreases to 25 μV/ph at 10^4 incoming photons.

One of the requirements set for analog processors in FEL applications is the capability of ensuring single photon resolution at small signals. This constraint requires that suitable noise performance be implemented in the charge preamplifier as the first stage of the analog processing chain. The simulated equivalent input noise of the amplifier is shown in Fig. 16 together with the noise contributed by the PMOS input device, which is the dominant part. In the frequency range between 10 Hz and 20 MHz, the noise voltage spectrum exhibits a $1/f$-like component at low frequency and a white noise component at high frequency, and can be modeled according to the following equation

$$S_e^2(f) = S_w^2 + \frac{A_f}{f^{\alpha_f}} \tag{12}$$

where the first term, S_w^2, accounts for the frequency independent contribution whereas the second one represents the flicker noise and depends on the intensity coefficient A_f. The α_f frequency exponent has been added to account for the deviation from the ideal $1/f$ power spectral density slope. From the noise voltage spectrum depicted in Fig. 16, the following values for the above mentioned coefficients have been extrapolated: S_w=4.16 nV/$\sqrt{Hz}$, A_f=3.7$\cdot 10^{-11}$ V^{2}Hz$^{\alpha_f-1}$ and α_f=1.1.

To evaluate the single photon capability of the amplifier, its noise performance has been expressed in terms of Equivalent Noise Charge (ENC) according to the following equation [17]:

$$ENC^2 = C_T^2 \left[\frac{A_1}{\tau} S_w^2 + (2\pi)^{\alpha_f} A_2(\alpha_f) A_f \tau^{\alpha_f - 1} \right] \tag{13}$$

where C_T is the total capacitance shunting the input node, A_1 and A_2 are the filter coefficients depending on the shape of the weighting function and τ is the shaping time of the readout filter. Parallel noise from the feedback network is not considered in (13) since its contribution to the overall ENC is negligible. To be consistent with the timing structure of the FEL laser (macro bunches of light pulses separated from each other by 220 ns in the case of the European XFEL laser), a time-variant shaping stage with a trapezoidal weighting function (A_1=2, A_2=1.38) and with an integration time τ=55 ns has been considered. Moreover, a value of C_T=240 fF has been extracted from simulation results, of which 70 fF are contributed by the detector and by the bump bonding stray capacitance [10]. With this choice, the ENC contributed by the charge sensitive amplifier is about 50 electrons (with a slope of 156 e$^-$/pF), thus leading to a Signal-to-Noise Ratio SNR=5.6 and making the stage compatible with single photon resolution at 1 keV.

V. Conclusion

This work discussed the design of a low-noise Charge Sensitive Amplifier featuring an active signal compression implemented at feedback level by exploiting the non-linear features of an inversion-mode MOS capacitor. Beside proving the effectiveness of this solution, the paper discussed a methodology for the proper design of the feedback network featuring an input-output transfer function complying with the requirements set by the specific application. Compression capability, together with improved output and reset stages, makes the device suitable for application to the next generation of X-ray FEL experiments. The amplifier, which has been designed in a 65 nm CMOS technology and takes an area of 85$\times$34 μm^2, has been included in a readout channel with a pixel pitch of 110 μm in the first prototype chip designed by the PixFEL Collaboration [10]. The design of an 8$\times$8 matrix has been submitted for fabrication and a characterization campaign will start as soon as the chip will be delivered by the foundry.

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