Total dose effects on deep-submicron SOI technology for Monolithic Pixel Sensor development

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Abstract

We developed and characterized Monolithic pixel detectors in deep-submicron Fully Depleted (FD) Silicon On Insulator (SOI) technology. This paper presents the first studies of total dose effects from ionizing radiation performed on single transistor test structures. This work shows how the substrate bias condition during irradiation heavily affects the resulting radiation damage.

I. Introduction

SOI technology employs standard CMOS integrated circuits fabricated on a thin Silicon layer, electrically insulated from the rest of the silicon wafer by means of a thick oxide layer (Buried Oxide, BOX). This approach gives several advantages over the standard bulk CMOS technology: the small active volume and the lower junction capacitance allow designs with higher latch-up immunity, higher speed and lower power consumption.

Moreover, being the electronics insulated from the substrate, it becomes possible to use a high resistivity substrate as sensitive volume for particle tracking and imaging. The possibility to deplete the sensor layer greatly improves the charge collection efficiency. Vias etched through the oxide connect the substrate to the electronics layer, so that pixel implants can be contacted and a reverse bias can be applied.

A monolithic pixel detector in SOI technology has several features which are appealing for its potential use in the inner volume of the CMS Tracker at SLHC. Unlike Hybrid Pixel Detectors, being both the detector and its front end electronics integrated in the same substrate, there is no need of the expensive bump bond process. The monolithic approach also reduces the material budget of the detector and makes the detector assembly and handling much easier. When compared to other kind of monolithic detectors (i.e. MAPS), a pixel with a depleted sensitive volume features a higher radiation tolerance to displacement damage and allows faster readout speed (as charge is collected by drift and not by diffusion).

However, SOI technology is well known to be prone to total dose damage due to the presence of the thick BOX, where positive charge gets trapped. In this work we will study the total dose tolerance of SOI technology under working conditions when used as particle detector.

II. Chip production

A first prototype chip, named LDRD-SOI-1, was obtained in 2007 in the OKI 0.15µm Fully Depleted (FD) SOI technology. This chip has been widely tested and characterized [1], [2]. As the 0.15µm process was not optimized for low leakage current, it was no longer adopted for the following chip productions.

A second prototype sensor, the LDRD-SOI-2 chip, was designed and fabricated in 2008 in the OKI 0.20µm FD-SOI process, optimized for low leakage current. This process features a full CMOS circuitry implanted on a 40nm thin Silicon layer on top of a 200nm thick BOX. The thickness of the CMOS layer is small enough for the layer to be FD at typical operational voltages. The sensor substrate is 350µm thick and has a resistivity of 700Ω·cm; it is thinned to 250µm and plated with a 200nm thin Al layer that allows back-biasing.

The chip is 5×5mm^2 with an active area of 3.5×3.5mm^2 divided into 168×172 pixels of 20µm. The pixel matrix is subdivided into a 40×172 pixel section with a simple, analog 3T architecture, and a 128×172 pixel section with a digital architecture providing a binary output. In the latter, two capacitors are integrated in each pixel for in-pixel Correlated Double Sampling (CDS), and a digital latch is triggered by a clocked comparator with a current threshold, which is common to the whole section. The chip design has been optimized to allow readout up to a 50MHz clock frequency, and the binary section is equipped with multiple parallel outputs for high frame rate.

A potential limitation of the SOI technology comes from the transistor back-gating effect. The reverse bias of the silicon substrate, necessary to deplete the sensitive volume, increases the potential at the silicon surface, so that the BOX acts as a second gate for the CMOS electronics on top. This typically causes a shift in the transistor threshold as a function of the increasing depletion voltage This was investigated with TCAD simulations and the most effective design found to limit the back-gating problem was a floating p-type guard-

ring around each pixel, which was implemented in the chip; two floating guard-rings also separate the peripheral electronics and I/O logic from the pixel matrix and from the pad area. This chip is currently under test [3].

III. ELECTRICAL CHARACTERIZATION OF LDRD-SOI-2

I-V and C-V measurements have been performed on the LDRD-SOI-2 detector, to extract both the breakdown voltage and the depletion depth of the sensitive volume, as a function of the backside voltage.

The I_{back}-V_{back} measurement (Figure 1), performed keeping at 0V the two external guard-rings, shows a breakdown occurring at $V_{back} \sim 85V$.

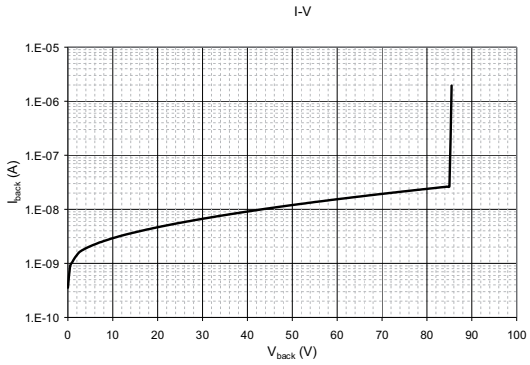

Figure 1: I_{back}-V_{back} measure on LDRD-SOI-2.

The C-V measure was performed on the chip by keeping at 0V the p-type implantation guard-ring around each pixel (which forms a grid all over the sensor) and by applying an increasing voltage to the backside, to deplete the whole sensitive volume under the BOX. With the knowledge of the area of the depleted volume and with the measure of the capacitance at a certain V_{back}, we could calculate the corresponding depletion depth (W). In Figure 2 we compare the so measured W with the value expected for a substrate with a nominal resistivity of 700Ω·cm. The measured value is a factor 2 lower than expected; this might indicate that the actual resistivity is slightly lower than the nominal value.

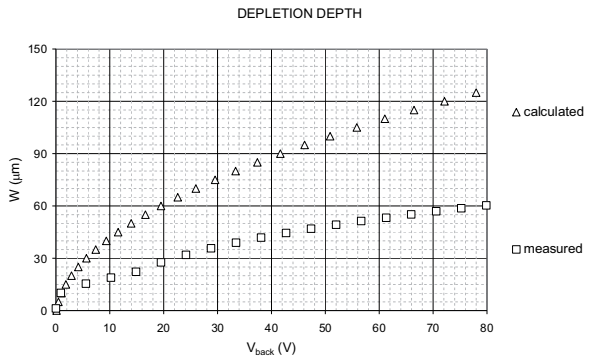

Figure 2: Comparison between the expected and the measured values of the depletion depth as a function of V_{back}.

IV. TOTAL DOSE STUDIES

A. Depletion voltage and Fractional Yield

In SOI technology, the thick buried oxide is expected to be very sensitive to ionizing radiation due to positive charge trapping, and a consequent increase of the top-gate leakage current. This effect is even larger when this technology is used to build monolithic radiation detectors. In fact, when a depletion voltage is applied to the sensitive volume (substrate), a strong electrical field is present across the BOX. When exposed to ionizing radiation, electron-hole pairs are created inside the thick oxide. The electrical field immediately separates these charges, which do not recombine; this greatly increases the amount of positive charge trapped throughout the BOX. The number of electron-hole pairs escaping recombination ("fractional yield") depends both on the bias given to the substrate and on the stopping power of the incident particle (Figure 3) - the higher the ionization density, the higher the recombination probability.

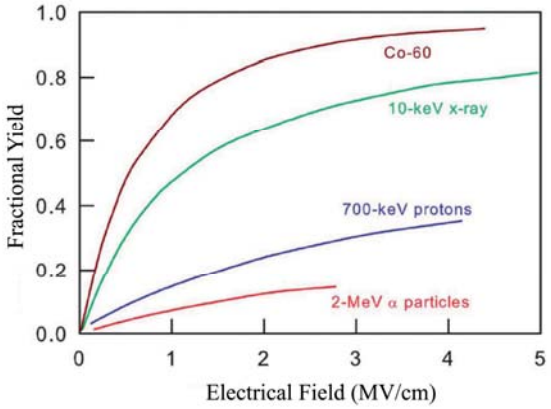

Figure 3: Fractional yield as a function of the electrical field applied throughout the oxide and for different incident particles [4], [5].

Previous works have been already carried out to study the total dose damage on monolithic pixel detectors fabricated in 0.15μm Fully Depleted (FD) SOI technology [6] in fixed bias conditions (transistor terminals floating). In our work we will study the total dose tolerance of OKI 0.20μm technology under different bias conditions during irradiation. This will allow a better understanding of the effects of the substrate voltage in real working conditions.

B. Irradiations on 0. 20μm process

We performed the studies described in this paper at the total dose test facility located at the INFN National Laboratory of Legnaro (Italy). The facility is equipped with the RP-149 Semiconductor Irradiation System from Seifert (Ahrensburg, Germany) which uses a standard tube for X-ray diffraction analysis (maximum power 3000 W, maximum voltage 60 kV, tungsten anode) [7]. The irradiations are performed in air, at room temperature and with a dose rate of 165rad(SiO_2)/sec.

The total dose studies have been carried out on test structures kindly provided by KEK (Japan). They consist of

16 NMOS and 16 PMOS transistors, with gates and drains separated and with common sources. Each transistor is surrounded by 1µm PSUB ring. For both NMOS and PMOS transistors, 8 are Body Float type and the remaining 8 have the body with different kinds of connection. In their turn, each set of 8 structures features both core and I/O transistors with threshold voltages (V_{thr}) and W and L values varying according to Table 1 and Table 2.

Table 1: Body Float Type.

Tr	L (µm)	W (µm)	Comment
M1	0.20	100	Core, normal V_{thr}
M2	0.50	250	Core, normal V_{thr}
M3	1.00	500	Core, normal V_{thr}
M4	0.20	100	Core, low V_{thr}
M5	0.50	250	Core, low V_{thr}
M6	1.00	500	Core, low V_{thr}
M7	0.35	175	I/O, high V_{thr}
M8	0.35	175	I/O, low V_{thr}

Table 2: Body Connection Type.

Tr	L (µm)	W (µm)	Comment
M9	0.20	100	Core, normal V_{thr}, Source Tie
M10	0.50	250	Core, normal V_{thr}, Source Tie
M11	1.00	500	I/O, Source Tie
M12	0.20	100	Core, normal V_{thr}, Body Tie
M13	0.50	250	Core, normal V_{thr}, Body Tie
M14	1.00	500	Core, normal V_{thr}, Body Tie
M15	10	100	I/O, D-NMOS
M16	10	100	I/O, D-NMOS, Source Tie

For Body Tie transistors M12, M13 and M14, the voltage for the body can be externally supplied by a connection pad. Each signal is directly connected to a pad without any protection diode, making the transistors very sensitive to electrostatic discharges.

During irradiation the transistors are in ON state, corresponding to the worst-case bias condition (the drain and the source of each transistor were kept to 0V, while the gate was kept HIGH for NMOS, LOW for PMOS). We irradiated the test structures at three different values of depletion voltage: V_{back} = 0V, 5V, 10V. In these first test, the PSUB guard-ring surrounding each pixel is kept floating, both during irradiation and during measurements, while the external body contact (for M12, M13 and M14) is kept grounded during irradiation and floating during measurement (no significative differences were found in the transistors characteristics if this contact is kept grounded during measurements).

Different transistors show different behaviors when exposed to X-ray radiation; some seem to be promising with regards to their total dose hardness.

The most radiation tolerant behaviour has been found in transistor M13 NMOS, whose I_{ds}-V_{gs} characteristics are displayed in Figure 4, Figure 5 and Figure 6.

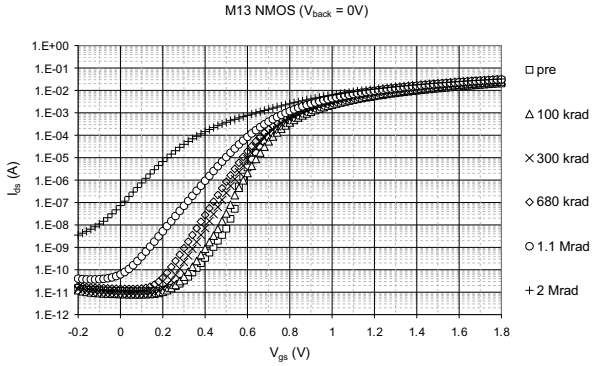

Figure 4: I_{ds}-V_{gs} curve for the M13 NMOS transistor before and after irradiation at V_{back} = 0V (up to a total dose of 2Mrad).

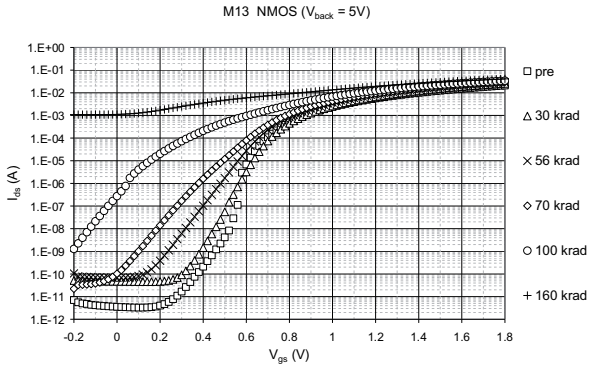

Figure 5: I_{ds}-V_{gs} curve for the M13 NMOS transistor before and after irradiation at V_{back} = 5V (up to a total dose of 160krad).

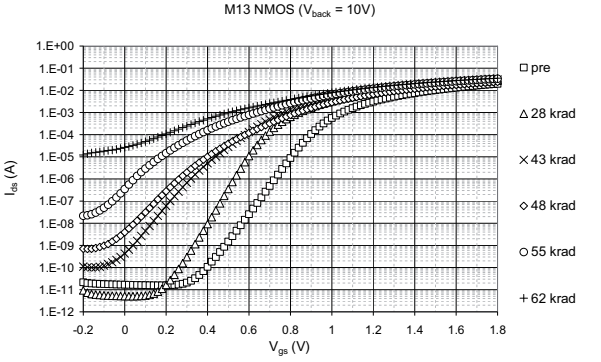

Figure 6: I_{ds}-V_{gs} curve for the M13 NMOS transistor before and after irradiation at V_{back} = 10V (up to a total dose of 62krad).

As expected, the total dose damage is heavily dependent on the substrate bias conditions during irradiation. It is well known that the accumulation of positive charge in the BOX causes a negative shift in the threshold voltage of the back transistor. The consequent parasitic conduction induces a current leakage in the front gate transistor, which can hardly be controlled by the front gate polarization. When a positive bias (5V or 10V) is applied to the backside to deplete the detector, the leakage current of the top transistor remains at acceptable levels only for few tens of krad of total dose.

When 0V is applied, instead, the transistor is working properly up to an accumulated dose of ~ 1Mrad.

This observation implies that the total dose tolerance of such devices would greatly increase if the potential under the BOX is kept low.

For this reason, we studied the effectiveness of the PSUB guard-ring to limit the backgate effect. In Figure 7 we report the I_{ds}-V_{gs} curve for one transistor (M2 NMOS) with the PSUB contact floating and in Figure 8 the same curve for the same transistor, but with the PSUB contact tied to GND.

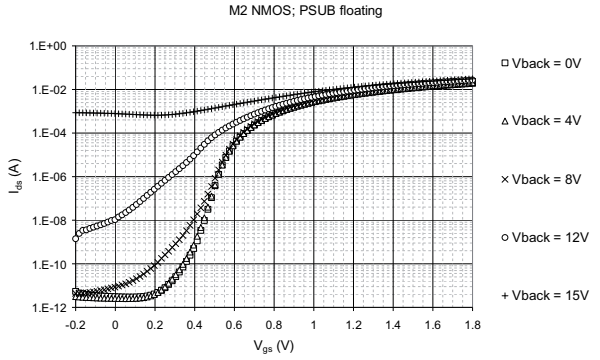

Figure 7: I_{ds}-V_{gs} curve for the M2 NMOS transistor before irradiation, with PSUB ring kept floating.

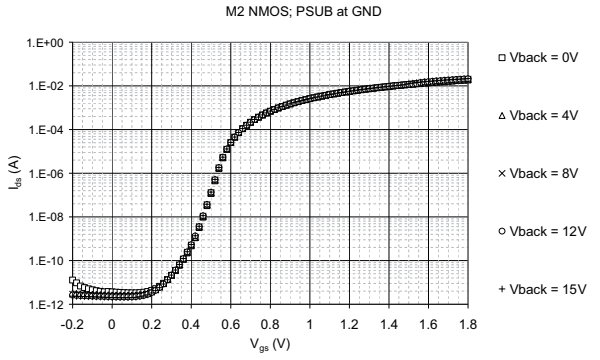

Figure 8: I_{ds}-V_{gs} curve for the M2 NMOS transistor before irradiation, with PSUB ring tied to GND.

With the PSUB at 0V, the leakage current is substantially unchanged, even for V_{back} values which usually cause the transistors to stop working properly. Analog behaviors are found for the other transistors. This result suggests that the presence of this PSUB guard-ring is indeed effective in keeping the voltage low under the BOX.

To verify if this approach is also helpful in improving the radiation tolerance of the transistors, we performed the following X-ray irradiation at V_{back} = 10V with the PSUB ring tied to GND and not floating, as in all the previous irradiations.

In Figure 9 we report in log-log scale a summarizing plot of the leakage current values (I_{ds} when V_{gs} = 0V) as a function of the total dose, for all the four irradiations of the previously described transistor, to better compare the effects.

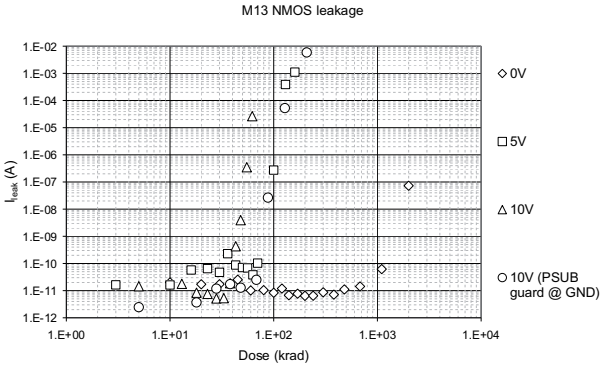

Figure 9: Leakage current values as a function of the total dose accumulated for the M13 NMOS transistor for the four different backside biases during irradiation.

The irradiation at V_{back} = 10V with the PSUB guard-ring tied to GND indeed improves the radiation hardness of the transistors, and the effect of the total dose damage is comparable with the irradiation performed at V_{back} = 5V (halfway between 0V and 10V).

The threshold voltage (V_{th}) decreases as expected as the accumulated dose increases (Figure 10); again we can see how the irradiation with PSUB guard-ring tied to GND is effective in containing the effect, even though not able to suppress it completely. The V_{th} is calculated as the intercept value with the x axis of the I_{ds}-V_{gs} curve in the linear range.

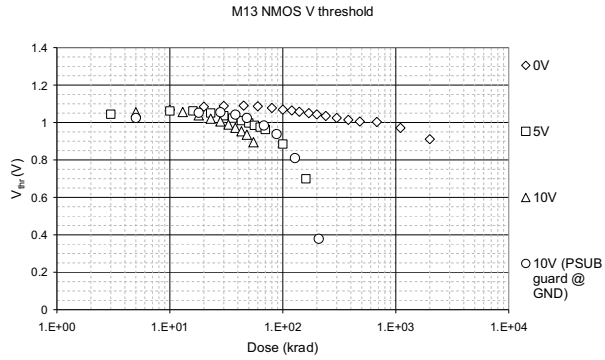

Figure 10: Threshold voltage for M13 NMOS transistor as a function of the total dose for all the four irradiation conditions.

It is interesting to note that M13 has the body externally tied to GND during irradiation, which apparently helps in keeping low the fields inside the oxides, enhancing its radiation tolerance. We can compare M13 to the transistor M2, which has the same W/L and the same threshold as M13, but with a floating body without no possibility to tie it to GND. This transistor shows a much lower radiation tolerance than M13 (at V_{back} = 0V, for example, it is able to sustain up to 80krad of accumulated dose).

V. CONCLUSIONS

Aim of this work was the study of the effect of the substrate bias conditions on the total dose damage on Monolithic Pixel Detectors fabricated in SOI technology.

The investigation focused on the 0.20µm OKI FD process, optimized for low leakage currents and used for the development of the last pixel matrix (LDRD2-SOI-2) and for the future detectors. Results are encouraging, as we experimentally proved that the transistors are able to sustain doses up to 1Mrad when the electrical field is kept low throughout the BOX. In this perspective, we also have experimental evidences of effectiveness of the use of a PSUB guard-ring in containing both the backgate effect and the total dose damage on the transistors.

Other technological solutions, like the implantation of a buried P-Well (BPW) under the BOX (and not only a PSUB guard-ring) will hopefully further suppress the backgate effect. It has been demonstrated [8] that this BPW effectively reduces the potential under the BOX and suppresses the backgate effect even at V_{back} = 100V. With a reduced electrical field through the BOX, the radiation hardness of the chip should also improve, opening up new possibilities for their applications in high radiation environment, such as SLHC.

VI. References

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