Ionizing Radiation Effects on the Noise of 65 nm CMOS Transistors for Pixel Sensor Readout at Extreme Total Dose Levels

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***Abstract*—This paper is focused on the study of the noise performance of 65 nm CMOS transistors at extremely high Total Ionizing Dose levels of the order of several hundreds of Mrad(SiO_2). Noise measurements are reported and discussed, analyzing radiation effects on 1/f noise and channel thermal noise. In NMOSFETs, up to 10 Mrad(SiO_2) the experimental behavior is consistent with a damage mechanism mainly associated with lateral isolation oxides, and can be modeled by parasitic transistors turning on after irradiation and contributing to the total noise of the device. At very high dose, these parasitic transistors tend to be turned off by negative charge accumulating in interface states and compensating radiation-induced positive charge building up inside thick isolation oxides. Effects associated with ionization and hydrogen transport in spacer oxides may be become dominant at 600 Mrad(SiO_2) and may explain the observed noise behavior at extremely high total ionizing dose. The results of this analysis provide an understanding of noise degradation effects in analog front-end circuits integrated in readout chips for pixel detectors operating in very harsh radiation environments such as the High Luminosity LHC.**

***Index Terms*—Ionizing radiation effects, MOSFET, noise, analog front-end electronics**

I. Introduction

FUTURE experiments based on high granularity silicon pixel sensors are considering the 65 nm CMOS technology as a promising candidate for mixed-signal readout integrated circuits. Such a technology has the potential to meet the very demanding requirements of diverse applications such as particle tracking in the innermost layers of high energy physics experiments at the CERN High Luminosity Large Hadron Collider (HL-LHC) and photon imaging at very high brilliance and high rate X-ray machines like the European XFEL. The readout circuits have to process signals with a very high rate while keeping a low noise performance; moreover, analog-to-digital conversion and information storage in relatively small pixels (50 μm x 50 μm for HL-LHC detectors) are also needed. Tolerance to extremely high levels of ionizing radiation is a key requirement for both application fields. It is estimated that during their operational lifetime these pixel readout chips should be able to stand a Total Ionizing Dose (TID) up to 1 Grad(SiO_2), keeping the essential performance parameters at the required values. These TID levels are unprecedented in the field of readout electronics for particle detectors, and several studies are being carried out to understand how 65 nm CMOS transistors and integrated circuits behave after the exposure to extremely high doses. The RD53 collaboration has carried out an extensive work with the goal of characterizing the behavior under irradiation of the TSMC 65 nm CMOS technology, with which a first generation of demonstrator chips is being designed [1, 2]. These studies pointed out degradation effects that are apparent in the behavior of the drain current I_D as a function of the gate-to-source voltage V_{GS} as TID exceeds a few hundreds of Mrad(SiO_2). This is especially critical for transistors with gate length and width approaching the minimum values allowed by the technology, which are mostly of interest for digital circuits [3]. Analog front-end circuits are usually based on longer and wider devices, which appear to be less sensitive to TID in terms of their I_D - V_{GS} static characteristics. However, their noise performance is a critical parameter in view of setting a hit threshold at several hundreds of electrons as it is foreseen in the RD53 demonstrator chips, or of achieving single photon resolution with X-ray imaging cameras at the XFEL.

The motivation of this work is based on the need of finding out if 65 nm CMOS analog front-end circuits can still provide an adequate noise performance even at extremely high total doses. Also, the study of radiation effects on noise can give very important hints about the damage mechanisms that degrade the performance of irradiated transistors [4, 5]. From this respect, there are already some proposed models for the mechanisms that affect I_D - V_{GS} at extremely high TID [1, 3, 6], but noise studies can give further insights.

II. Experimental Details for CMOS Transistors

A. Investigated Devices and Irradiation Procedures

An irradiation campaign has been carried out on TSMC 65 nm CMOS transistors, belonging to the LP (Low Power)

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flavour of the technology, that was chosen by RD53 and by other projects for the development of new pixel readout integrated circuits. N- and P-type transistors of various gate lengths L and widths W were integrated in purposely designed test chips, which were then exposed to TID up to 600 Mrad(SiO_2). The devices were laid out using a standard open structure, interdigitated configuration. Enclosed layout transistors were not integrated in this chip. As mentioned in the Introduction, this work is focused on TID damage studies in view of the design of 65 nm CMOS analog circuits for the readout of silicon sensors with a total pixel area of 50 µm x 50 µm. In the RD53 demonstrator chips, the area allocated to the analog front-end will be about 35 µm x 35 µm or less. Using enclosed transistor would bring along an area penalty which would be very difficult to afford. Therefore, an important goal of this paper is to prove that standard interdigitated transistor can provide an adequate noise performance up to several hundreds of Mrad(SiO_2).

Irradiation was done with 10-keV X-rays from a 50 kV X-ray machine at INFN Laboratori Nazionali di Legnaro (Italy) with a dose rate of 2 krad(SiO_2)/s. A subset of devices was exposed to a total dose of 10 Mrad(SiO_2) of γ-rays from a ^{60}Co source with a dose rate of about 8 rad(SiO_2)/s. The MOSFETs were biased during irradiation in the worst-case condition, that is, with all terminals grounded, except the gate of the NMOS, which was kept at V_{DD} = + 1.2 V. This is often considered as a worst-case bias (see for example [7]), since it is the condition actually met in a real circuit which maximizes the transport of radiation-generated holes towards the Si-SiO_2 interface. Irradiation and following measurements were performed at room temperature. During the time between irradiation and measurements, the devices were kept at - 4 °C to prevent annealing effects. A total of about 40 transistors were irradiated and tested.

B. Measurement Setup

The gate-referred noise voltage spectrum of the devices under test was measured by a Network/Spectrum Analyzer Agilent 4395A in a frequency range between 1 kHz and 100 MHz. An interface circuit was used to amplify the noise of the devices above the noise level of the spectrum analyzer [8]. This setup makes it possible to study transistor noise behavior after irradiation on a wide frequency band, monitoring both 1/f and white terms in the noise voltage spectrum. Measurements were carried out biasing the transistor in the saturation region, with |VDS| = 0.6 V, which is the normal operating condition in high gain analog amplifiers. Moreover, extremely tight power dissipation constraints are typical of high density pixel readout circuits, which dictates to operate the devices at very low current densities, in the weak or weak-to-moderate inversion region. Measurements were done in these regions, with V_{GS} close to the threshold voltage V_{TH}, with a maximum $|V_{GS}-V_{TH}|$ span of about 100 mV, again emulating the actual operating conditions of transistors in analog pixel front-end circuits.

Measurements of static and signal parameters were carried out with an Agilent B1500A Semiconductor Device Analyzer with B1511A Source/Measurement Unit (SMU) modules. Key device parameters such as the threshold voltage V_{TH} and its shift ΔV_{TH} were extracted from I_D - V_{GS} curves measured before and after irradiation, according to the procedures discussed in [9] and [10].

III. Experimental Results

A. NMOSFETs

The noise voltage spectrum $S_e(f)$ of a MOSFET is determined by a white and a 1/f noise contribution:

$$S_e^2(f) = 4kT\frac{\Gamma}{g_m} + \frac{K_f}{WLC_{OX}^2}\frac{1}{f^{\alpha_f}} = S_W^2 + S_{1/f}^2 \qquad (1)$$

The first term in (1) is due to channel thermal noise; g_m is the transconductance, k is the Boltzmann's constant and T is the absolute temperature. The value of the coefficient Γ is determined by the device operating region and takes into account possible excess noise associated with short channel effects. The second term in (1) is due to 1/f noise in the channel current. C_{OX} is the gate capacitance per unit area and K_f is an intrinsic process parameter for 1/f noise. For this 65 nm technology, it was experimentally demonstrated [11] that, in the weak and moderate inversion regions, for both NMOS and PMOS K_f is independent of the device inversion level, in agreement with the carrier fluctuation model proposed by McWhorter [12]. In this model, as in (1), the 1/f term in the noise voltage spectrum is inversely proportional to C_{OX}^2.The slope coefficient α_f was found to be close to 0.9 in NMOS from various generations and foundries, including the TSMC LP process studied in this paper [11].

According to the number fluctuations model, K_f is proportional to $D_t(E_f)$, that is the number of traps per unit energy per unit area at the Fermi level E_f [5, 13]. Actually, only so-called border traps (traps located in the gate oxide near the interface with the device channel) [5] contribute to 1/f noise in the investigated frequency range.

Fig. 1 shows the typical behavior of the noise voltage spectrum of an NMOSFET measured before and after an irradiation step at 200 Mrad(SiO_2), followed by another step reaching up to a total dose of 600 Mrad(SiO_2). In the high-frequency part of the spectrum, beyond 1 MHz, channel thermal noise is dominant. From Fig. 1, it clearly results that this noise term is negligibly affected by irradiation, even at very high TID, as it was also previously found at 10 Mrad(SiO_2) [14]. This behavior appears to be independent of the drain current density $I_D \cdot (L/W)$ the device is operated at, as shown by Fig. 2. For the device in Fig. 1, $I_D \cdot (L/W)$ = 13 nA, whereas for the transistor in Fig. 2 $I_D \cdot (L/W)$ = 130 nA; both transistors have the same gate length L = 0.13 µm. In both cases, channel thermal noise is not affected by irradiation, in agreement with the behavior of the transconductance g_m: as shown by Fig. 3, the value of g_m at a constant I_D does not change with TID, as for the value of the white noise voltage spectrum S_W.

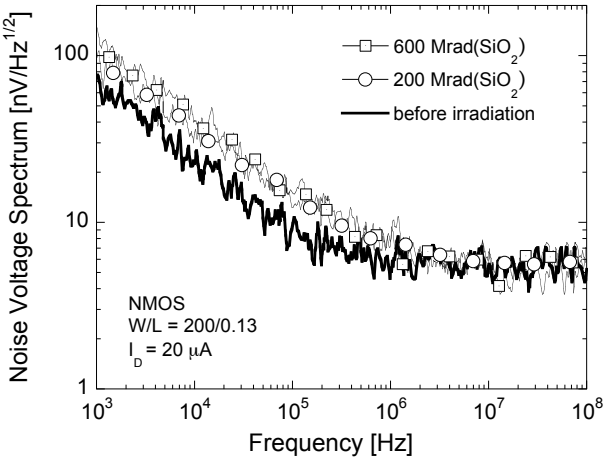

Fig. 1. Noise voltage spectra before irradiation and after exposure to 10 keV X-rays for an NMOSFET with W/L = 200/0.13 at I_D = 20 μA, V_{DS} = + 0.6 V. The plot shows results of measurements at 200 Mrad(SiO_2) and 600 Mrad(SiO_2) TID.

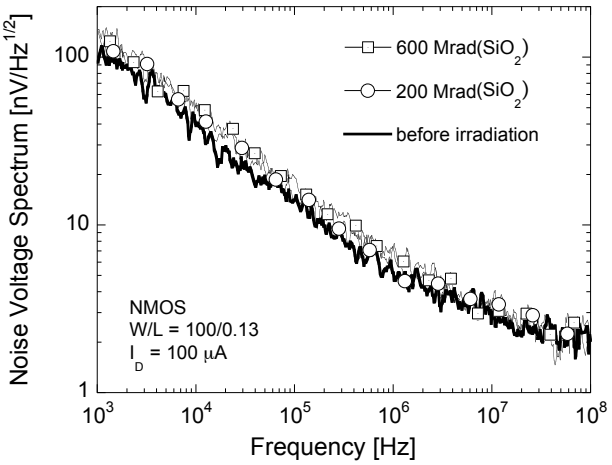

Fig. 2. Noise voltage spectra before irradiation and after exposure to 10 keV X-rays for an NMOSFET with W/L = 100/0.13 at I_D = 100 μA, V_{DS} = + 0.6 V. The plot shows results of measurements at 200 Mrad(SiO_2) and 600 Mrad(SiO_2) TID.

As far as 1/f noise is concerned, a moderate increase of the noise voltage spectrum at low frequencies was observed in all the tested devices, as it is apparent from Figures 1 and 2. Previously reported results at 10 Mrad(SiO_2) TID in 65 nm NMOSFETs [14] showed a relatively large 1/f noise increase at low drain current density, whereas at higher currents an almost negligible degradation was observed. This behavior was also detected in devices from less scaled CMOS nodes [15]. 65 nm NMOSFETs exhibit a remarkably different behavior at very high TID, where the increase in 1/f noise is not so strongly dependent on the drain current density, as shown by Figures 1 and 2.

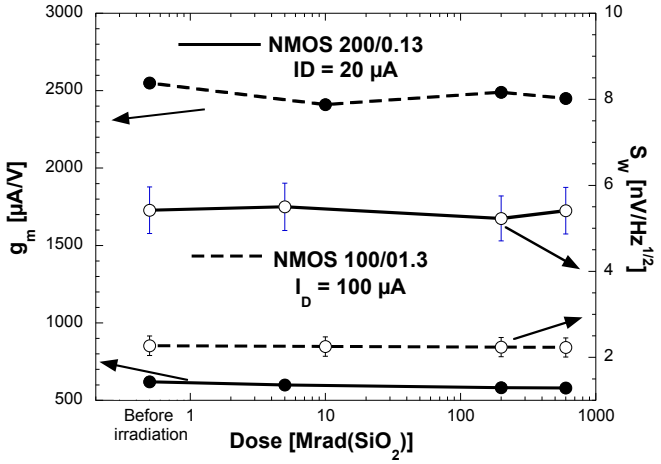

Fig. 3. Values of the white noise voltage spectra S_W and of the transconductance g_m measured before irradiation and after exposure to 10 keV X-rays (data at 5, 200 and 600 Mrad(SiO_2)) and ^{60}Co γ-rays (data at 10 Mrad(SiO_2)) for NMOSFETs with W/L = 200/0.13 at I_D = 20 μA, and with W/L = 100/0.13 at I_D = 100 μA, V_{DS} = + 0.6 V. Error bars for S_W values show the typical 10 % error associated with the extraction of noise parameters from measurements.

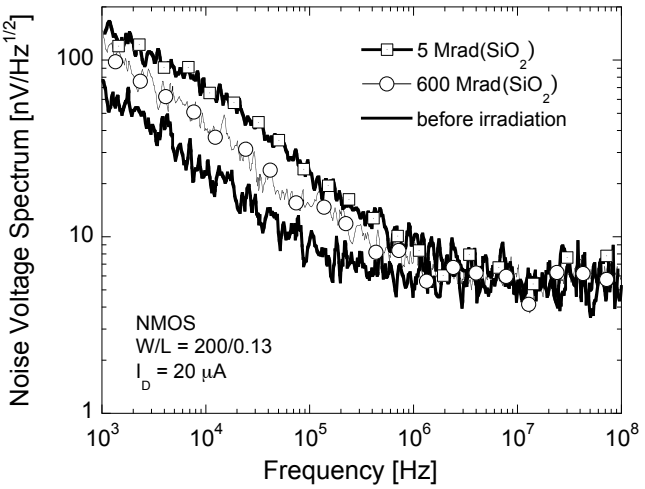

Fig. 4. Noise voltage spectra before irradiation and after exposure to 10 keV X-rays for two NMOSFETs with W/L = 200/0.13 at I_D = 20 μA, V_{DS} = + 0.6 V. The plot shows results of measurements at 5 Mrad(SiO_2) for one of the transistors and at 600 Mrad(SiO_2) for the other one.

Moreover, the 1/f noise term has a remarkable behavior as a function of TID. Figures 4 and 5 show the noise measurements up to 600 Mrad(SiO_2) for an NMOSFET with W/L = 200/0.13, and data taken at 5 Mrad(SiO_2) for another transistor with the same geometry at the same drain current. Both transistors had very similar values of the noise voltage spectrum before irradiation. The plots show that, at a low I_D value of 20 μA, 1/f noise at 5 Mrad(SiO_2) is sizably higher than at 600 Mrad(SiO_2), whereas increasing I_D up to 100 μA this difference becomes almost negligible.

Fig. 6 shows the typical behavior of the ratio of 1/f noise terms measured after irradiation and before irradiation in NMOSFETs. At low current density, the 1/f noise increase with respect to preirradiation values is larger at 10 Mrad(SiO_2),

then becomes smaller at 200 Mrad(SiO_2), and finally grows again at 600 Mrad(SiO_2). At higher current density, 1/f noise increases gradually with increasing TID. This behavior can be explained by the action of different mechanisms, affecting the noise voltage spectrum to an extent which depends on the TID level. At relatively low TID (5 and 10 Mrad(SiO_2)) the dominant effect may be given by the noise contribution from the lateral parasitic devices associated with the Shallow Trench Isolation (STI) oxides, as discussed in previous papers for NMOSFETs in CMOS nodes from 130 nm to 65 nm [14, 15, 16]. Radiation-induced positive charge accumulates in thick lateral STI oxides, inverting P-type silicon bulk regions at the transistor edges and creating leakage paths along the STI sidewalls. In [15], it was demonstrated that, at a TID of 10 Mrad(SiO_2), lateral parasitic transistors are turned on in this way, and that at small total drain current they affect the device characteristics to a larger extent. In the low I_D region, also their contribution to the total noise of the device is larger, especially as far as the 1/f noise term is concerned. This interpretation was also supported by data gathered on enclosed transistors in the 130 nm CMOS process, which did not show this behavior at all [15].

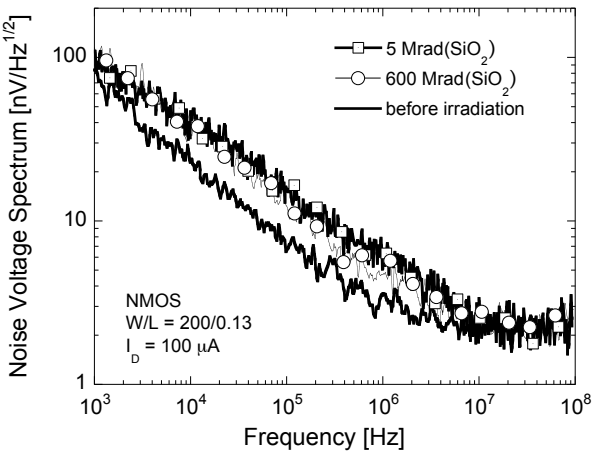

Fig. 5. Noise voltage spectra before irradiation and after exposure to 10 keV X-rays for two NMOSFETs with W/L = 200/0.13 at I_D = 100 μA, V_{DS} = + 0.6 V. The plot shows results of measurements at 5 Mrad for one of the transistors and at 600 Mrad for the other one.

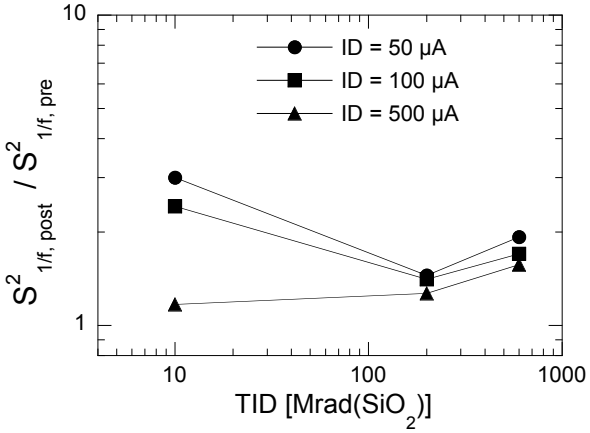

Fig. 6. Ratio of 1/f noise terms after irradiation (at various TID) and before irradiation for an NMOS transistor with W/L = 100/0.13 at three values of the drain current I_D.

This paper explores for the first time the effects on noise of extremely high TID values on a wide frequency band on NMOSFETs. From the previous discussion, and specifically from Fig. 6, it is clear that at 200 and 600 Mrad(SiO_2) the dependence of the 1/f noise increase on the drain current is much smaller than at 10 Mrad(SiO_2). This requires a different mechanism taking place at these high TIDs, as compared to what is at play at low TID. According to studies carried out in the frame of the RD53 collaboration [1, 3], at very high TID radiation-induced interface states building up at the STI oxide interface play an important role in affecting the behavior of irradiated transistors. In the case of NMOSFETs, they become negatively charged, counteracting and at a certain point overcoming the effect of positive charge trapped in the STI oxides. The drop in the 1/f noise term going from 10 to 200 Mrad(SiO_2) can be explained by the effect of negatively charged interface states which turn off lateral parasitic transistors, so deleting their contribution to the total noise of the device.

The increase of 1/f noise going from 200 up to 600 Mrad(SiO_2) shows that another effect is also occurring and becomes the dominant one at high doses. In this extremely high TID region, the increase in the 1/f noise magnitude (with no significant variation of the slope α_f) can be explained by an increase in the density of border traps $D_t(E_f)$. Recent studies demonstrated that, at very high doses, degradation mechanisms in 65 nm transistors are associated with ionization in the spacer dielectrics that in modern CMOS processes are deposited on the sidewall of the gate oxide [3, 6]. Radiation-induced ionization in spacer oxides, among other effects, frees hydrogen ions, that are transported towards the interface with the channel region. As protons reach the near-interfacial region, some may ultimately form border traps [17] and increase 1/f noise, with an effect that becomes significant at high TID. In [6], this mechanism was thoroughly investigated, studying its voltage dependence and the effects of high temperature annealing. As discussed in Section II.B, we focus here on the behavior of transistors operating close to the weak inversion region, so that a limited range (about 100 mV) of $|V_{GS} - V_{TH}|$ is explored, making it difficult to assess possible variations in the defect-energy distribution [6].

This explanation of the damage mechanism that affects the noise of irradiated NMOSFETs is supported by experimental data from the static characteristics, that are consistent with the behavior of the 1/f noise term. In this work, we studied devices with a relatively large W/L, where effects on I_D static curves are small even at the highest doses we explored, as shown by Fig. 7. This plot shows the typical behavior of the NMOS drain current as a function of the gate-to-source voltage V_{GS}. A moderate I_D increase is detected in the NMOS constant leakage current region (corresponding to negative V_{GS}). However, looking at these static measurements in more detail, it is possible to see effects that can be correlated with the previously discussed behavior of 1/f noise, especially concerning the reduced impact at high TID of mechanisms associated with lateral parasitic transistors. In Fig. 8, the percent variation of I_D is plotted as a function of the

preirradiation value $I_{D,pre}$ of the drain current, at three different TID values, for the same device in Fig. 7. The drain current range in Fig. 8 includes the values of I_D relevant to the noise measurements discussed above. At 10 Mrad(SiO_2), I_D increases because of the contribution of lateral parasitic transistors, combined with the small negative shift of the threshold voltage (of the order of a few mV) shown in Fig. 9. At large TID, I_D decreases because lateral leakage paths are not present any more. Moreover, there is a positive threshold voltage shift (again of a few mV) which can also be associated with the growing effect of negatively charged interface states.

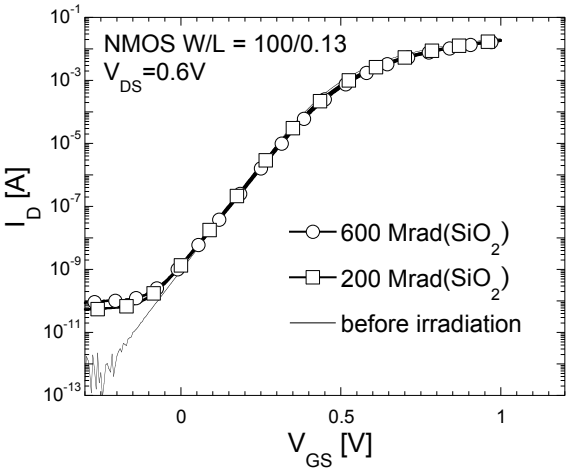

Fig. 7. Drain current I_D as a function of the gate-to-source voltage V_{GS}, before irradiation and upon absorption of a 200 and 600 Mrad(SiO_2) total dose of 10 keV X-rays for an NMOSFET with W/L = 100/0.13 at V_{DS} = + 0.6 V.

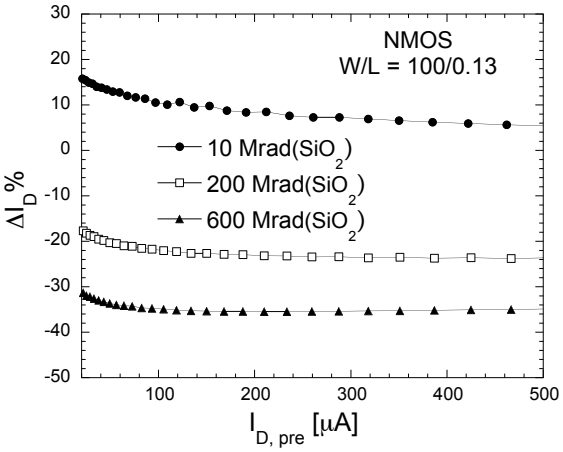

Fig. 8. Percent variation of I_D as a function of the preirradiation value of the drain current for an NMOSFET with W/L = 100/0.13 at 10, 200 and 600 Mrad(SiO_2) total dose of 10 keV X-rays.

B. PMOSFETs

Figures 10 and 11 show typical results of measurements of the noise voltage spectra of PMOSFETs at extremely high TID values. As in NMOSFETs, no degradation of the white noise component of the spectrum is observed. There is instead a moderate increase of the 1/f noise term, by a smaller magnitude than in N-type transistors, so that it is barely detectable from Figures 10 and 11. Moreover, the behavior of 1/f noise with increasing TID is different. In PMOSFETs, there is no dependence of 1/f noise degradation on the drain current density, so even at low current density this term increases gradually with TID, as shown by Fig. 12.

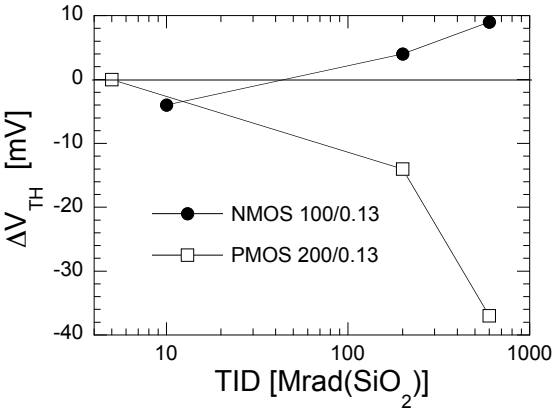

Fig. 9. Threshold voltage shift ΔV_{TH} as a function of the absorbed dose of 10-keV X-rays for an NMOSFET and a PMOSFET.

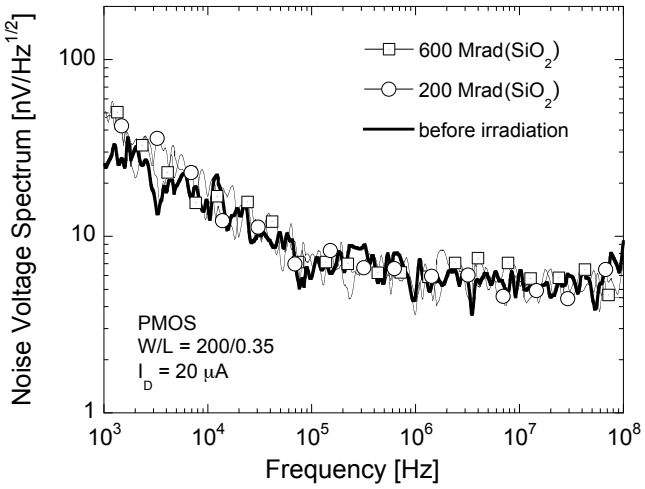

Fig. 10. Noise voltage spectra before irradiation and after exposure to 10 keV X-rays for a PMOSFET with W/L = 200/0.35 at I_D = 20 μA, V_{DS} = - 0.6 V. The plot shows results of measurements at 200 and 600 Mrad(SiO_2) TID.

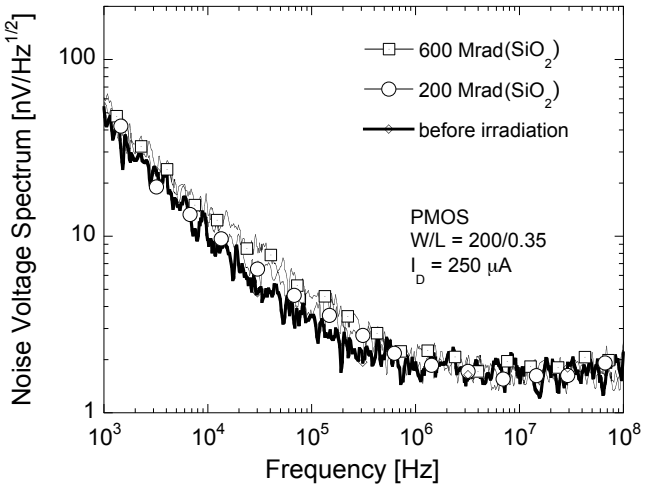

Fig. 11. Noise voltage spectra before irradiation and after exposure to 10 keV X-rays for a PMOSFET with W/L = 200/0.35 at I_D = 250 μA, V_{DS} = - 0.6 V. The plot shows results of measurements at 200 and 600 Mrad(SiO_2) TID.

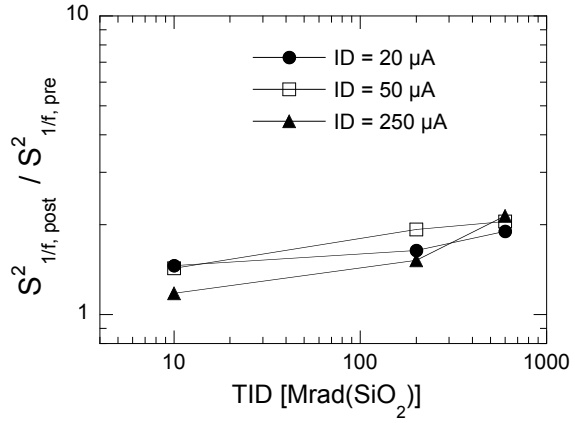

Fig. 12. Ratio of 1/f noise terms after irradiation (at various TID) and before irradiation for a PMOS transistor with W/L = 200/0.35 at three values of the drain current I_D.

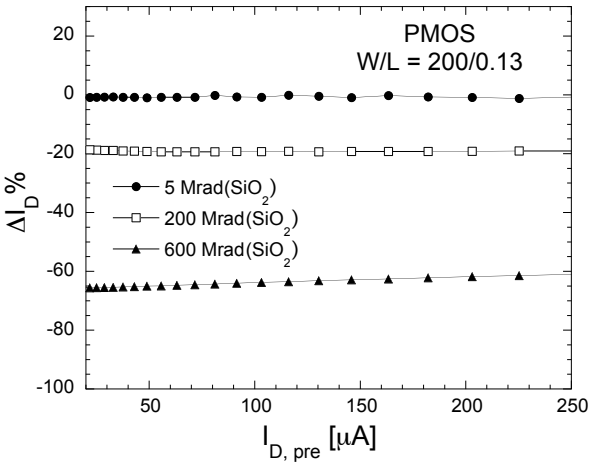

Fig. 13. Percent variation of I_D as a function of the preirradiation value of the drain current for a PMOSFET with W/L = 200/0.13 at 5, 200 and 600 Mrad(SiO_2) total dose of 10 keV X-rays.

This behavior of irradiated PMOSFETs is due to the fact that radiation-induced positive charge in lateral isolation oxides brings the substrate region close to the STI deeper into accumulation, without creating any leakage path for holes from source to drain, and so without turning on any noisy lateral parasitic transistor. For these devices, interface states along the STI become also positively charged, adding to the effect of positive charge trapped inside STI oxides. So there is no effect on noise associated with lateral parasitic transistors, that are never turned on. The main effect is a negative shift of the threshold voltage, by a larger magnitude than in NMOSFETs, as shown by Fig. 9. This is also consistent with the percent variation of the drain current I_D in irradiated PMOSFETs, which has always a negative sign (with a very small magnitude at 5 Mrad(SiO_2)) also at the lowest investigated TID, as shown by Fig. 13.

In PMOSFETs, the dominant mechanism underlying the observed 1/f noise increase can be associated with an increase in border traps, from low TID levels up to 600 Mrad(SiO_2). Again, as discussed in Section III.A for NMOSFETs, the model proposed in [6] can provide a convincing interpretation of effects related to hydrogen transport in spacer oxides.

IV. Evaluation of TID Effects on the Noise Performance of a Pixel Analog readout Channel

The experimental data gathered with the irradiation campaign on 65 nm CMOS transistors can provide the basis for estimating the performance of an analog readout channel designed in this technology, in view of applications where the front-end electronics is required to stand TID levels of several hundreds of Mrad(SiO_2). The noise behavior at these total dose levels is crucial for the operation of the front-end electronics in the innermost pixel layer of HL-LHC. Because of radiation damage in the pixel sensors, resulting in a reduction of collected signal charge, a pixel readout cell has to work with a low discriminator threshold to maximize detection efficiency. In terms of input charge, it is estimated that the hit threshold should be set below 1000 electrons, possibly as low as 600 electrons [2, 18]. Maintaining a low noise performance at high TID is then crucial to avoid an excessive noise occupancy during several years of operation of the pixel detector.

A prediction of radiation damage effects on the noise performance of a pixel analog front-end channel has to take into account the specific features of the design of this circuit. First of all, it is reasonable to assume that the main contribution to the noise of the whole channel is given by the noise in the drain current of the preamplifier input device. This term can be modeled by a noise voltage generator in series with the preamplifier input, with a power spectral density $S_e^2(f)$ given by (1). Parallel noise contributions associated with the preamplifier feedback network or with the detector leakage current are of a lesser importance at the short signal processing times relevant to this application. Actually, the signal peaking time has to be of the order of the foreseen bunch crossing period of 25 ns. The preamplifier input device has to be at least approximately matched to the sensor capacitance, expected to be of the order of several tens of fF up to 100 fF, which drives the choice of a gate width of a few μm, considering that the gate capacitance per unit area is C_{OX} = 18.5 fF/μm^2. Previous noise studies on the 65 nm CMOS generation suggest that the minimum gate length is avoided, so as to minimize excess noise contributions [19]. As a result, in the asynchronous continuous time pixel front-end described in [20, 21], the preamplifier input device is an NMOSFET with W/L = 5/0.10. Moreover, power dissipation constraints limit the drain current of the input transistor to very few μA, specifically 2.8 μA in the case discussed in [20, 21].

As already discussed in Section II.A, another important point is that the analog front-end channel has to be integrated inside a pixel cell with a small pitch, typically of the order of 50 μm x 50 μm, where digital logic also has to fit in. This has driven the designers towards the so-called shaperless architecture to reduce the amount and the area of analog circuitry in the pixel cell [18, 22]. This means that the detector current signal is integrated by a charge-sensitive preamplifier and then fed into the input of a discriminator. Bandwidth limitations and noise filtering are performed by the preamplifier itself, since no signal shaping stage is present.

According to the previous considerations, the prediction of the noise behavior under irradiation of a pixel readout channel at HL-LHC can be accomplished by the two following steps. First, the noise voltage spectrum for the preamplifier input transistor with the correct gate area and drain current can be calculated using parameters extracted from noise voltage spectra measured before and after irradiation on devices in the 65 nm process. Second, the transfer function relevant to the series noise voltage generator can be calculated using realistic parameters for a shaperless front-end based on the general schematic in Fig. 14.

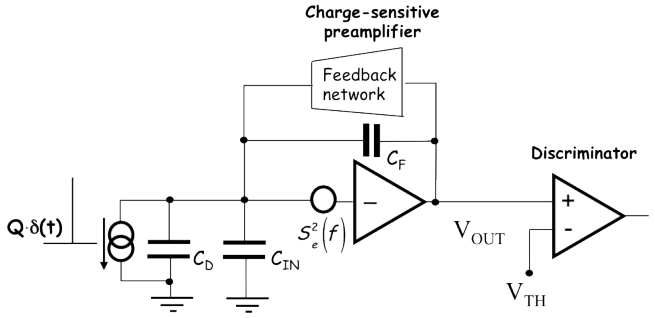

Fig. 14. Schematic of a continuous-time asynchronous front-end for the readout of pixel sensors at HL-LHC. The detector is modeled as a current source delivering a Dirac δ pulse with an area equal to the charge Q collected by the pixel electrode. The preamplifier output voltage signal V_{OUT} is compared with a threshold voltage V_{TH} for detection of particle hits.

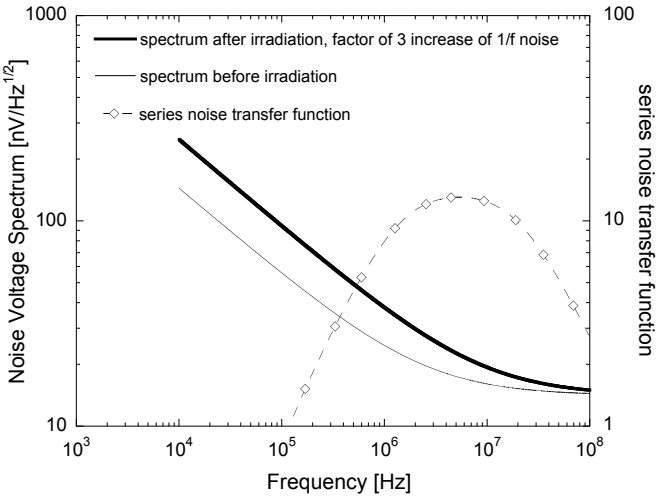

Fig. 15. Noise voltage spectra calculated from measured data before irradiation and after exposure to a 600 Mrad(SiO_2) total dose of 10-keV X-rays for an NMOSFET with W/L = 5/0.10 at I_D = 2.8 μA. The plot shows also the calculated magnitude of the transfer function for the series noise voltage generator at the input of the preamplifier in a front-end cell for the readout of pixel sensors at HL-LHC.

Fig. 15 shows the calculated noise voltage spectra before irradiation and after exposure to a 600 Mrad(SiO_2) TID for an NMOSFET with W/L = 5/0.10 operating at I_D = 2.8 μA. The values in the plot where calculated assuming the noise model in (1). For the 1/f noise term, values of the coefficient K_f were extracted from measurements on NMOSFETs. This made it possible to evaluate the 1/f noise term, which is inversely proportional to the gate area and, in NMOSFETs, is independent of the drain current I_D. A factor of 3 increase of 1/f noise after irradiation was assumed, that is close to the value we measured at 600 Mrad(SiO_2) TID for devices operated at a similar drain current density. The white noise term was estimated by calculating the value of the coefficient Γ and of the transconductance g_m according to relationships discussed in [11, 19], which take into account the weak-to-moderate inversion region where the device is operating at the relevant drain current density levels. According to measurements results, it is assumed that white noise does not increase after irradiation.

Fig. 15 also shows the magnitude of the transfer function T(j2πf) from the series noise voltage generator at the preamplifier input to the preamplifier output. This has the purpose of highlighting the frequency region of the noise spectrum that actually determines the noise performance of the pixel front-end cell. T(j2πf) is related to the frequency response F(j2πf) of the charge-sensitive preamplifier (from the input current source to the voltage signal output) by the relationship:

$$T(j2\pi f) = j2\pi f\left(C_D + C_{IN} + C_F\right)F(j2\pi f) \tag{2}$$

In (2), C_F is the preamplifier feedback capacitance, C_{IN} is the preamplifier input capacitance and C_D is the sensor pixel capacitance. F(j2πf) is normalized, considering an amplitude equal to 1 for the response of the preamplifier to a unit input charge. T(j2πf) was calculated according to simulated parameters for the forward inverting gain stage and the feedback network in the preamplifier [21], which result in a time domain response with a peaking time of about 25 ns to a detector Dirac δ current pulse. From the data in Fig. 15, the radiation-induced 1/f noise increase is expected to give an effect in the bandwidth of the pixel readout channel. Actually, the Equivalent Noise Charge (ENC) can be calculated from these data according to the following relationship [21]:

$$\begin{aligned} ENC^2 &= \int_0^{+\infty}\left|T(j2\pi f)\right|^2 S_e^2(f)df = \\ &= \int_0^{+\infty}\left(2\pi f\right)^2\left(C_D + C_{IN} + C_F\right)^2\left|F(j2\pi f)\right|^2 S_e^2(f)df \end{aligned} \tag{3}$$

Using data from Fig. 15, at C_D = 100 fF Equation (3) yields ENC = 85 e rms before irradiation, ENC = 100 e rms after irradiation. This 15 % ENC increase is consistent with experimental data gathered on prototypes of pixel readout front-end chips irradiated with 10 keV X-rays up to a 600 Mrad(SiO_2) TID [23, 24]. With this moderate ENC increase, these analog front-end circuits are still compliant with the noise specifications set by RD53 [2]. This analysis confirms that the irradiation data for single transistors and the noise degradation mechanisms discussed in this paper are able to provide the basis for understanding and predicting the behavior of analog front-end circuits for the readout of pixel detectors in very harsh radiation environments.

V. Conclusion

This paper presented a study of the effects of extremely high total ionizing doses on the noise behavior of transistors in a 65 nm CMOS process. For the first time, noise measurements on heavily irradiated 65 nm transistors were performed on a very wide frequency range, up to 100 MHz, as needed to forecast the behavior of analog circuits operating at high signal rates for the readout of pixel sensors at the HL-LHC. The experimental results confirm the high degree of radiation tolerance that is typical of CMOS processes from the 130 nm to the 65 nm node. It is important to underline that the goal has been to understand degradation effects in low-noise analog circuits, where minimum size transistors are very seldom used. In digital circuits, these are the most critical devices that may impair the radiation tolerance of a mixed-signal chip at a TID of several hundreds of Mrad(SiO_2). The data discussed in this paper instead support the prediction that analog circuits can operate up to 600 Mrad(SiO_2) TID with a moderate (10 – 15%) degradation of their noise performance, as it is also confirmed by tests on prototype chips. The major damage mechanism at doses up to 10 Mrad(SiO_2) appears to be associated with NMOSFETs and lateral parasitic transistors, whose noise adds to the total noise of the device when they are turned on by radiation-induced positive charge in STI oxides. At several hundreds of Mrad(SiO_2), negatively charged interface states compensate positive charge build-up in isolation oxides, making the contribution from lateral parasitic transistors less important. At very high TID, the noise behavior of NMOSFETs and PMOSFETs is consistent with damage mechanisms associated with ionization in spacer oxides [15], which become dominant with respect to the contribution from noisy lateral parasitic transistors. Overall, a moderate noise increase is detected at 600 Mrad(SiO_2), the largest TID studied in this paper. This is very promising in view of applications of 65 nm analog front-ends in very harsh radiation environments, such as the readout of pixel sensors in high energy physics and photon science experiments. Studies of annealing effects and of radiation effects on noise at low temperature may provide further insight, but they are beyond the scope of this paper.

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