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Design and characterization of novel monolithic pixel sensors for the ALICE ITS upgrade

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ABSTRACT

Within the R&D activities for the upgrade of the ALICE Inner Tracking System (ITS), Monolithic Active Pixel Sensors (MAPS) are being developed and studied, due to their lower material budget ($\sim 0.3\% X_0$ in total for each inner layer) and higher granularity ($\sim 20\ \mu m \times 20\ \mu m$ pixels) with respect to the present pixel detector. This paper presents the design and characterization results of the Explorer0 chip, manufactured in the TowerJazz 180 nm CMOS Imaging Sensor process, based on a wafer with high-resistivity ($\rho > 1\ k\Omega\ cm$) and 18 μm thick epitaxial layer. The chip is organized in two sub-matrices with different pixel pitches (20 μm and 30 μm), each of them containing several pixel designs. The collection electrode size and shape, as well as the distance between the electrode and the surrounding electronics, are varied; the chip also offers the possibility to decouple the charge integration time from the readout time, and to change the sensor bias. The charge collection properties of the different pixel variants implemented in Explorer0 have been studied using a ^{55}Fe X-ray source and 1–5 GeV/c electrons and positrons. The sensor capacitance has been estimated, and the effect of the sensor bias has also been examined in detail. A second version of the Explorer0 chip (called Explorer1) has been submitted for production in March 2013, together with a novel circuit with in-pixel discrimination and a sparsified readout. Results from these submissions are also presented.

1. Upgrade scenario

The present ALICE Inner Tracking System (ITS) [1] is composed of six cylindrical layers placed around the interaction point. The layers are equipped with silicon detectors fabricated in three different technologies: proceeding from the interaction point outward there are two layers of Silicon Pixel Detectors, two layers of Silicon Drift Detectors and two layers of Silicon Strip Detectors. An upgrade of the ITS is being prepared to enhance the capabilities, among other topics, to study heavy flavor particles generated in heavy ion collisions, following the LHC plans to increase the beam luminosity after 2018 [2].

One of the main goals of the upgrade is to increase the impact parameter resolution by a factor of ~ 3 in the bending plane ($r\phi$) with respect to the present architecture: the number of layers of the ITS will be increased from 6 to 7, and the first detector layer will be placed at 22 mm from the interaction point (to be compared with the present 39 mm) following a reduction of the beam pipe outer radius that will decrease from 29.8 mm to 19.8 mm. The impact parameter resolution is also directly dependent on the granularity of the first detection layers, which will be increased using a smaller pixel size.

Table 1 summarizes the main specifications for the future ITS, distinguishing the three innermost layers (inner barrel) from the four outermost layers (outer barrel). The silicon thickness for all of the layers will be of 50 μm, allowing to reach a total material budget of only $0.3\% X_0$ for the inner barrel layers and $0.8\% X_0$ for the outer ones. The chip size will be $15 \times 30\ mm^2$, with a pixel size in the order of $30\ \mu m \times 30\ \mu m$ (inner barrel) up to $50\ \mu m \times 50\ \mu m$

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Table 1
Specifications for the inner and the outer barrel for the upgrade of the ITS.

Characteristic	Inner barrel	Outer barrel
Silicon thickness (μm)	50	50
Material thickness	$0.3\%X_0$	$0.8\%X_0$
Chip size (mm^2)	15×30	15×30
Pixel size (μm^2)	$O(30 \times 30)$	$O(30 \times 30)$–$O(50 \times 50)$
Integration time (μs)	< 30	< 30
Power density (mW/cm^2)	< 300	< 100
Hit density (Pb–Pb) (cm^{-2})	~ 115	~ 1.5
Radiation load (TID) (krad)	< 700	< 10
1 MeV n_{eq} fluency (cm^{-2})	1.1×10^{13}	3×10^{10}

Table 2
Options for the ALICE ITS upgrade chip.

Design	Speed (μs)	Power (mW/cm^2)	Characteristics
Mistral	30	> 300	2 Rows rolling shutter discrim. at end of column
Astral	15/30	$< 150/200$	2/4 Rows rolling shutter in pixel discrim.
Cherwell2	30	< 100	Rolling shutter, strixel module
ALPIDE	2	< 50	Sparsified readout, in pixel discrim.

(outer barrel). The new detector will target an integration time of less than 30 μs, and a low power consumption below 300 mW/cm^2. According to the target statistics in terms of Pb–Pb and pp collisions, the new detector is required to be tolerant to 700 krad, including already a conservative safety factor of 4.

The optimal way to achieve these constraints, especially the ones on the material budget and on the pixel granularity, is the usage of CMOS Monolithic Active Pixels Sensors (MAPS), where the sensor and the readout electronics are integrated inside the same silicon chip. The monolithic pixel detectors have shown a significant progress in recent years [3,4], and they are fabricated in commercial CMOS technologies, optimized for large volumes and very cost-effective. Studies on their radiation tolerance have also been performed [5]. The state of the art of monolithic pixel detectors is represented by the STAR PXL detector at RHIC, which is equipped with the ULTIMATE chips [6] developed in 0.35 μm technology by the IPHC Strasbourg group and which is expected to be installed during 2013. However, the ULTIMATE chip does not meet the specifications for the ALICE ITS upgrade, especially in terms of readout time and radiation tolerance, so further developments are needed.

The technology chosen for the ITS upgrade is the TowerJazz[1] 180 nm CMOS technology: it offers a standard epitaxial layer of 15–18 μm with a resistivity between 1 and 5 kΩ cm and a gate oxide thickness below 4 nm, thus being more robust to TID than the 0.35 μm technology. Up to six metal layers can be used, allowing the design of high density and low power digital circuits that can reduce the periphery area (from the current 2.4 mm to ~1–1.5 mm) and thus reduce the amount of dead material. An important feature of this technology is the possibility to add a special deep P-well to shield the N-well containing PMOS transistors that could otherwise compete with the N-well of the sensing diode for the charge collection. This allows the usage of both NMOS and PMOS transistors inside the pixel area, with the possibility to include a discriminator inside the pixel and have a fast readout based on the binary information.

[1] www.jazzsemi.com

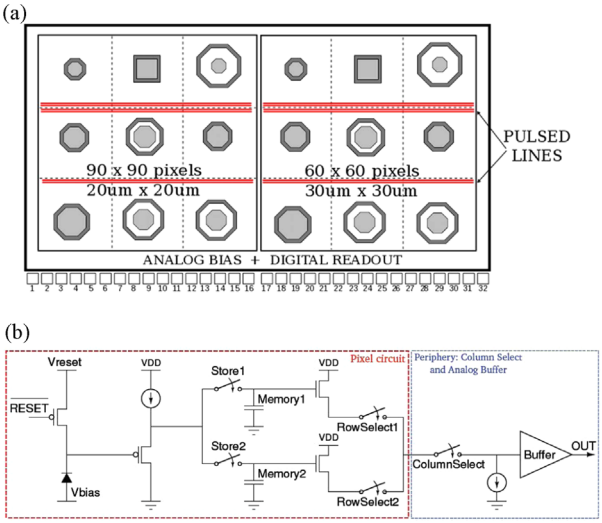

Fig. 1. (a) Structure of the Explorer chip, with, superimposed, its segmentation into sectors and the pulsed rows. (b) Circuitry of the Explorer front-end.

Four different design streams for the ITS upgrade are being explored by different groups; their main characteristics are summarized in Table 2. This paper will focus on the ALPIDE development that is being designed in a collaboration among CERN, INFN (Italy) and CCNU (China). All of the options presented in Table 2 can meet the ITS upgrade requirements, but the ALPIDE design is exploring a less conventional architecture based on a sparsified readout that offers a low integration time and a low power consumption. The small integration time is beneficial because it reduces the event pile-up effects, which also have an impact on the event reconstruction and analysis, while the low power consumption allows a reduction of the material budget of the electrical power cables and cooling system.

2. Explorer prototypes

2.1. Chip design

The Explorer chips are developed with the goal of optimizing the sensor diode layout for the ALPIDE development. In particular, with the Explorer family it is possible to study the effect on the chip performance of geometrical characteristics of the collecting diode, such as its shape and size, as well as the distance between the diode N-well and the surrounding electronics, the pixel size and the reverse bias applied to the pixel.

As shown in Fig. 1, the chip is composed of two matrices of pixels. The matrix on the left side of the chip contains pixels with a size of 20 μm × 20 μm arranged in 90 columns and 90 rows, while the matrix on the right contains pixels with a size of 30 μm × 30 μm arranged in 60 columns and 60 rows. Each matrix is sub-divided into nine sectors, each of them containing a different diode geometry as represented in the figure. The bottom part of the chip contains the electronics for the matrix readout and the analog biases. The nominal supply voltage is 1.8 V both for the analog and digital power.

Some rows in the matrices can be pulsed injecting a charge by applying a step voltage to a series capacitor. This was implemented only for a limited number of rows in order to avoid perturbations to the pixel matrix. In the other rows, the injection capacitor is present in the pixel, but it is connected to a fixed voltage.

Two versions of the Explorer chip have already been fabricated: the first version was submitted in July 2012 with a standard epitaxial layer of 18 μm and a resistivity between 1 and 5 kΩ cm,

and further versions were submitted in April 2013 on seven different substrates.

The front-end circuitry of the Explorer chip is shown at the bottom of Fig. 1. Each pixel contains two independent memory cells that implement a Correlated Double Sampling: the voltage signal at the output of the collecting diode is stored in one cell just after a RESET signal is propagated in the pixel matrix (reference voltage level), and it is stored in the other cell at the end of the integration cycle (signal voltage level). These two analog voltage levels are sent outside the chip and the hit information is obtained subtracting the two levels off-chip after digitization. An advantage of the Explorer architecture is that the readout time is totally decoupled from and independent of the integration time. All the pixels are read sequentially with a ColumnSelect and a RowSelect signal managed by a sequencer at the periphery of the chip.

2.2. Characterization results

The chip was tested with a ^{55}Fe X-ray source to determine its charge collection efficiency. The response was checked for the seed pixels, i.e. the pixels with the highest collected signal in a 5×5 matrix, and for the clusters, i.e. 5×5 pixels around each seed pixel; an example of the two signals is shown in Fig. 2.

The plots show the signal before and after the chip was irradiated to 1×10^{13} cm^{-2} MeV n_{eq}. The signal coming from the 20 μm pixel pitch matrix has a peak around 550 ADC counts, and the signal coming from the 30 μm pitch matrix has a peak around 460 ADC counts; this variation is due to the readout scheme of the Explorer chip, read column by column starting with the 20 μm × 20 μm pixel matrix and continuing with the 30 μm × 30 μm pixel matrix: during the readout, the leakage current of the capacitor where the signal is stored lowers the signal of the 30 μm × 30 μm pixels. The dispersion of the signal distribution is the same in both cases. Both plots also show a small peak at high values, which corresponds to the source calibration peak, where all the 1640 electrons generated by the X-ray deposition in the detector of the ^{55}Fe source are collected by a single pixel; the position of this peak gives the possibility to correlate the number of ADC counts on the *x*-axis of the plots with the number of electrons. The charge collected by the single pixel is almost not affected by the non-ionizing radiation, while the 5×5 clusters show a small degradation of the charge collection efficiency that can be quantified in a reduction of about 20%, due to the probability of charge trapping in the sensor bulk.

The signals shown in the plots have been obtained with a reverse bias of −6 V applied to the chip. The effect of the reverse bias on the charge collection efficiency was also measured. Increasing (in absolute value) the reverse bias voltage, from 0 V to −6 V, determines an increase of the depletion volume under the collecting diode; this translates to an increase of the signal collected by the single pixel, and also to a reduction of the cluster size, with a consequent positive effect on the charge collection.

The Explorer chips were also characterized in terms of noise, whose evolution was studied both in space and time; data acquisitions with 100 consecutive pedestal measurements were taken, each measurement corresponding to approximately 30 s. A sector to sector variation was observed as expected, due to the different diode structures implemented in them, but within a sector the noise variations are in the order of a few tens of electrons, with a good stability both in space and in time. In particular, with a bias of −6 V, the noise values before irradiation are in the range 19–34 electrons depending on the diode size and spacing; after irradiation the noise levels move to the range 21–39 electrons, due to charge trapping in the bulk of the sensor. At −6 V the sensor is largely, but not fully, depleted, and in the zone outside the depletion area the charges are still collected by

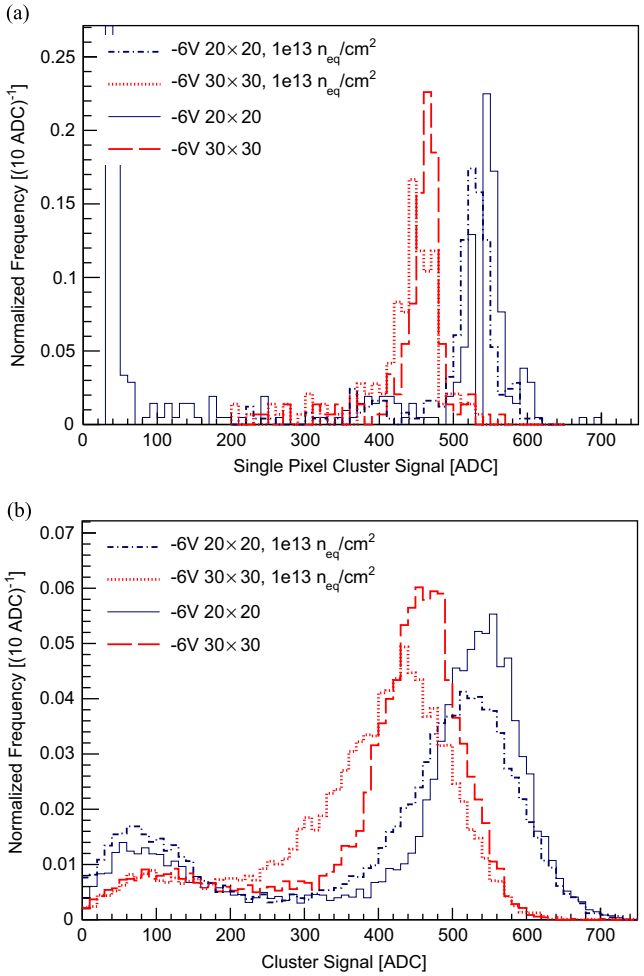

Fig. 2. Measurement of (a) seed signal and (b) cluster signal.

diffusion, with a consequent higher effect of charge trapping after non ionizing radiation.

A signal over noise (SNR) measurement was possible after a test beam at DESY, where the Explorer chip was tested with 4 GeV/c positrons. The SNR depends on the noise value of the sector, on the conversion gain of the circuit and also on the size of the clusters generated by the particles. The SNR values for seed pixels before irradiation, with the chip biased at −6 V, are in the range 18–30 for 20 μm × 20 μm pixels and 17–25 for 30 μm × 30 μm pixels, depending on the diode geometry; these values decrease, respectively, to 17–24 and 12–19 after irradiation.

After all these measurement campaigns, some conclusions can be drawn on the different layouts of the collecting diodes. In general, the 20 μm × 20 μm pixels have a better performance at low reverse bias compared to the 30 μm × 30 μm pixels, because the depleted volume under the collection diode takes a larger fraction of the pixel volume; after irradiation the charge collection efficiency drops by 10–20%, but this drop can be largely recovered by applying a reverse bias to the diode.

The sector that implements the smallest diode of 2 μm diameter, without any spacing between the N-well of the diode and the surrounding deep P-well, has the lowest collection efficiency; this is most probably due to a lateral diffusion of the surrounding deep P-well under the N-well of the diode that is, therefore, partially shielded. A larger size of the N-well does not increase the diode efficiency, because the input capacitance gets larger and the noise also increases. The collection efficiency and the signal over noise can be increased with a larger spacing between the diode

and the surrounding deep P-well; in this configuration, with a reverse bias the depletion under the diode gets wider, and the input capacitance of the diode is reduced. The best performance was obtained on sectors with diodes of 2 μm and 3 μm diameter and a spacing of 1.04–1.54 μm. Their layout is the basis for the subsequent variations of the Explorer chip.

Fig. 3 compares the cluster signals averaged over one sector for the Explorer0 and Explorer1 chips. Moving from Explorer0 to Explorer1 the input capacitance of the readout circuit was reduced from 5 fF to 2 fF. With the same reverse bias of −6 V the Explorer1 chips show an increase in the cluster signal of more than 50% with respect to the previous version, both for the 20 μm and for the 30 μm pixel pitch. In parallel to this signal increase, the noise level has remained approximately the same, so the total signal-to-noise ratio has drastically improved in the new Explorer version.

This significant improvement can be seen in the comparison of the charge detection efficiency between Explorer0 (Fig. 4) and Explorer1 (Fig. 5). These measurements were done in a test beam with 4 GeV/c electrons at DESY, using a stack of four sensors; the tracks were reconstructed into two planes, while a hit extrapolation was searched in a third plane.

The two efficiency plots have the same horizontal axis in number of noise sigma cuts, clearly illustrating the improvement obtained with Explorer1. In Fig. 4 the efficiency drops below 100% already with a cut at 6 sigma over the noise, while in Fig. 5 the plateau is much larger and the detection efficiency is above 99% up to 10 sigma cut. A decrease in the detection efficiency observed on the smaller pitch matrix can be recovered with a higher reverse bias applied to the diode. The fake hit rate for Explorer1 is also shown in Fig. 5 (right axis) and it is very low, below 10^{-5} already for a cut at 6 sigma.

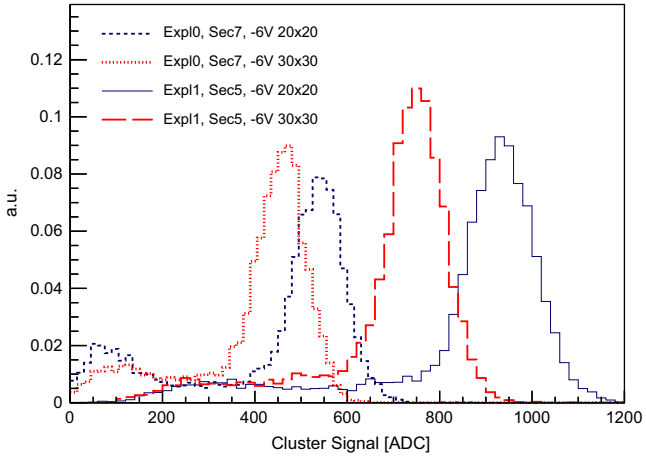

Fig. 3. Comparison of ^{55}Fe cluster signals for Explorer0 and Explorer1.

3. pALPIDE prototype

The pALPIDE chip (prototype *AL* ICE *PI*xel *DE*tector) has been fabricated in March 2013, with a design that is close to a possible architecture of the final chip. The aim of the pALPIDE prototype is to investigate the performance of a front-end with an in-pixel discriminator connected to a sparsified readout circuitry; its functional block diagram is shown in Fig. 6, and an abstract view of the chip with a zoom of a pixel is shown in Fig. 7.

The pALPIDE is organized as a matrix of 64 columns and 512 rows, with a pixel size of 22 μm × 22 μm; the vertical dimension of the chip is 12 mm, close to the real size of the final chip that will be 15 mm according to the specifications. Each column of the chip is divided into an analog section implementing the pixel front-end, and a digital section containing the sparsified readout circuitry implemented as a priority encoder. These two functional blocks communicate by means of STATE signals, which are generated in the pixel front-ends by particles which are crossing the sensors and stored in state registers, and RESET signals, which are sent to the pixels to reset their internal registers after they have been read.

In the analog section of each pixel, the collecting diode is connected to a discriminator and a 1 bit memory cell; when the charge collected by the diode exceeds a certain threshold, the memory, if enabled, is written with a logical 1. The in-pixel discriminator is based on a current comparator circuit that can work with a low bias current of only 20 nA. The discriminator digitizes the analog signal, which therefore does not need to propagate over a long distance, thus reducing the power consumption of the matrix. The output of each comparator is connected to a digital storage element that stores the hit information until the arrival of the RESET signal during the readout phase.

The readout logic is able to read and reset the memory cells of the pixels connected to it; it is designed as an asynchronous priority encoder that is used to read the address of each hit pixel and propagate back the signal to reset it. The priority encoder is structured as a tree in order to decrease as much as possible the length of the lines, thus decreasing their capacitive loads, with the advantages of minimizing the power consumption and increasing the readout speed. One advantage of this type of readout

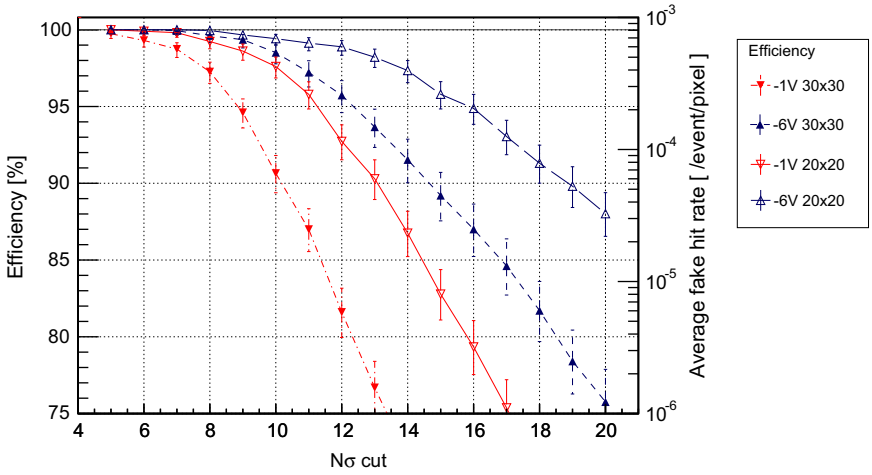

Fig. 4. Charge detection efficiency for Explorer0, for a diode with 3 μm diameter and 1.04 μm spacing (best performance).

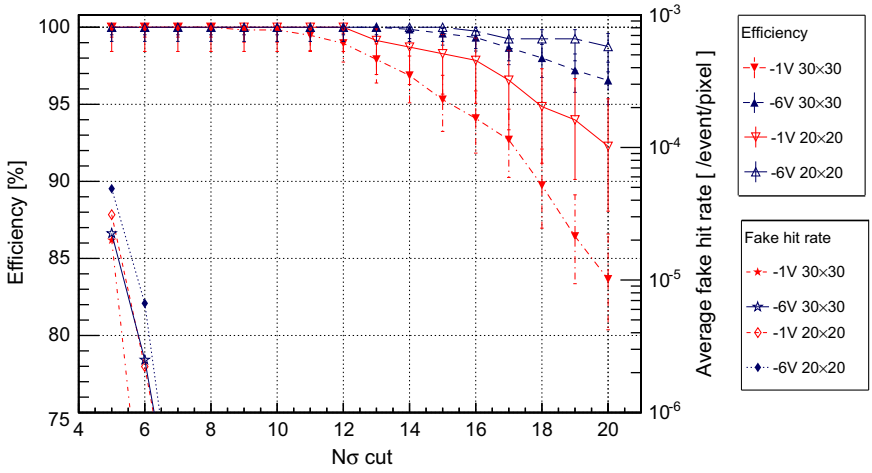

Fig. 5. Charge detection efficiency for Explorer1, averaged on all diode geometries.

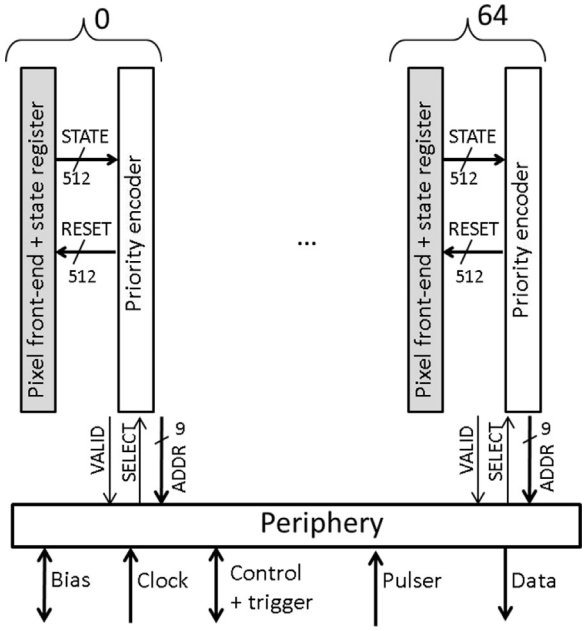

Fig. 6. Functional block diagram of the ALPIDE chip.

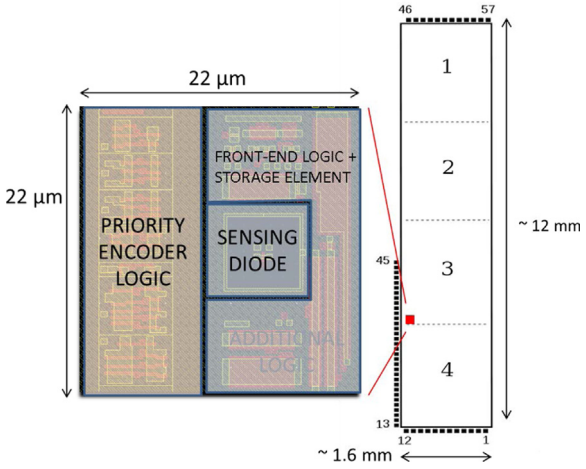

Fig. 7. Schematic view of the pALPIDE chip (right) with a zoom of one pixel (left).

architecture is that it uses completely asynchronous combinatorial logic; the clock runs only in the periphery and is not propagated inside the pixel matrix, resulting in a small power consumption of less than 50 mW/cm^2 during the readout phase and a negligible value when the readout is not activated.

With a sparsified readout, the readout time scales with the chip occupancy, because only the hit pixels are read. With the multiplicities foreseen in ALICE, we expect to have on average less than 1 hit per column, therefore the time needed to read the full matrix is, on average, lower than with a rolling shutter architecture: for central Pb–Pb collisions, the typical time needed to read the full matrix and to transfer the information to the periphery of the chip is in the order of 10 µs. The full hit information is always preserved, because there is no limitation applied on the number of pixels that are read per event.

Outputs of the priority encoders in each column are the addresses (ADDR) of each hit pixel and a VALID signal that is asserted as long as there is a hit pixel in the column that has not yet been read. The periphery circuitry collects the address data from all of the columns and checks all the VALID signals; if the VALID in one column is asserted, then a SELECT signal is propagated back into that column to look for the unread hit pixel with the highest priority, in order to activate the propagation of its address and reset its storage element. At the periphery, one address value is read at every clock cycle, and in the pALPIDE prototype the periphery is equipped with another smaller priority encoder that sends off-chip the hit information of the 64 columns.

The pixel matrix is divided into four sectors, each implementing pixels with a different geometry. The two central sectors, numbers 2 and 3, have been designed with an input capacitance that can be used to send an external pulse to the pixels: two lines per sector are connected to a pulsing line that can be used to pulse all the pixels of these four rows at the same time. The pulse capacitors of the other rows of these sectors are connected to ground. The digital part of the prototype has already been validated by applying a digital pulse to the chip; the readout and the reset scheme work as expected from the design. The full characterization in terms of charge detection efficiency is ongoing and new results will be available soon.

4. Conclusions

The new ALICE Inner Tracking System, to be installed in 2018, will be entirely based on monolithic pixel detectors, to be able to record Pb–Pb collisions at 50 kHz and proton–proton up to 1 MHz collision rates with improved vertexing capabilities. Among the

technical specifications for the new detector, stringent requirements that have justified a dedicated R&D phase are an integration time smaller than 30 μs, a total material budget for the innermost layers of 0.3‰X_0, and a power consumption smaller than 300 mW/cm^2. Several prototypes have been already fabricated in the TowerJazz 180 nm CMOS technology. Chips of the Explorer family, fabricated in different variants and implemented on different substrates, have been tested in terms of charge collection efficiency, noise and charge detection efficiency both with radioactive source and beams of charged particles. The results obtained fully support the chosen approach, and an efficient layout of the collecting diode has been identified. Another prototype, pALPIDE, has also been fabricated with a matrix of pixels read with a sparsified readout based on a priority encoding scheme for the pixel address that also acts as a reset circuitry for the pixel being read. Measurements on this prototype have already been performed by applying a digital pulse to some of the pixels inside the matrix, and the encoding circuitry for the address has been validated.

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