Bias Dependence of Total Ionizing Dose Effects on 28-nm Bulk MOSFETs

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***Abstract*—This paper investigates the effects of total ionizing dose up to 1 Grad on 28-nm bulk MOSFETs under different bias conditions during irradiation. The aim is to assess the potential use of this commercial bulk CMOS technology in the future high-luminosity Large Hadron Collider at CERN that will require highly improved radiation-tolerant tracking systems.**

***Index Terms*—Bias condition, interface traps, narrow-channel effect, 1 Grad, oxide traps, short-channel effect, total ionizing dose, 28-nm bulk MOSFETs**

I. Introduction

CERN's forthcoming high-luminosity Large Hadron Collider (HL-LHC) will require highly improved tracking systems with much more radiation-tolerant front-end (FE) electronics to withstand 1 Grad of total ionizing dose (TID) over ten years of operation [1]–[3]. Nowadays, the aggressive downscaling of CMOS technologies introduces ultra-thin dielectrics into gate stacks that benefits the radiation tolerance of high-performance CMOS circuits [4]–[6]. Meanwhile, TID effects become more complex for nanoscale MOSFETs using hafnium oxide (HfO_2) as the gate oxide and being surrounded by thick shallow trench isolation (STI) oxides [6]. To evaluate the potential use of nanoscale MOSFETs in the HL-LHC, we have been studying a commercial 28-nm bulk CMOS technology up to 1 Grad of TID [7], [8]. This work presents the radiation response of three representative bulk MOSFETs for each type of channel under different bias conditions during irradiation, including the conducting bias condition ($|V_{GB}| = |V_{DS}| = 1.1$ V) and the switched-on bias condition ($|V_{GB}| = 1.1$ V, $|V_{DS}| = 0$). Since a high drain current flows under the conducting bias condition during irradiation, this work also compares the behaviors of irradiated samples to the chips stressed under the same electrical condition for the same duration. Starting with the comparison of transfer characteristics, we then investigate the impact of bias conditions during irradiation on the most sensitive device parameters, such as the threshold voltage, the free carrier mobility, and the drain leakage current. We finally discuss the radiation-induced short-channel (RISCE) and narrow-channel effects (RINCE) on MOSFETs with specific dimensions.

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II. Irradiation and Stress Tests on Transfer Characteristics

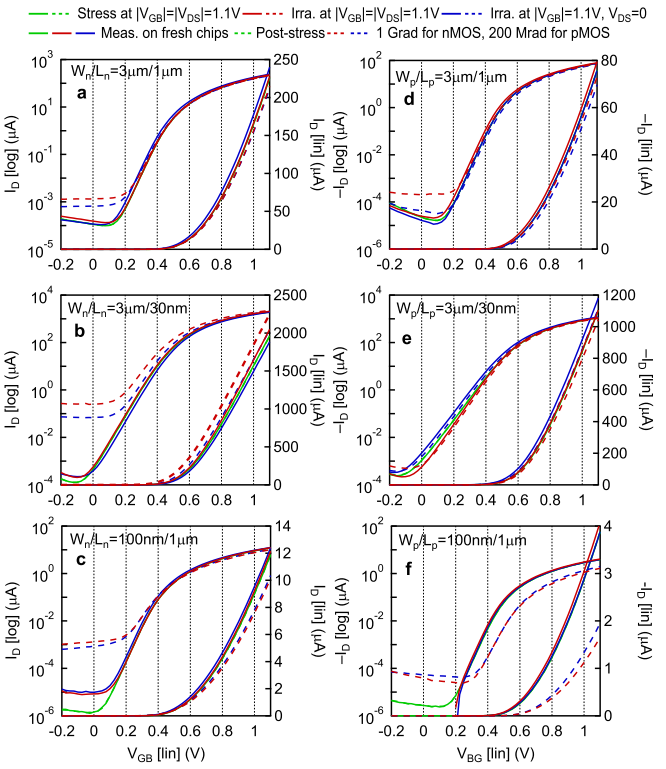

Fig. 1. Transfer characteristics of three representative *n*- (abc) and *p*MOSFETs (def) in saturation ($|V_{DS}| = 1.1$ V). Solid lines are for pre-stress and pre-irradiation, while dashed lines are for post-stress and post-irradiation. Green curves correspond to stress, while red and blue curves correspond to irradiation.

The conducting bias condition has been reported to be the worst bias case for a commercial 65-nm bulk CMOS process [9]. Furthermore, in most analog circuits and particularly the analog FE electronics, MOSFETs are biased in saturation with a nonzero drain-to-source voltage except the switches

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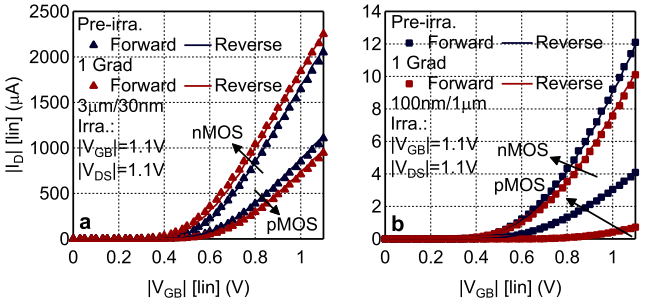

Fig. 2. Transfer characteristics of wide/short- (a) and narrow/long-channel (b) *n*- and *p*MOSFETs in saturation ($|V_{DS}| = 1.1$ V) with respect to pre-irradiation and 1 Grad. The results correspond to the samples irradiated at $|V_{GB}| = |V_{DS}| = 1.1$ V. The samples were measured with drain and source normally configured and interchanged.

working at a zero V_{DS}. Therefore, we start to investigate the effects of TID on this commercial 28-nm bulk CMOS process with this bias condition. The results, plotted as red curves in Fig. 1, demonstrate the strong radiation tolerance of this technology apart from the significant drain leakage current increase of *n*MOSFETs and the significant drive current loss of the narrow/long-channel *p*MOSFET. The corresponding stress test, plotted as green curves in Fig. 1, present a negligible performance loss. Therefore, TID is the main contributor to the observed performance degradation.

The results with the switched-on bias condition are plotted as blue curves in Fig. 1. Considering the chip-to-chip variability, the difference between two different bias conditions is insignificant. Interchanging the roles of drain and source leads to the same results with the normal drain and source configuration, as seen in Fig. 1. Both indicate that the longitudinal electric field has no big influence on the effects of TID on 28-nm bulk MOSFETs. This is different from what is observed for 65-nm bulk MOSFETs from the same foundry [10]. Especially, short-channel MOSFETs fabricated with this 65-nm bulk CMOS technology demonstrate a lower drain current when swapping drain and source. This has been mostly attributed to the charge generation in spacers and the following transport to the gate oxide. The absence of this behavior for 28-nm bulk MOSFETs might be due to an improved spacer processing or a higher energy barrier between SiO_2 for spacers and HfO_2 for gate oxide.

A. Threshold voltage and free carrier mobility

Both *n*- and *p* types of 28-nm bulk MOSFETs demonstrate a limited variation in threshold voltage (Fig. 3a and Fig. 3c) and free carrier mobility corresponding to the drain current drop at a specific overdrive voltage (Fig. 3b and Fig. 3d) except the narrow/long-channel *p*MOSFET. The performance degradation of this *p*MOSFET can be attributed to the significant influence of the charge trapping related to the shallow trench isolation (STI) oxides, which prevents the formation of the *p*-channel along the STI edges and increases its threshold voltage (Fig. 3c). The STI-related charge buildup can also act as Coulomb scattering centers that reduces its free carrier mobility (Fig. 3d). For the narrow/long-channel *n*MOSFET, the

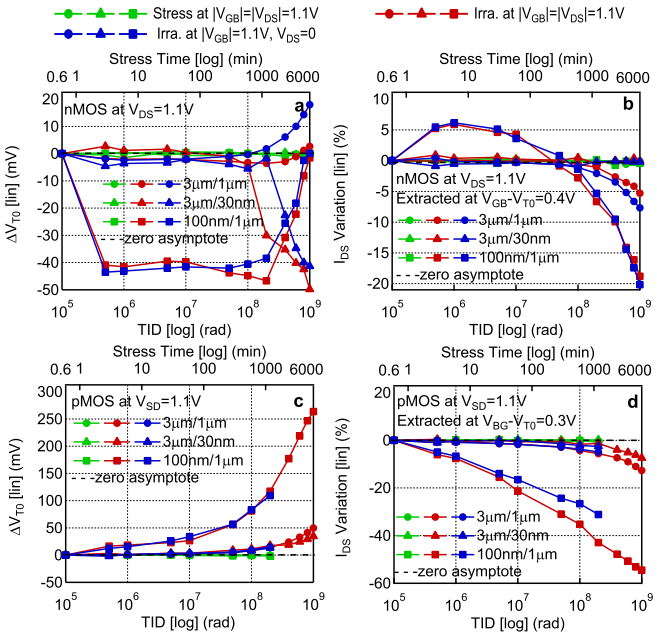

Fig. 3. Variation of threshold voltage (ac) and drain current at a specific overdrive voltage (bd) of *n*- (ab) and *p*MOSFETs (cd) in saturation with respect to total ionizing dose.

negatively charged interface traps counterbalance the positive oxide-trapped charges, which leads to a first decreased and then increased threshold voltage as well as the corresponding mobility degrdation (Fig. 3a and Fig. 3b).

B. Drain leakage current

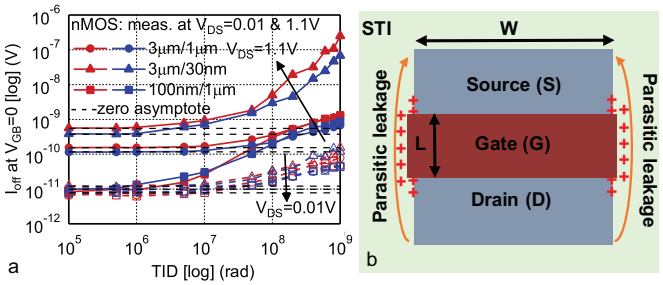

Fig. 4. Drain leakage current of *n*MOSFETs with respect to total ionizing dose (a) and transfer characteristics of the wide/short-channel *n*MOSFET in linear ($|V_{DS}| = 0.01$ V) and saturation ($|V_{DS}| = 1.1$ V) (b).

Fig. 4a demonstrates a significant increase in the drain leakage current of *n*MOSFETs. This is closely related to the positive oxide-trapped charges in the thick STI oxides [11], [12], as seen in Fig. 4b. The I_D-V_{GB} curves at high TID levels are V_{GB}-independent, confirming the dominant contribution of the parallel parasitic *n*-FETs along the STI edges [8]. Fig. 4a also shows that the wide/short-channel *n*MOSFET has the highest drain leakage current increase. Furthermore, Fig. 4a shows an increase up to 1000 times in saturation (solid lines) while around 10 times in linear (dashed lines). This big difference can be due to the drain-induced barrier lowering (DIBL) of the corresponding parasitic *n*-FETs. Fig. 4a also shows similar results from two different bias conditions

during irradiation, which indicate no big influence from the longitudinal electric field on the STI-related charge trapping.

III. Radiation-Induced Short-Channel Effect

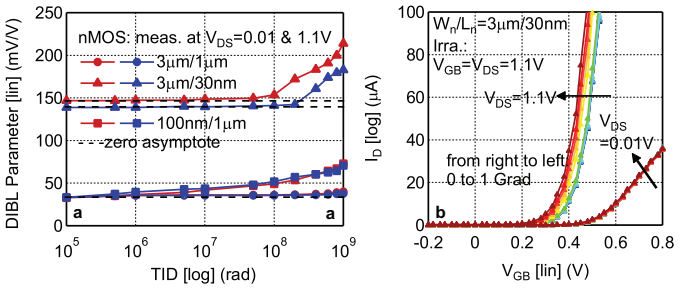

Fig. 5. DIBL parameter of *n*MOSFETs (a) and transfer characteristics of the wide/short-channel *n*MOSFET in linear ($|V_{DS}| = 0.01$ V) and saturation ($|V_{DS}| = 1.1$ V) (b).

The wide/short-channel *n*MOSFET demonstrates the highest increase in DIBL parameter, as seen in Fig. 5a. This radiation-enhanced DIBL is clearly seen in the weak inversion region of the I_D-V_{GB} curves in Fig. 5b, which shows a negative threshold voltage shift in saturation and an almost constant threshold voltage in linear. The channel is depleted of electrons in saturation at the drain side. Owning to the high drain-to-source voltage, the free electrons can be attracted to the drain terminal without being able to tunnel to oxides and neutralize oxide-trapped charges. This leads to a higher threshold voltage shift in saturation than in linear and enhances the DIBL effect.

IV. Radiation-Induced Narrow-Channel Effect

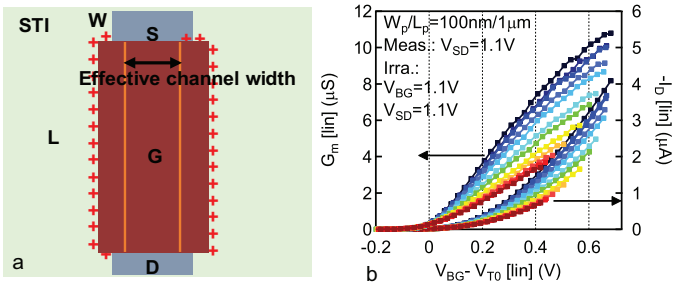

Fig. 6. Top view (a) and transfer characteristics in saturation (b) of a narrow/long-channel *p*MOSFET. Here, "+" refers to the equivalent charge state of both oxide-trapped and interface-trap charges.

The narrow/long-channel *p*MOSFET presents the worst device behavior after 1 Grad of TID. Both the STI-related oxide-trapped and interface-trap charges accumulate electrons along the STI edges, prevent the formation of the *p*-channel, and reduce the effective channel width (Fig. 6a). The charge buildup can also be strong enough to influence the main channel and increase the threshold voltage of the main *p*MOSFET. Furthermore, the G_m and $-I_D$ versus $V_{BG} - V_{T0}$ curves in Fig. 6b evidence the mobility degradation due to the STI-related charges acting as Coulomb scattering centers.

V. Conclusion

TID effects on 28-nm bulk MOSFETs demonstrate a weak dependence on the longitudinal electric field imposed during irradiation. Compared with 65-nm bulk MOSFETs, 28-nm bulk MOSFETs are less sensitive to this longitudinal electric field. This 28-nm bulk CMOS process is rather radiation tolerant except that *n*MOSFETs have a significant drain leakage current increase due to the parasitic *n*-FETs and the narrow/long-channel *p*MOSFET has a significant drive current loss as a result of the strong influence of the STI-related charge trapping. We plan to extend this work by including high-temperature annealing and conducting irradiation tests at different temperature.

Acknowledgements

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