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Influence of Halo Implantations on the Total Ionizing Dose Response of 28 nm pMOSFETs Irradiated to Ultra-High Doses

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***Abstract*— In this work, the Total Ionizing Dose (TID) response of a commercial 28 nm high-k CMOS technology at ultra-high doses is measured and discussed. The degradation of pMOSFETs depends not only on the channel width, but also on the channel length. Short channel pMOSFETs exhibit a higher TID tolerance compared to long ones. We attributed this effect to the presence of the halo implantations. For short channel lengths, the drain halo can overlap the source one, increasing the average bulk doping along the channel. The higher bulk doping attenuates the radiation-induced degradation, improving the TID tolerance of short-channel transistors. The results are finally compared and discussed through Technology Computer-Aided Design simulations.**

***Index Terms*—Total dose effects, 28nm CMOS, MOSFETs, Shallow Trench Isolation, halo, bulk doping, charge trapping, threshold voltage shift, RINCE, high-k dielectric.**

I. Introduction

FUTURE High-Energy Physics (HEP) experiments require chips able to withstand ever-increasing radiation dose levels. It is expected that the luminosity of the Large Hadron Collider (LHC) at the Conseil Européen pour la Recherche Nucléaire (CERN) will be increased by a factor of 10 in the next years. The high-luminosity LHC electronics will experience ultra-high Total Ionizing Doses (TID) up to 1 Grad(SiO_2) over 10 years of operation. The critical area has been identified in the LHC collision points. The upgrade of electronics at A Toroidal LHC ApparatuS (ATLAS) and Compact Muon Solenoid (CMS) is necessary to increase the radiation tolerance of the tracking systems and increase the performance with higher granularity and bandwidth [1] [2].

Research on total dose effects at these ultra-high doses has just started. In recent works [3] [4], the TID response of SiO_2-based 65 nm CMOS technology was studied up to 1 Grad(SiO_2), in connection with the process variability [5]. In these devices, the radiation-induced degradation was stronger in narrow-channel transistors. This effect was called Radiation-Induced Narrow-Channel Effect (RINCE) [6] and it is related to charge buildup in Shallow Trench Isolation (STI) oxide and its interface [7]. RINCE increases the leakage currents due to the activation of parasitic transistors in n-channel MOSFETs and induces a parametric drift in narrow n and p-channel MOSFETs.

Another concern of modern bulk MOSFETs is the radiation-induced degradation of the spacer oxides and of the overlying silicon nitride layers above the Lightly Doped Drain (LDD) extensions [8]. The charge buildup in the spacer dielectrics leads to an increase of the parasitic series resistance and to a reduction in the drive current. The worst case was found in short-channel transistors and is known as Radiation-Induced Short-Channel Effect (RISCE) [9].

In addition, the scaling limits of SiO_2 [10] have required the introduction of high-k dielectric materials [11]. Consequently, the research interests of the HEP community have moved towards the evaluation of the high-k gate oxide response at ultra-high radiation levels. In a recent publication [12] [13], HfO_2-based MOSFETs were investigated up 1 Grad(SiO_2), but additional work is still needed to characterize the sensitivity of HfO_2-based MOSFETs exposed to ultra-high doses.

Finally, in sub-micron technology nodes, halo implantations are extensively used to reduce Short Channel Effects (SCEs) [14]. Halo implantations in Ge-based MOSFETs use a high doping level. When such devices are irradiated up to 1 Mrad(SiO_2), they exhibit an increase in the off leakage, enhanced interface-trap buildup and greater 1/f noise [15] [16]. The influence of the halo on radiation-induced effects in Si-

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based MOSFETs was studied in a few publications. Most of the studies [17] [18] were focused on the development of analytical models that describe the increase in the off-state leakage current in nMOSFETs, considering the charge buildup in the STI and the process variation of the doping profile along the sidewall regions of STI. It has been found that the high variability on the radiation-induced leakage current in nMOSFETs is caused by the statistical variation of the doping implantation process in the regions close to the STI [19]. In particular, [18] showed through simulations that the radiation-induced leakage current decreases in 90-nm nMOSFETs, when the doping along the STI sidewalls is increased. Similar results were also obtained in a recent work [20], where radiation-induced STI effects were modelled as a function of the halo implants. In this case, it was demonstrated that the higher doping of halo implantation reduces the magnitude of the radiation-induced off-state leakage currents in nMOSFETs. Therefore, the radiation sensitivity of nMOSFETs can be largely affected by variations in the doping of halo implantation.

In this work, we evaluate the radiation-induced effects on 28 nm pMOSFETs with high-k oxides at ultra-high doses. The RINCE effect is studied, showing new experimental evidence pointing to the strong influence of the halo implantation on the TID response of pMOSFETs.

II. Experimental Details

A. Test Structures

The Devices Under Test (DUTs) were manufactured with a commercial 28-nm bulk CMOS process using high-k gate dielectric. Transistors were designed for core applications with a nominal operating voltage of 0.9 V. The DUTs were provided in an array structure, containing pMOSFETs with several gate lengths (L_{min}=30 nm, L_{max}=1 um) and gate widths (W_{min}=100 nm, W_{max}=3 um). The transistors had separated drain and gate contacts, while they shared the source and bulk contacts. The gate terminals were protected by ESD protections designed in a two-diodes configuration. A customized probe-card allowed us to bias 10 different transistors at the same time during the exposure, while a switching matrix selected the transistors to connect to the measurement system.

B. The halo implantations

The 28 nm pMOSFET structure is represented schematically in Fig. 1. The bulk doping along the channel is not uniform due to the halo implantations and the doping profile depends on the channel length. In short channel transistors the drain halo implantation can overlap with the source one [21], causing an increase in the overall channel doping. In the shortest channel transistors, the overlap of halos can induce a doping peak in the center of the channel, which increases abruptly the threshold voltage of the short transistors [22]. The rise of the threshold voltage with decreasing channel-length is called Reverse Short Channel Effect (RSCE) [23], and characterizes scaled CMOS technologies with high halo doping concentration.

Fig. 2 shows the threshold voltage V_{th} of the pMOSFETs before the exposure. The V_{th} is plotted as a function of the channel-length for transistors with channel-width of 100 nm and 3 um. The trend of the V_{th} vs. L is characterized by an

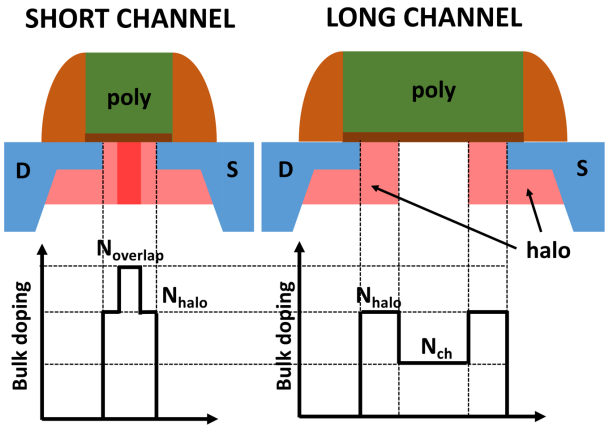

Fig. 1. 28 nm pMOSFET structure with non-uniform doping distribution of the bulk due to the halo implantations. In short-channel transistor the drain halo can overlap with the source one, whereas in long channel transistor halos are confined in the lateral regions of the channel.

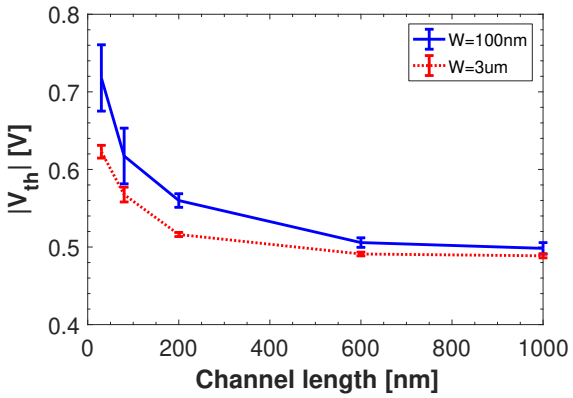

Fig. 2. The threshold voltage V_{th} of fresh pMOSFETs under test are plotted as a function of the channel length for different channel width. Measurements are carried out at room temperature in linear region ($|V_{ds}|$=0.1 V).

evident RSCE, indicating highly doped halo implantations and low substrate concentration, which cause the increase of the V_{th} in short-channel transistors. The abrupt increase of the V_{th} for L<100 nm suggests that the drain halo starts to overlap the source one when L is reduced below 100 nm.

Finally, Fig. 2 evidences a V_{th} dependence with transistor width. This effect is caused by the gate fringing field in the channel corner edge with the STI and is called Narrow-Width Effect (NWE) [24].

C. Exposure Conditions and Measurements Details

The irradiation tests were performed at the University of Padova using an X-ray irradiator composed by a tungsten tube with peak energy deposition at 10 keV [25]. In order to reach ultra-high doses up to 1 Grad(SiO_2), the dose rate was set to 5.12 Mrad/h(SiO_2). After the exposure, transistors were annealed at 100 °C for 24 hours. During the irradiation and the annealing, all transistors of the array structure were biased in one of the following configurations: “diode” ($|V_{gs}|$=1 V, $|V_{ds}|$=1 V), “on” ($|V_{gs}|$=1 V, $|V_{ds}|$=0 V) and “off” ($|V_{gs}|$=0 V, $|V_{ds}|$=0 V). The measurements were performed on 23 samples up to different cumulated dose. At least two different devices of each type were evaluated for all experimental conditions, with typical results shown below. The static characteristics of the

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transistors were measured with a semiconductor parameter analyzer (HP 4156) before the exposure, at several irradiation steps and after the annealing.

III. Radiation Test Results

In the following section, the TID response of pMOSFETs is reported by measuring the DC static characteristics and extracting the main parameters: drive current variation (ΔI_{on}), threshold voltage shift (ΔV_{th}), degradation of the transconductance (Δg_m) and subthreshold swing variation (ΔSS). The I_{on} current is defined as the drain-to-source current in linear region ($|V_{ds}|$=0.1 V) when the channel is in strong inversion at $|V_{gs}|$=1 V. The threshold voltage V_{th} is extracted by the linear region (ELR) method [26], as the gate voltage axis intercept of the linear extrapolation of the I_d-V_{gs} characteristics at its maximum first derivative point.

A. TID response

Fig. 3 reports the I_d-V_{gs} characteristics at $|V_{ds}|$=0.1 V of pMOSFETs with three different channel sizes: (a) W/L=100/30 nm, (b) W/L=100/1000 nm and (c) W/L=1000/1000 nm. The transistors were irradiated at room temperature up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours. Both during the exposure and the annealing, the transistors were biased in the "diode" configuration. In all tested pMOSFETs, the drive current decreases with cumulated dose and the threshold voltage shifts to lower values. The pMOSFET with long and wide channel (c) exhibits the highest TID tolerance, showing a $\Delta|I_{on}|$ variation of -15% at 1 Grad(SiO_2). The worst TID degradation was found in the narrow and long channel transistor (b), which exhibits a $\Delta|I_{on}|$ decrease of -78% at 1 Grad(SiO_2). While the shortest and narrowest pMOSFET (a) has a $\Delta|I_{on}|$ degradation of -40%, which is half of the large and narrow channel transistor.

The off-state drain leakage current of all pMOSFETs increases of more than an order of magnitude after 1 Grad(SiO_2).

The black dash-dotted lines indicate the TID responses of the transistors after 24 hours at 100 °C. Transistors with narrow channel show a visible recovery after the annealing. The annealing measurement after 1 Grad(SiO_2) is not available for the shortest pMOSFET, due to the long exposure time combined to the difficulties related to its high sensitivity to electrostatic discharges. The TID response of the shortest transistor after the annealing is evaluated at lower cumulated doses in the next section.

Fig. 4 shows the TID degradation of pMOSFETs of different gate areas. Similarly to Fig. 3, the transistors were irradiated at room temperature up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours in the "diode" configuration. The degradation of the $\Delta|I_{on}|$ evidences that the narrowest transistors (W=100 nm) are the most sensitive to TID. Narrow and large transistors with L>=200 nm degrade almost equally, $\Delta|I_{on}|$ is about -80% after 1 Grad(SiO_2). Whereas, narrow and short transistors with L<100 nm exhibit a channel-length dependence, with the shortest transistor (L=30 nm) having the smallest degradation. Focusing on this channel length dependence of narrow transistors, after 1 Grad(SiO_2), pMOSFETs with L=30 nm, 80 nm and 100 nm exhibit

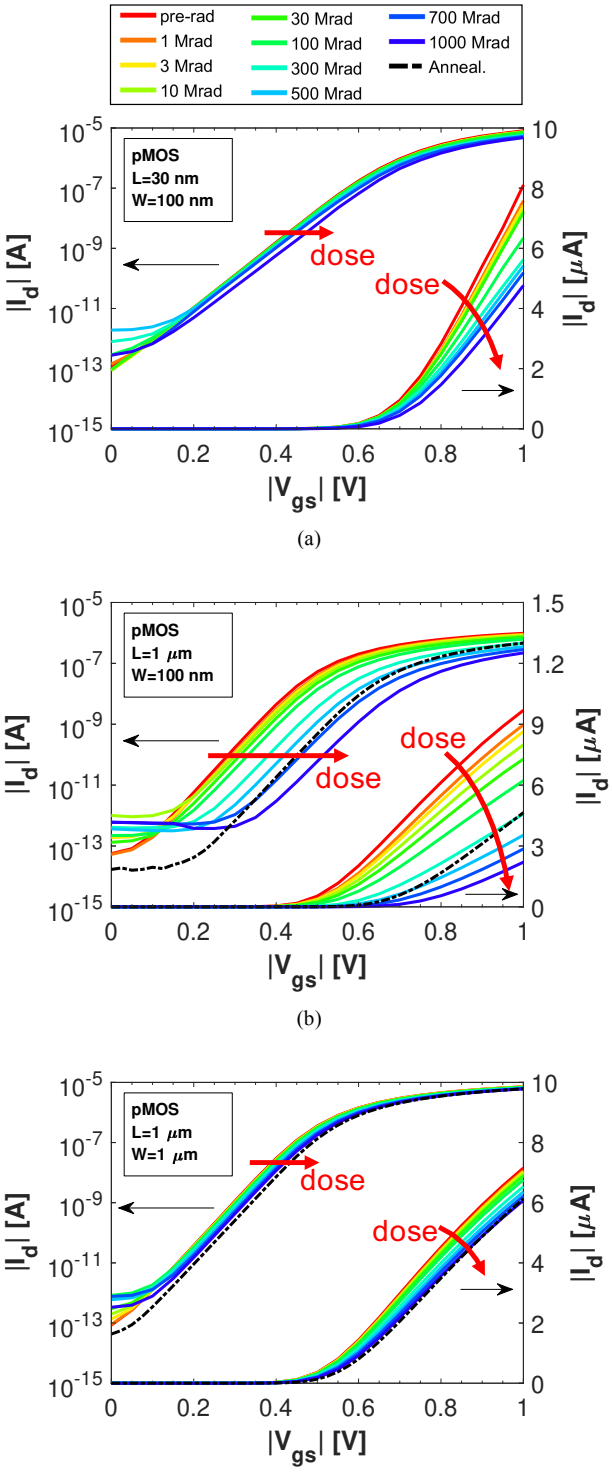

Fig. 3. Degradation of the I_d-V_{gs} in linear region ($|V_{ds}|$=0.1V) of pMOSFETs irradiated at room temperature up to 1 Grad(SiO_2) and then annealed for 24 hours at 100°C in the "diode" configuration. (a) W=100 nm, L=30 nm. (b) W=100 nm, L=1000 nm. (c) W=1000 nm, L=1000 nm.

respectively a $\Delta|I_{on}|$ degradation of -40%, -63% and -82%. The length-dependent effect is visible at high doses, since 10 Mrad(SiO_2), and is dominant at ultra-high doses over 100 Mrad(SiO_2).

As visible in Fig. 4(b) and Fig. 4(c), the decrease of the drive current I_{on} is caused by a degradation of both V_{th} and g_m. The channel-length dependence of the degradation of $\Delta|I_{on}|$ is visible

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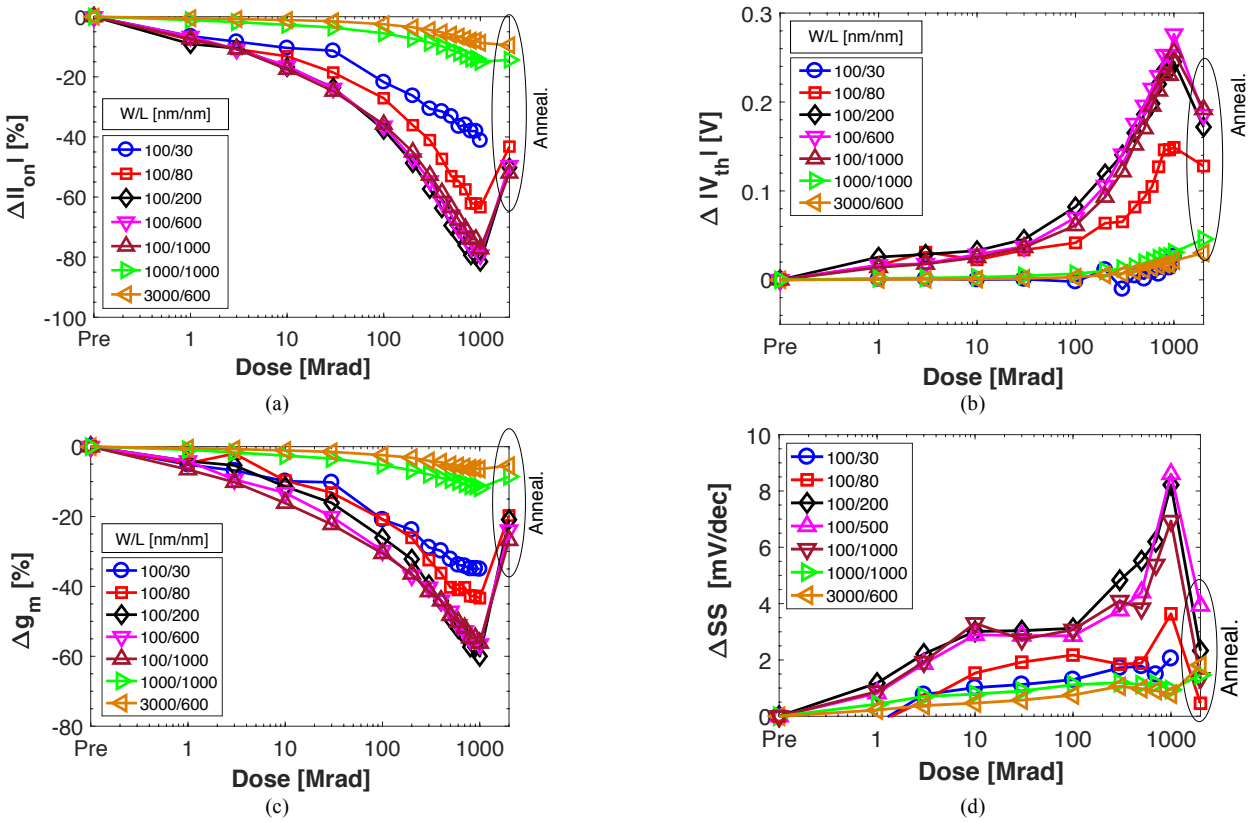

Fig. 4. Summary of the main parameters degradation of pMOSFETs irradiated up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours in the "diode" configuration. All measurements were carried out in linear region ($|V_{ds}|$=0.1 V) and at room temperature. (a) Drive current $\Delta|I_{on}|$. (b) Threshold voltage $\Delta|V_{th}|$. (c) Transconductance Δg_m. (d) Subthreshold swing ΔSS.

also on the Δg_m and in particular on the $\Delta|V_{th}|$. The pMOSFETs exhibit a $\Delta|V_{th}|$ degradation of -20 mV, -140 mV and -280 mV respectively on transistors with L=30 nm, 80 nm and 200 nm.

Finally, Fig. 4(d) shows the variation of the subthreshold slope as a function of the dose. The ΔSS is almost negligible, less than 9 mV/dec after an exposure of 1 Grad(SiO_2). The worst case is the narrowest channel transistors with ΔSS of about 9 mV/dec, whereas all other channel geometries exhibit a ΔSS of less than 2 mV/dec.

B. *Channel-width dependence*

Fig. 5 highlights the TID degradation of I_{on} as a function of the channel width for pMOSFETs irradiated with different bias conditions. Only long channel transistors are taken into account to minimize short channel effects. The worst-case bias conditions were the "diode" and "on" modes, in which the gate-to-bulk voltage is maximized. In all bias conditions and at both high doses (10 Mrad(SiO_2)) and ultra-high doses (400 Mrad(SiO_2)), the degradation is channel-width dependent. Narrow channel transistors exhibit a lower TID tolerance compared to long channel pMOSFETs. At 400 Mrad(SiO_2) in the worst-case "diode" bias, the I_{on} of the narrowest channel transistor degrades of about -60%, while the largest channel transistor degrades of about -7%. However, the TID tolerance is improved in the "off" irradiation bias condition, with a degradation of -30% at 400 Mrad(SiO_2) in the narrowest channel pMOSFET. A similar width dependence was reported also in [12].

C. *Channel-length dependence*

The channel-length dependence is one of the most interesting result of this work. Fig. 6 shows the TID degradation of the I_{on} as a function of the channel length in narrow channel pMOSFETs irradiated in different bias conditions. The worst-case bias was found in the "diode" and "on" conditions, whereas the TID sensitivity in "off" condition is half compared to the "diode" and "on" configurations.

Transistors with L<100 nm exhibit a channel-length dependence. The TID tolerance of short-channel transistors is improved if compared to the long channel transistors. At 400 Mrad(SiO_2), in the worst-case "diode" bias, the I_{on} of the shortest transistor degrades of -27%, while the longest channel transistor degrades of -60%. However, p-channel transistors with L>100 nm do not show any channel-length dependence, showing a constant degradation around -60%. This short-channel effect is visible only in narrow channel transistors at both very high doses (10 Mrad(SiO_2)) and ultra-high doses (400 Mrad(SiO_2)).

D. *High temperature annealing*

Fig. 7 reports the degradation of the I_{on} during the exposure up to 500 Mrad(SiO_2) and during the 24 hours of annealing at 100 °C in the "diode" bias mode. The first and last measurements reported in the annealing plot were carried out at room temperature, whereas the others in the red span were carried out at 100 °C. The large difference between the first and the second points in the annealing plot is mainly related to the

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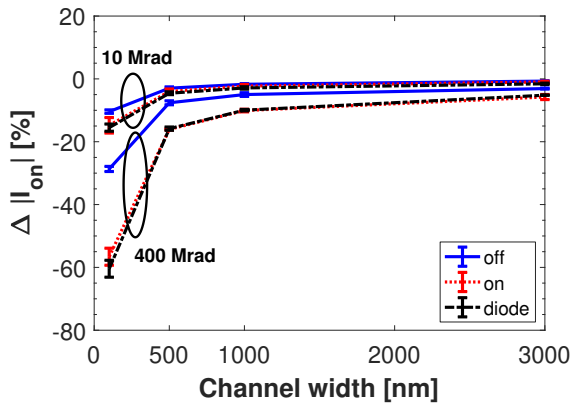

Fig. 5. Degradation of the I_{on} in linear region ($|V_{ds}|$=0.1 V) as a function of the channel width for long channel pMOSFETs (L=1 um, except W/L=3000/500 nm), irradiated in different bias conditions at room temperature.

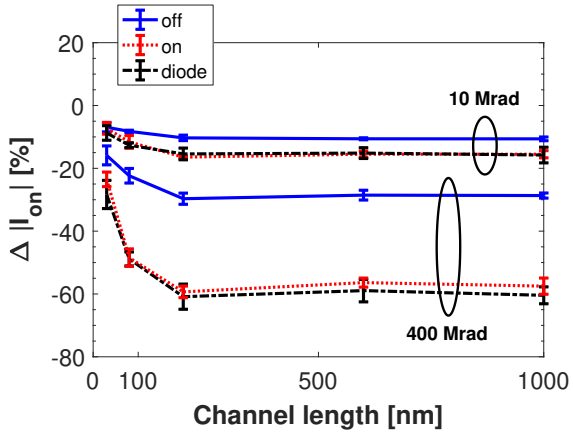

Fig. 6. Degradation of the I_{on} in linear region (($|V_{ds}|$=0.1 V) as a function of the channel length for narrow channel pMOSFETs (W=100 nm), irradiated in different bias conditions at room temperature.

effects of high temperature, which generally causes a reduction of the threshold voltage and of the carrier mobility.

The annealing evolution is very fast during the first hour at high temperature. After 24 hours at 100 °C, narrow transistors recovers part of the degradation caused by the exposure. The highest recovery of the response is found in the narrowest (W=100 nm) and long (L>100 nm) transistors, which exhibit a $\Delta|I_{on}|$ of about -70% after the exposure and a $\Delta|I_{on}|$ of -40% after the annealing. The $\Delta|I_{on}|$ of shortest channel transistors degrade of -30% after the exposure and recovers up to -18% after the annealing. In these devices the recovery of the TID response is mainly due to a large improvement of the transconductance. On the contrary, the TID response of wide transistors after the annealing is almost negligible or, even, of the opposite sign, such as for pMOSFETs with W=3000 nm.

IV. Discussion

The gate oxide of HfO_2-based MOSFETs consists in a relatively thick layer of HfO_2 built over a very thin layer of SiO_2. Therefore, in HfO_2-based MOSFETs the interface between the dielectric and the substrate is composed by the well-known SiO_2/Si materials. The experimental results evidence a negligible subthreshold slope variation of 28 nm pMOSFETs with the accumulated dose, regardless of the length of the transistor, and a very small degradation in devices with large width. This result indicates a very small generation of interface traps along the channel interface and a very limited amount of charge buildup in the gate oxide, confirming the robustness of the SiO_2/Si interface and not highlighting any issue with the high-k layer.

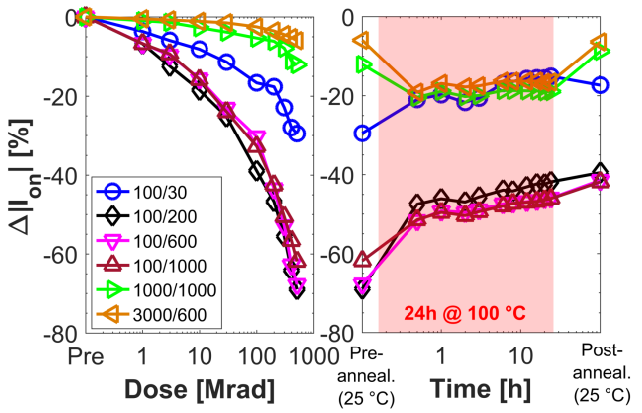

Fig. 7. The I_{on} variation ($|V_{ds}|$=0.1 V) of pMOSFETs irradiated up to 500 Mrad(SiO_2) and then annealed at 100 °C for 24 hours in the "diode" configuration. Measurements in the red space were carried out at 100°C, whereas the others in the white background were carried out at room

A. STI-related effects

The width-dependence of the degradation suggests that the charge trapping in the gate dielectric is not the dominating radiation-induced effect. In p-channel MOSFETs, the positive trapped charges in the STI oxide can buildup an electric field capable of depleting the lateral edges of the transistor channel. This reduces the effective channel width, concurrently decreasing the threshold voltage $|V_{th}|$ of the transistor [6]. Consequently, the width-dependent degradation found in 28 nm pMOSFETs can be related to the STI charge buildup, proving the sensitivity of 28 nm pMOSFETs to the RINCE effects.

Moreover, the results show that the worst-case bias conditions are the "diode" and "on" modes, in which the gate-to-bulk voltage is maximized. This is in agreement with the simulations in [20], which demonstrated that the charge trapping generation in the STI oxide rises by increasing the gate-to-bulk electrical field. This result differs from the past literature about TID effects on pMOSFETs [27], where the worst-case bias condition for p-channel MOSFETs was the "off" state. This difference is attributed to the different nature of the radiation-induced damage. Older CMOS devices were usually dominated by the gate oxide charge buildup, which is maximized in the "off" bias condition. On the contrary, 28 nm pMOSFETs are dominated by STI degradation, which tends to be maximized in the "diode" and "on" conditions.

The recovery of the TID response of narrow transistors is fast during the high temperature annealing test and it is related to the recombination of the positive charge trapped in the STI. The largest transistors exhibit a slight degradation after annealing, due to the generation of interface traps along the gate oxide interface and due to their low sensitivity to STI effects.

The observed variation of the off-state leakage current is probably due to the peripheral drain to substrate junction leakage current. This current is associated to the surface generation at the intersection of the depletion region and the STI sidewalls, where a high density of interface traps is located [28]. The slight variation of the SS suggests that interface trap

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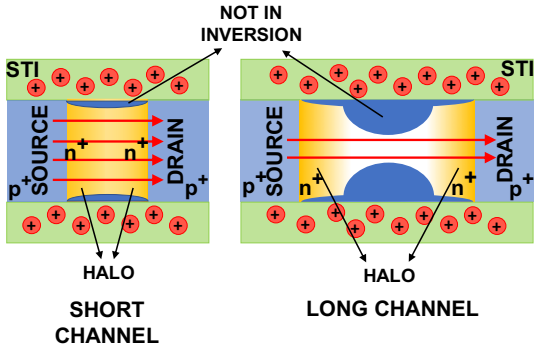

Fig. 8. Schematic view of the influence of the halo regions on the TID response of short and long channel pMOSFETs.

generation is limited to the STI sidewalls and does not extend along the gate oxide/bulk interface.

B. *Halo influence*

One of the most interesting result of this work is the observed length dependence, which is opposite to the Radiation-Induced Short-Channel Effect (RISCE) affecting the 65 nm node [9].The absence of the RISCE in both narrow and large transistors suggests an improvement of the robustness of the spacers in 28 nm technology, but it is not clear if it is due to the high-k materials or to the fabrication process.

We think that one possible explanation of the decreased sensitivity at short gate lengths is the influence of the halo implantations used in modern CMOS processes [29]. Large implant doses and energies in the halo regions can induce a positive $|V_{th}|$ shift, known as V_{th} roll-off [11]. This effect is evident in short channel transistors, where the halo implantations can slightly overlap each other, increasing the average doping of the channel region. By analyzing the pre-rad $|V_{th}|$ of 28 nm pMOSFETs (Fig. 2), the V_{th} roll-off is visible, and it increases abruptly on the pMOSFETs with L<100 nm, indicating that in these transistors the halo implantations increase the overall channel doping.

In recent studies based on device simulation [17] [18], it was demonstrated that the doping of the bulk regions close to the STI edge can drastically modify the TID tolerance of nMOSFETs. In nMOSFETs the positive trapped charges in the STI invert the lateral edges of the transistor channel, forming a parasitic n-channel FET [6]. An increase of the bulk doping in the regions close to the STI edge can lead to an improvement of the TID response of the nMOSFET, as the electrical field generated by the trapped charge in the STI is not able to invert the lateral channel regions. As a consequence, the off-state leakage current of the nMOSFETs decreases. We think that these results can be applied to the pMOSFETs as well. On pMOSFETs the increase of the bulk doping in the regions close the STI edge can reduce the depleted lateral region responsible for RINCE. Consequently, the width reduction of the irradiated transistor is limited, leading to an increase of the TID tolerance of the pMOSFETs. Fig. 8 shows a schematic top view of narrow pMOSFETs in the channel region. The green regions represent the STI oxides, filled by the buildup of positive trapped charges. The color gradient in the yellow regions denote the halo implantations, which almost overlap in the short-channel transistors. The dark-blue areas are the regions which do not reach strong inversion due to the influence of the STI trapped charges and are responsible of the reduction of the effective transistor width.

V. Simulations

In this paragraph, the experimental results are compared with Technology Computer-Aided Design (TCAD) Sentaurus simulations. The 28 nm pMOSFETs are simulated by adopting a 3D structure with halo implantations and STI. Simulations presented in this work aim to support the interpretation of the length dependence of TID effects. The radiation damage is simulated by inserting a volumetric concentration of fixed positive charges in the STI oxides, allowing to study the TID effects during the irradiation.

A. *Simulation approach and goals*

The manufacturer does not provide any information of the

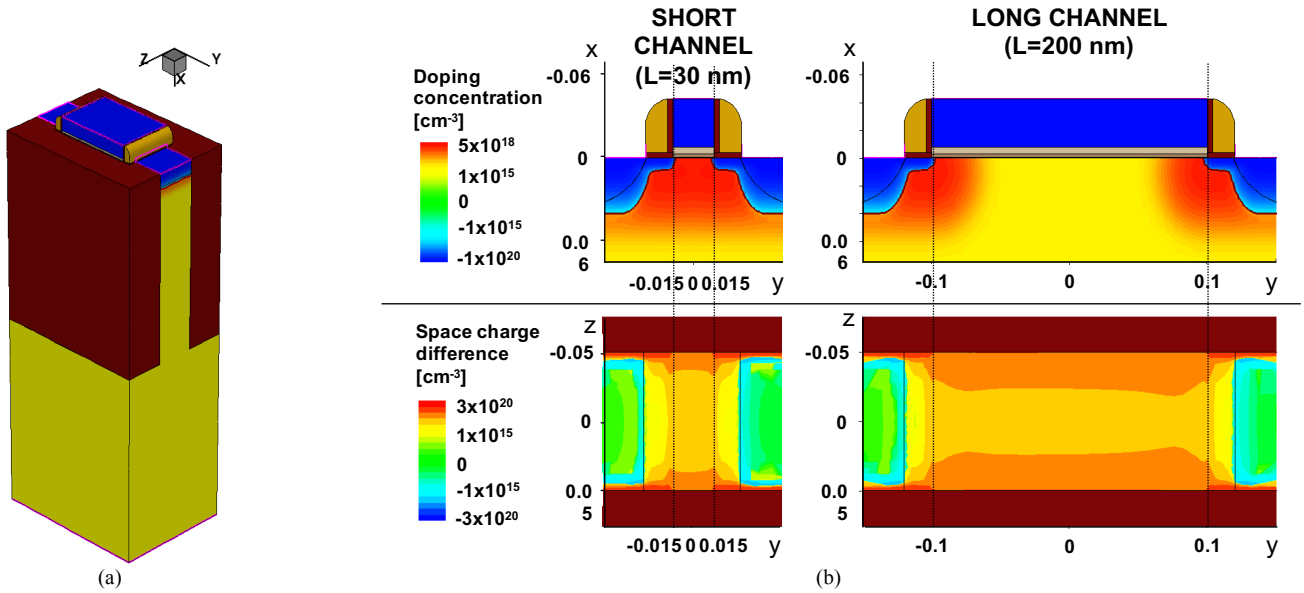

Fig. 9. The 3D TCAD simulations of the 28 nm pMOSFETs. (a) The simulation are based on a 3D structure, implementing STI and halo regions. (b) In the first row, a cut plane at z=0 um shows the doping concentrations in short and long channel pMOSFETs. In the second row, cut plane at x=2 nm shows the delta space charge density, calculated as the difference of the space charge density between pre-rad and irradiated devices in short and long channel pMOSFETs.

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fabrication process, such as doping concentrations and materials. For this reason, the simulated device structure was designed on the basis of publicly available information and agreement with the experimental characterization of the pre-rad devices. For example, the high-k gate dielectric thickness was estimated by the gate capacitance of a p-channel varactor. Supposing a thickness of the SiO_2 layer of about 0.7 nm, the thickness of the HfO_2 layer is 2 nm.

Fig. 9(a) shows the simulated 3D structure of a pMOSFET with L=200 nm. In the top part of Fig. 9(b), a cut plane at z=0 um shows the doping concentration in the short channel and long channel pMOSFETs. The highly doped regions in red color identify the halo implantations, which almost overlap each other in the short channel transistor with L=30 nm. In the bottom part of Fig. 9b, the plots have been obtained at a horizontal cut plane at x=0.002 um, which is 2 nm beyond the SiO_2/Si interface. The transistors are simulated in linear region with $|V_{ds}|$=0.1 V and $|V_{gs}|$=1 V. The plots report the concentration difference of the space charges between a fresh device and an irradiated device. The irradiated device is simulated by inserting a uniform volumetric density of positive charges Q_{STI}=3x10^{18} cm^{-3} in the STI, equal to 8x10^{12} cm^{-2} along the STI sidewalls, which is comparable to the charge densities of other previous works [17].

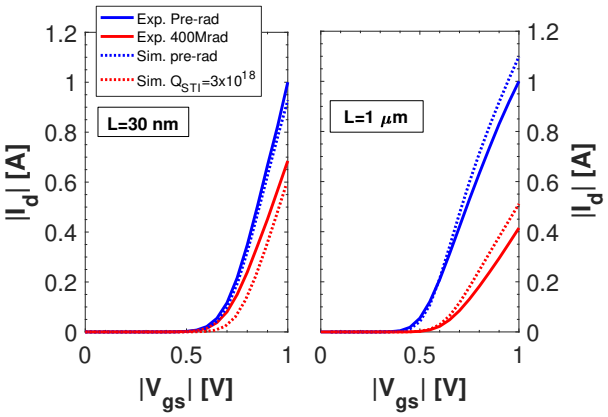

Fig. 10. The simulated DC characteristics are compared to experimental measurements for $|V_{ds}|$=0.1 V before and after the exposure for pMOSFETs with W=100 nm. (a) L=30 nm. (b) L=1 um. Irradiated devices are simulated by inserting a uniform density of positive charges Q_{STI}=3x10^{18} cm^{-3} in the STI.

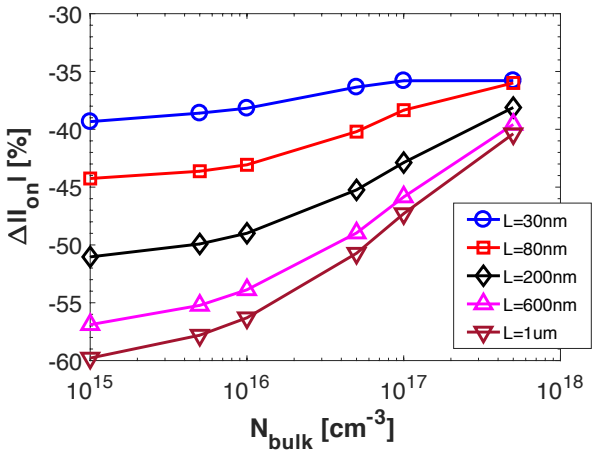

Fig. 11. The degradation of the I_{on} in linear region ($|V_{ds}|$=0.1 V) is simulated by TCAD. Irradiated devices are simulated by inserting a uniform density of positive charges (Q_{STI}=3x10^{18} cm^{-3}) in the STI. The $\Delta|I_{on}|$ is plotted as a function of the bulk doping for different channel length transistors, while the doping of halo implantations is constant ($N_{halo\text{-}peak}$=3.2x10^{18} cm^{-3}).

The decrease of the space charge regions close to the STI is larger in the long-channel pMOSFET than in the short-channel one. The smooth increase of the space charge difference visible close to y=-0.1 um and y=0.1 is due to the higher doping of halos. In the short channel transistor, the high doping of the halos reduces the space charge degradation along the entire channel. Simulations confirm that the degradation of the carrier concentration due to the STI fixed charges is reduced in short-channel transistors, where the channel doping is dominated by the high concentration of the halo implants.

Fig. 10 compares the simulated I_d-V_{gs} with the experimental values for the shortest and longest pMOSFETs with W=100 nm. In the simulations, the fixed charge in the STI causes a degradation of the V_{th} and of the g_m, which is comparable to the experimental measurements.

Fig. 11 shows the simulated degradation of the I_{on} in pMOSFETs with different channel lengths at several bulk doping concentrations. The irradiated transistor is simulated by inserting a volumetric uniform density of positive charges of 3x10^{18} cm^{-3} in the STI. Only the bulk doping is varied, whereas halo implantations are constant with $N_{halo\text{-}peak}$=3.2x10^{18} cm^{-3}.

This plot clearly evidences the influence of the bulk doping on the transistor TID response. The TID effects in long channel transistors decrease by increasing the doping of the bulk. The pMOSFET with L=1 um exhibits a degradation of -60% when the bulk is doped at 10^{15} cm^{-3} and decreases to -40% when the bulk concentration is raised to 5x10^{18} cm^{-3}. On the contrary, the TID degradation of short channel transistors is almost insensitive to the bulk doping concentration. At 10^{15} cm^{-3}, the $\Delta|I_{on}|$ of pMOSFET with L=30 nm is -39% and slightly decreases to -36% at 5x10^{18} cm^{-3}.

This demonstrates that the increase of the bulk concentration improves the TID radiation response. In short channel transistors, the insensitivity of the TID response with bulk doping is due to the high doping of the halo implantations, which increase the overall concentration along the entire channel, independently from the bulk concentration.

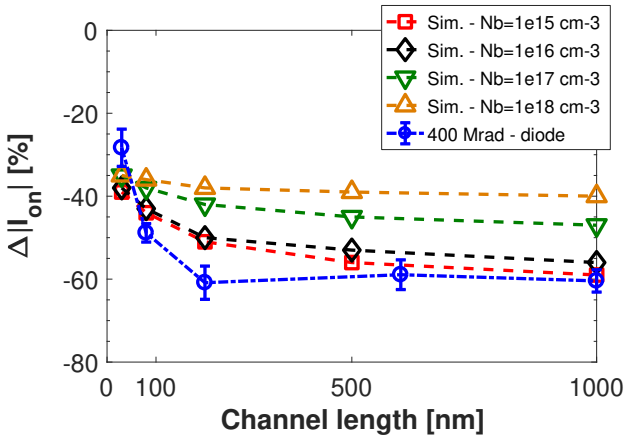

Fig. 12. The experimental degradation of the I_{on} in linear region ($|V_{ds}|$=0.1 V) at 400 Mrad(SiO_2) in the "diode" bias configuration is compared to simulations at different channel lengths. Irradiated devices are simulated by inserting a uniform density of positive charges (Q_{STI}=3x10^{18} cm^{-3}) in the STI. Simulations are carried out for different bulk concentrations, while the doping of halo implants is constant ($N_{halo\text{-}peak}$=3.2x10^{18} cm^{-3}).

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Finally, Fig. 12 evidences the channel-length dependence of the TID in simulations and experimental measurements. The plot compares the experimental and simulated $\Delta|I_{on}|$ degradation as a function of the channel length. The simulated curves are obtained similarly to Fig. 11. Here, the channel-length dependence of the $\Delta|I_{on}|$ is clearly visible in the simulations and follows the experimental trend. The not perfect match between simulations and experimental values can be due to the differences in the STI edge profile, in the STI corner rounding, in the position and quantity of trapped charges. Moreover, when the bulk doping N_{bulk} is increased, the channel-length dependence is reduced and it disappears at $N_{bulk}\approx10^{18}$ cm^{-3}, which is comparable to the peak doping of the halos $N_{halo-peak}$=3.2x10^{18} cm^{-3}.

In conclusion, TCAD simulations highlight the influence of the bulk doping on the transistor TID response. High doping regions in the bulk attenuate the effects induced by the charge buildup in the STI. This attenuation is larger in short-channel pMOSFETs due to the overlap of the halo regions.

VI. Conclusion

The degradation of 28 nm pMOSFETs exposed to ultra-high doses is dominated by the STI charge buildup effects. We found out that in narrow-channel transistors the TID response of pMOSFETs is channel-length dependent. Short-channel transistors show lower radiation-induced degradation than long channel ones. Modern CMOS technologies employ the halo implantations, highly doped bulk regions close to the extensions. In short channel transistors, the source and drain halo implantations can overlap each other, increasing the overall doping in the channel region. TCAD simulations confirm the influence of the bulk doping concentration on the TID response. Higher doping concentrations in the bulk increase the TID tolerance of the transistors. By combining the experimental measurements with simulations, we confirm that the channel-length dependence is associated with the halo implantations, which fortuitously increase the radiation tolerance of modern CMOS devices.

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