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Design of 28 nm CMOS front-end channels for pixel detectors in future high energy physics colliders and advanced X-ray imaging instrumentation

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Abstract

The development of integrated front-end circuits for hybrid pixel detectors represents a crucial challenge for advanced instrumentation in high energy physics and X-ray imaging. Future high-luminosity experiments and advanced imaging applications in Free Electron Lasers impose stringent requirements in terms of integration density, acquisition speed, high event rate handling, low temporal occupancy, radiation hardness, high dynamic range, and low noise. Despite the promising robustness and performance of 28 nm CMOS technology at the single device level, its practical application in complete front-end circuits for hybrid pixel detectors remains scarcely explored. This thesis aims to investigate the potential and limitations of 28 nm CMOS technology for the design and implementation of integrated readout channels in these scenarios. The work involved the design, simulation, layout implementation, and tapeout of three distinct front-end channels. The original contribution of this research lies in translating the theoretical evaluation of 28 nm CMOS technology into concrete implementations, realizing three prototype integrated circuits for hybrid pixel detectors, each with specific application objectives. A zero dead-time front-end with in-pixel 2 bit flash analog-to-digital converter, designed for ultra-high luminosity experiments. It demonstrated the ability to successfully process consecutive signals in adjacent bunch crossing periods. Simulations revealed a threshold dispersion below 30 e^- r.m.s. and a measured equivalent noise charge of about 63 e^- r.m.s., comparable to state-of-the-art chips such as those from the RD53 collaboration. The power consumption per pixel is only 5.4 µW. A second architecture based on the Time-over-Threshold technique for high energy physics applications, intended for accurate energy measurements and operation in high-radiation environments. Simulations showed noise levels not exceeding 50 e^- r.m.s. at −20 °C (for a detector capacitance of 50 fF) and a time-walk below 25 ns for an overdrive of 50 e^-. The uncalibrated threshold dispersion of about 200 e^- r.m.s. was reduced to 16 e^- r.m.s. after in-pixel calibration. The integral non-linearity of the Time-over-Threshold response was close to 2 % for an input charge range up to 15 000 e^-. The chip was fabricated and characterization is planned for late 2025/early 2026. A third Time-over-Threshold prototype with bilinear dynamic range dedicated to X-ray imaging, featuring an automatic gain switching mechanism has been developed. This allows operation in high-gain mode for weak signals (1 −100 photons) and low-gain mode for strong signals (100 −4000 photons), extending the dynamic range while maintaining low noise and fast response. Post-layout simulations confirmed a good integral non-linearity of 1.7 % in high gain and 1.4 % in low gain. The Time-over-Threshold counting system uses a 1 GHz ring oscillator within an 8-bit counter, ensuring a time resolution of 1 ns. The prototype was submitted for fabrication in July 2025. Overall, the results obtained in this work demonstrate the suitability of 28 nm CMOS technology for the next generation of pixel detectors in both high energy physics and X-ray imaging contexts, laying a solid foundation for future advances in experimental physics.

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Introduction

Front-end electronics for hybrid pixel detectors play a crucial role in advanced scientific instrumentation. These systems are essential in both High Energy Physics (HEP) and X-ray imaging. The challenges posed by future high-luminosity experiments, such as the upgrade of the CMS detector at the High Luminosity Large Hadron Collider (HL-LHC) or proposals for the Future Circular Collider (FCC-hh) experiments, require increasingly stringent specifications in terms of noise occupancy, granularity, bandwidth, power consumption, and radiation tolerance. Similarly, in imaging contexts such as detectors for Free Electron Lasers (FEL), the demand for temporal resolution, extended dynamic range, and compact circuit design makes electronic design ever more complex. While current research has demonstrated that individual transistors and basic building blocks in this technology can achieve good performance and radiation tolerance [1], [2], [3], there is still a lack of practical experience and published results regarding the integration of complete, fully functional front-end circuits for hybrid pixel detectors in 28 nm CMOS [4]. In particular, the challenges of combining dense analog and digital circuitry, ensuring reliable operation in harsh radiation environments, and meeting the stringent requirements of experimental physics applications remain largely unexplored in the literature.

In particular, there is a lack of systematic studies on how these circuits perform in real-world conditions, where they must handle both analog and digital signals and withstand radiation effects. Previous CMOS technology nodes, such as 130 nm and 65 nm, have been extensively used and validated in major projects like RD53 [5] and Medipix/Timepix [6]. However, these consolidated technologies are now facing significant challenges in meeting the increasingly demanding requirements for low power, high temporal resolution, in-pixel digitization, and compact circuit design.

The 28 nm CMOS node, which is already well-established in the industrial sector, offers the potential to enable a new generation of high-performance front-end electronics for physics applications. To realize this potential, it is essential to critically evaluate its design considerations, suitability for specific applications, and the practical testability of circuits built with this technology.

To address these challenges, three different front-end channels were designed, each with a specific architecture and application focus. The process began with the design and simulation of the circuits. Their electrical, functional, and post-layout performance were evaluated. Next, the layouts were physically realized and submitted for fabrication (tapeout). Dedicated test PCBs were created for each prototype. In parallel, software and firmware were developed to enable data acquisition from the prototypes. Where possible, the circuits underwent experimental characterization. The resulting data were analyzed to assess their performance. The outcomes of this research were then formalized in scientific articles and technical reports.

This thesis aims to fill the current gap on the real applicability of the 28 nm CMOS node in HEP and advanced X-ray imaging. Through the design and experimental charac-

terization of three integrated prototypes, it demonstrates that this technology can enable the design of high-performance front-ends compatible with future requirements of experimental physics.

The original contribution of this thesis lies in having brought 28 nm CMOS technology from theoretical evaluation to concrete implementation in three integrated circuits for hybrid pixel detectors, each with different application objectives. In particular, a zero-deadtime front-end with an in-pixel 2-bit flash ADC was designed and characterized. This circuit is intended for very high luminosity experiments and was developed within the FALAPHEL project, funded by Istituto Nazionale di Fisica Nucleare (INFN). The second front-end, based on the Time-over-Threshold principle, was developed by combining a compact architecture with indirect charge estimation, again targeting high-energy physics and designed within the framework of FALAPHEL and PiHex (PRIN 2022), and its tapeout and test board design have been completed. Finally, a third channel with bilinear dynamics was designed, intended for photon detection in FEL sources, designed entirely within the PiHex project. It was recently submitted to the foundry and its delivery is expected at the beginning of 2026. These circuits represent a first concrete step in evaluating the real applicability of the 28 nm CMOS node in extreme experimental contexts. They provide valuable indications both at the design and system testability levels.

The thesis introduces in Chapter 1 the scientific context and motivations that guided the research, outlining the current challenges in high-energy physics and advanced x-ray imaging, including a description of the role of particle accelerators and how the particles produced in collisions can be detected by detectors placed at the interaction points. This is followed by an overview of silicon detectors, focusing on pixel detectors, highlighting their main features, design requirements, and state-of-the-art architecture. Chapter 2 provides a summary of 28 nm CMOS technologies, focusing on their physical, electrical, and radiation hardness characteristics, and how these can be exploited for applications in high-energy physics and advanced imaging. Chapters 3 and 4 present the three designed front-end channels, specifying their architectural and application approaches. In particular, Chapter 3 discusses the zero-deadtime channel with 2-bit flash ADC, while Chapter 4 covers both the Time-over-Threshold channel for HEP applications and the bilinear dynamics channel for X-ray imaging.

The results obtained, partly already consolidated, partly under development, lay a solid foundation for a future generation of pixel detectors based on nanoscale technologies, and pave the way for further investigations and developments in the PiHex, FALAPHEL projects and other international contexts. In addition to presenting and discussing the work carried out during the PhD, this document is also intended to serve as a reference for future operational activities on the developed chips. In particular, it aims to provide guidance for the forthcoming characterization of the Time-over-Threshold front-end for FEL applications, which is planned to take place following the delivery of the fabricated prototypes (expected in early 2026), as well as for the design and implementation of the acquisition system—including PCB, software, and data analysis. The thesis is therefore conceived not only as a report of the research conducted, but also as a practical resource to support and streamline the next phases of experimental validation and system integration.

To understand the necessity of this thesis, it is first necessary to outline the scientific context in which the work is set. The scientific context of particle physics and photon science, which forms the basis for the work presented in this thesis, is introduced in the following.

Chapter 1

Technologies for pixel detectors

1.1 Scientific Motivation

The field of particle physics aims to answer fundamental questions about the nature of matter, the fundamental particles and forces, and the phenomena underlying the universe. The Standard Model [7] describes three of the four known fundamental forces and classifies all known elementary particles, but does not include gravity or explain dark matter and dark energy, which together constitute about 95% of the Universe [8], [9]. General Relativity [10] describes gravity as the curvature of spacetime, but is not yet unified with the Standard Model. The search for a unified theory remains a central goal of modern physics.

According to the Standard Model, matter is composed of fermions (quarks and leptons) and their interactions are mediated by bosons (photon, gluon, W and Z bosons). Each particle has properties such as mass, electric charge, and spin. Mass arises from interaction with the Higgs field [11], and electric charge determines electromagnetic interactions. Quarks and leptons are considered elementary, with quarks combining to form hadrons (such as protons and neutrons) due to the strong force, described by quantum chromodynamics (QCD). Quarks are confined within hadrons and cannot exist freely, a property known as confinement [12]. Hadrons are color-neutral combinations of quarks, and their electric charge results from the sum of the charges of their constituent quarks.

Particle Physics is therefore concerned with studying subatomic particles, which are the building blocks of matter and fundamental forces. These particles are subject to the laws of quantum mechanics and relativity. The subatomic world is made up of fermions (quarks and leptons) that interact via the exchange of bosons. It is possible to study particles through their interactions and secondary effects, which are detected and analyzed using advanced experimental techniques and detector systems.

1.1.1 Particle accelerators and colliders

From a practical point of view, studying subatomic particles requires instruments capable of imparting high energy to the particles, bringing them to speeds close to that of light. Particle accelerators are devices that use electric and magnetic fields to accelerate charged and stable particles, which can be leptons or hadrons, guiding them along a controlled trajectory. The main types of accelerators are circular (synchrotrons, cyclotrons, storage rings) and linear (linacs). Neutral particles can be accelerated with other methods [14]. Accelerators are distinguished both by their structure and by the type of particles they

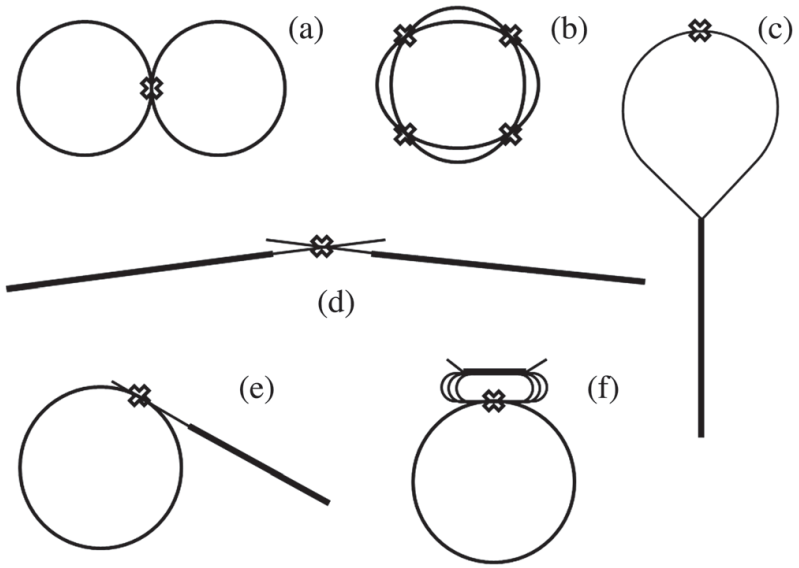


Figure 1.1: Schematics of particle collider types. In storage-ring configurations (a) and (b), particles of each beam circulate and repeatedly collide. In linear colliders, the two colliding beams are accelerated in linacs and transported to a collision point, either with use of the same linac and two arcs (c) or in the simple two-linac configuration (d). Other configurations are possible, such as the linac-ring scheme (e) or a collision of beams circulating in a ring and a few-pass Energy Recovery Linac (f) [13]. It is important to note that the typical size of particle accelerators can reach kilometers in length and tens of kilometers in circumference.

accelerate.

It is not enough to accelerate the particles; it is also necessary to make them interact with each other. A specific category of accelerators includes colliders, which accelerate two beams of particles in opposite directions and make them collide. Some examples of typical structures are shown in Figure 1.1.

Based on the nature of the accelerated particles, colliders can be divided into two categories: hadron colliders and lepton colliders. The peculiarity of these machines, in addition to the type of accelerated particles, depends on some physical parameters that are chosen as design requirements: the center-of-mass energy, the energy reachable by the machine, the luminosity, and the type of collisions to be studied. [12], [13], [15], [16] discuss in detail the physical parameters that characterize colliders. The following paragraphs briefly summarize the main definitions of these parameters, as discussed in the referenced sources.

Particle collisions are rare events, so it is necessary to find a way to increase their probability. To do this, identical particles are grouped into bunches, and care is taken to ensure that they cross at specific points in the accelerator, called interaction points. At these points, colliding two high-speed particle beams against each other (colliding-beam setup) offers a kinematic advantage, as the total energy of the system is double that of a single particle beam hitting a stationary target (fixed-target setup) [13]. The total energy of the system is important because it determines the mass of the particles that can be produced during the interaction [17]. This quantity is called center-of-mass energy,

$\sqrt{s}$, and it is defined as the total energy available in the center-of-mass reference frame, where the total momentum is zero. In particle physics, energy is usually expressed in electronvolts (eV) and its multiples (MeV, GeV, TeV), units more suitable for the order of magnitude of the phenomena under consideration. Since this quantity is calculated from the vector in Minkowski spacetime [18], it has a norm invariant under Lorentz transformations, which are the transformations that connect reference frames in relativistic motion. Consequently, $\sqrt{s}$, with $s = (E_{tot})^2 - (\vec{p}_{tot})^2$, where E_{tot} and $\vec{p}_{tot}$ are respectively the total energy and the resulting momentum vector of the system, is invariant with respect to the chosen reference frame. Colliders are designed to operate at specific center-of-mass energies to achieve certain scientific goals.

The parameter of energy reachable by the machine refers to the energy of individual particles within the beam. Although directly related to the center-of-mass energy, it describes the intrinsic capability of the acceleration system. In linear colliders, the beam energy is determined by the gradient of the accelerating electric field G and the length of the linac L. The energy gained by a single charged particle can be approximated by $E_{beam} = eGL$, where e represents the elementary charge of the electron. In this type of accelerator, particles travel a straight path only once and therefore receive all the energy in a single acceleration. In circular colliders, particles gain energy gradually as they complete multiple revolutions around the ring. This is achieved using radiofrequency (RF) cavities [13], which accelerate the particles by applying an electric field at precise intervals. At each pass through an RF cavity, a particle receives an energy increment of approximately $\Delta E \simeq eV_{rf}$, where e is the elementary charge and V_{rf} is the voltage applied by the RF cavity. Through many passes, the particles are accelerated to the desired energy. Magnets bend the particles, keeping them on a circular trajectory. The relationship between the average magnetic field B and the bending radius ρ allows us to determine the momentum of the beam, according to the relation $p = eB\rho$. If the particle is ultrarelativistic, meaning its kinetic energy is much greater than its rest energy ($E_{kin} \gg E_{rest} = mc^2$), and is moving at speeds close to the speed of light, its total energy can be approximated as $E_{tot} \approx pc$. Combining the two relations, it is possible to obtain the beam energy as a function of the bending radius and the average magnetic field: $E_{beam} \approx eB\rho c$. The bigger the radius, the higher the energy that can be reached.

The luminosity is a parameter that describes the rate of events that can be observed in a given time interval at the interaction point of an accelerator. The expected number of events (collisions) observable N for a certain physical process is proportional to the integrated luminosity $\mathcal{L}_{int}$ and the cross-section σ of the physical process under consideration, i.e. $N = \sigma \cdot \mathcal{L}_{int}$, where $\mathcal{L}_{int} = \int \mathcal{L}(t)dt$. The instantaneous luminosity $\mathcal{L}(t)$ represents the number of collisions per unit area as a function of time, and is expressed in units of $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. In colliders with structured bunches, the instantaneous luminosity can be expressed as [13]:

$$\mathcal{L}(t) = f_{coll} \cdot \frac{N_1(t)N_2(t)}{4\pi\sigma_x^*(t)\sigma_y^*(t)}, \tag{1.1}$$

where f_{coll} is the collision frequency, N_1 and N_2 are the number of particles in the two beams, and σ_x^* and σ_y^* are the root mean squared dimensions of the beam at the point of interaction in the horizontal and vertical directions, respectively. The cross-section σ is a measure of the transverse area that a target presents to an incoming particle flux, and is expressed in units of area (barn, or cm^2).

Luminosity is directly proportional to the collision frequency and the number of par-

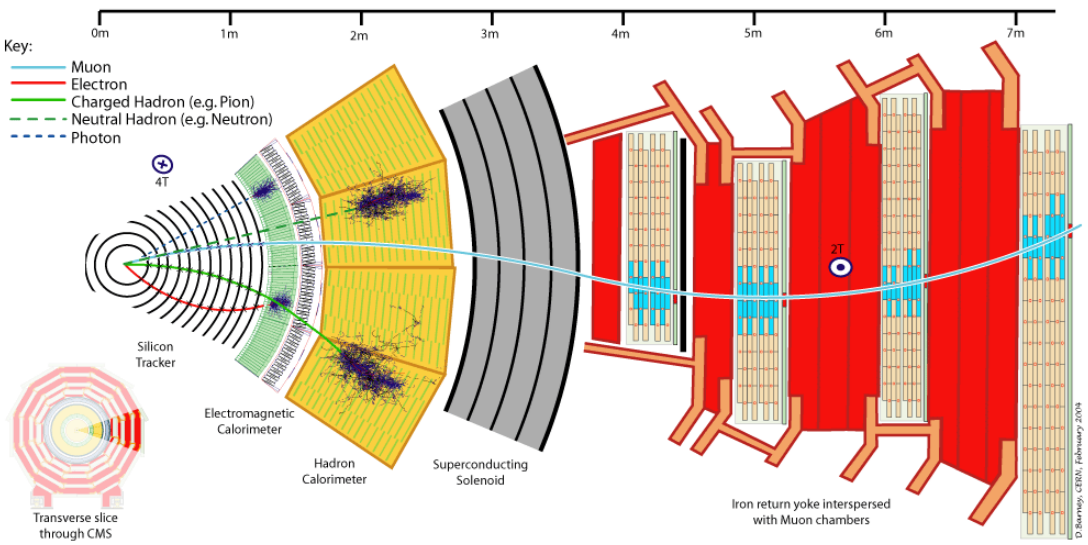


Figure 1.2: Cross-sectional view of the CMS detector [19] at the Large Hadron Collider at CERN . The detector is composed of several concentric layers, each designed to detect specific types of particles and measure certain properties. The layers include muon chambers, calorimeters, and trackers, which work together to reconstruct the properties of subatomic particles produced during collisions. The size of the detector is about 21 meters in diameter and 15 meters in height, and it weighs about 14,000 tons. The detector is designed to operate in a strong magnetic field, which allows for the measurement of the momentum of charged particles. The CMS detector is one of the largest and most complex particle detectors ever built, and it has played a crucial role in the discovery of the Higgs boson in 2012 [20].

ticles in the beams, and inversely proportional to the beam size at the interaction point. The collision frequency depends on the number of bunches and the revolution frequency of the beams within the accelerator. Increasing the number of bunches is a well-established method to increase luminosity [13]. To achieve high luminosity, it is also possible to increase the number of particles per bunch, or reduce the beam size at the interaction point, or compress the beams at the interaction point. The type of collisions studied determines the physics domain and the design of the collider. Lepton colliders, using point-like particles, allow for precise measurements and clean signals, but require large or linear accelerators due to energy loss from synchrotron radiation. Hadron colliders, accelerating composite particles like protons, reach higher energies and luminosities, enabling the study of rare processes, but have more complex collision dynamics due to parton interactions. Hybrid colliders, colliding leptons with hadrons, offer detailed studies of hadron structure, though with additional technical challenges and typically lower luminosity.

1.1.2 Detection Systems

The different types of colliders are designed to study specific physical phenomena and to answer questions about the nature of matter and fundamental forces. They all share

the common feature of accelerating particles to speeds close to the speed of light and colliding them at interaction points. In these zones, subatomic particles interact with each other and produce other subatomic particles, which can be studied to understand the fundamental laws of physics. It is therefore necessary to have detection systems, also called experiments, whose purpose is to observe, record, and then study the dynamics of the interaction, in order to reconstruct the properties of the subatomic particles produced during the collisions. These detectors are generally designed with a concentric layered structure around the pipe that accelerates the bunches of particles. Each layer, or subsystem, is optimized to detect specific types of particles or measure certain properties. There exists experiments with more specific configurations, aiming to study specific phenomena, such as neutrino detectors or dark matter detectors, or other more general purpose detectors, aiming to study a wide range of phenomena. One of the most famous examples of the latter is the CMS detector at the Large Hadron Collider at CERN [19], whose cross-section is reported in Figure 1.2. Detectors are generally classified into three main categories: muon chambers, calorimeters, and trackers.

Muon chambers Muon chambers are the outermost detectors in the detection system and are designed to detect muons, which are charged particles similar to electrons but with a mass about 200 times greater. Due to their massive nature, muons can travel through and penetrate large thicknesses of material without undergoing significant interactions. Muons can therefore be detected even at large distances from the interaction point, and for this reason, muon chambers are positioned in the outermost layers of the detector. Muons are charged particles and therefore interact with electric and magnetic fields, but their high mass makes them less susceptible to such interactions compared to other charged particles. Muons can be detected through the emission of bremsstrahlung radiation when they pass through dense materials, such as lead or copper. This radiation produces photons that can be detected by light-sensitive devices, such as photomultipliers or solid-state detectors. Muon chambers are designed to detect muons by measuring their position and trajectory, typically using technologies such as drift chambers or scintillation detectors. These systems exploit the ability of muons to penetrate dense materials, providing essential information for event reconstruction in particle physics experiments.

Calorimeters Calorimeters are systems of devices located in the outermost layers of the detector and are designed to measure the energy of charged and neutral particles. Electromagnetic calorimeters, ECAL, are designed to absorb and measure the energy of photons and electrons. ECALs also exploit the principle of bremsstrahlung, as well as the pair production principle, which is the process of creating a pair of charged particles (an electron and a positron) from a photon when it interacts with a strong electric field. These processes lead to the production of a cascade of secondary particles, which deposit energy in the material of the calorimeter, until a depth sufficient to completely stop the incident particle is reached. The sum of the energy deposited throughout the material of the calorimeter provides a measure of the energy of the incident particle. Hadronic calorimeters, HCAL, are designed to measure the energy of charged and neutral hadrons. HCALs interact with particles through elastic and inelastic scattering processes, which lead to the production of secondary particles. Again, the sum of the energy deposited throughout the material of the calorimeter provides a measure of the energy of the incident particle. HCALs are designed to be thicker than ECALs, as they need to stop heavier and faster particles that penetrate more deeply into the material before being completely

absorbed. Calorimeters can be built as homogeneous devices (using continuous active material) or as sampling devices (alternating absorber and sensor layers), depending on the required energy resolution and engineering constraints. They are essential for measuring particle energy and aiding in particle identification.

Trackers Trackers are the innermost detectors of the detection system and are designed to provide the measurements necessary for a precise reconstruction of the trajectories of charged particles. The curvature of the reconstructed trajectories, along with the possible presence of external magnetic fields, allows for the determination of the momentum of the particles and thus their mass, enabling their identification. These detectors are crucial for identifying the production points of particles (vertices), distinguishing the primary vertex of the collision from the secondary vertices created by the decay of long-lived particles [16]. Timing detectors can be seen as an extension of tracking systems. They introduce the measurement of the arrival time of charged particles in the detector with high resolutions, on the order of tens of picoseconds. Timing detectors are integrated between the layers of traditional trackers or directly downstream of the tracker.

These devices allow for the reconstruction of collision vertices both in space and in time, helping to address the phenomenon of pile-up, which occurs when multiple collisions happen within a very short time interval. Pile-up events can complicate data analysis, making it difficult to distinguish between particles produced in different collisions. This phenomenon is particularly relevant in hadronic colliders, where the luminosity is very high and multiple collisions are common. As luminosity increases, the probability of pile-up events rises, making data analysis increasingly challenging. Timing detectors thus enable the distinction of events that would otherwise be overlapping within spatial regions of a few millimeters and with time scales on the order of tenths of nanoseconds.

1.1.3 Silicon Trackers

The properties of silicon as a semiconductor, particularly its ability to generate electrical signals when traversed by charged particles, are fundamental to the operation of these detectors and represent the key enabling technology for their functionality. There are pixel and strip detectors, and they are constructed to realize particular pn-junction diodes biased with a strong reverse voltage, creating a deep depletion zone along with an electric field throughout the depletion zone. When a charged particle traverses the volume depleted of charge carriers, it deposits energy and creates a number of electron-hole pairs proportional to the energy released in the material along its trajectory. Under the effect of the electric field due to the polarization, these charge carriers move by drift towards the electrodes of the sensor, where they induce an electrical signal. The main difference between the two types of detectors used in silicon trackers lies in their geometry and granularity. Pixel detectors are typically made up of square silicon cells, each of which acts as a single sensitive element. The typical size of a pixel is on the order of tens of micrometers, and their arrangement allows for high spatial resolution. Strip detectors, on the other hand, consist of long, thin strips of silicon. The typical width of a strip is comparable to that of a pixel, but the length is on the order of centimeters.

Pixel modules are designed to be highly integrated and compact, in order to maximize detection density and minimize the volume of the detector, especially in the innermost regions where track density is highest. They are indeed grouped into pixel matrices, which can be grouped into module arrays, forming a mosaic of modules. Each module,

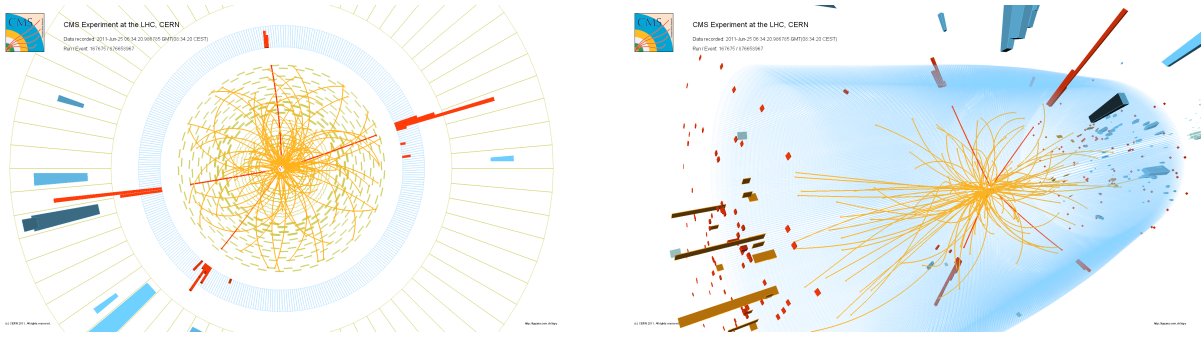


Figure 1.3: Event display from the CMS experiment at the LHC showing a real CMS proton-proton collision event in which 4 high energy electrons are observed. The red towers in the display represent the energy deposits of these electrons in the calorimeter. The event shows characteristics expected from the decay of a Higgs boson but is also consistent with background Standard Model physics processes.[21].

whether strip or pixel, along with its readout circuits, is assembled into a concentric layered detection system around the interaction point. By combining pixel modules for areas where high granularity and spatial precision are required, in the regions closest to the interaction point, with strip modules for the outer regions, where lower spatial resolution is needed, a layered detection system is obtained that allows for high-precision measurements of the vertices and trajectories of charged particles.

Silicon detectors generate an electrical signal in response to interactions with charged particles, and this signal is amplified and digitized for subsequent analysis. This operation of reading, amplifying, shaping, and digitizing the signal is fundamental. Each pixel or strip is therefore equipped with a readout circuit, designed as Application Specific Integrated Circuits (ASICs). The characteristics of the readout circuits depend on the specific technology chosen to implement them and the type of detector that needs to be read. In general, the detector system with its readout circuit is designed to meet specific requirements in terms of spatial resolution, readout speed, pile-up handling capability, and radiation hardness that depend on the operational characteristics of the collider and the scientific needs of the experiment. The design and realization of tracking detectors is therefore a complex task, requiring a deep understanding of particle physics, semiconductor technology, and electronic engineering techniques.

The general detector system presented until now is designed to operate in the context of high energy physics, where the need to detect particles with high spatial and temporal resolution is crucial. All of the subsystems described above are designed to work together to provide a complete picture of the events occurring at the interaction point. In Figure 1.3, it is possible to see an example of a collision event observed at the Large Hadron Collider (LHC) at CERN, specifically in the CMS experiment. This is one of the final outputs of the detection system, the starting point for the analysis of the events produced by the collisions, where physicists can study the properties of the particles produced and search for new phenomena, such as the Higgs boson.

1.2 Principles and types of silicon pixel detectors

Tracking systems in high-energy physics experiments require materials that allow for the efficient detection of charged particles while minimizing unwanted interactions such as

scattering and energy loss. Silicon is an ideal material for these applications, as it has several favorable physical and electronic properties. As reported in [22], in a crystal of semiconductor material, the energy states of the atoms are quantized and form energy bands. This quantization is crucial for detector operation, as the separation between energy bands (the band gap) determines the energy required to generate electron-hole pairs, which are the fundamental charge carriers collected by silicon detectors. These energy levels, determined by the interactions between the atoms in the crystal and the position of the electrons in the atomic orbitals, are characteristic of the material. It is possible to distinguish between conduction bands and valence bands. The conduction band is the energy band in which electrons are free to move throughout the crystal lattice, enabling electrical conduction, while the valence band is the energy band in which electrons are bound to their respective atoms and are not mobile. There is a separation between these bands, which is determined by the crystal structure of the material and the interactions between the atoms, as well as the chemical properties of the material itself, and is known as the energy band gap. This represents the minimum energy, known as the band gap energy, required to excite an electron from the valence band to the conduction band. The band gap can be overcome by providing thermal energy (which increases atomic vibrations and can excite electrons), applying an electric voltage (which creates an electric field that accelerates electrons), or exposing the material to electromagnetic radiation (such as photons with energy greater than the band gap, which can directly excite electrons across the gap). Temperature affects both the generation and mobility of electrons and holes: as temperature increases, more charge carriers are thermally generated, but the increased thermal energy also leads to stronger lattice vibrations, which hinder carrier mobility and reduce their drift velocity.

At room temperature, intrinsic silicon has an energy band gap of about 1.12 eV [22]. The mobility of electrons and holes determines the conductivity of the semiconductor. For electrons, the mobility μ_n is generally greater than that of holes μ_p, which means that electrons move more quickly through the material than holes. This aspect leads to a faster collection for electrons compared to holes, affecting the response time of a detector. As a result, the timing resolution of the detector is improved, and the signal shape is sharper and faster when dominated by electron collection, which is advantageous for precise particle tracking and minimizing signal overlap.

When a photon or other ionizing particle passes through silicon, it can interact with the atoms of the crystal lattice, transferring part of its energy to the electrons. A sufficiently energetic particle incident on silicon can deposit enough energy to generate an electron-hole pair, promoting an electron from the valence band to the conduction band. The average energy required to create an electron-hole pair in silicon is about 3.6 eV [23], [24], [25]. It is important to emphasize that this value represents the average energy lost by the incident particle to produce a single pair, and does not exactly coincide with the amplitude of the band gap. The difference between these two energies is due to the fact that only a fraction of the deposited energy directly contributes to electron-hole pair creation; the remainder is dissipated through other mechanisms, such as lattice vibrations (phonons), multiple excitations, and heat production [26].

In the absence of an electric field, the movement of charge carriers (electrons and holes) in silicon is governed by the process of *diffusion*. This motion, due to thermal agitation, can be qualitatively compared to Brownian motion [27], even if in semiconductors it is described more rigorously through continuity equations and the Einstein model: $D = \mu \frac{kT}{q}$, where D is the diffusion coefficient, μ the carrier mobility, k the Boltzmann constant, T

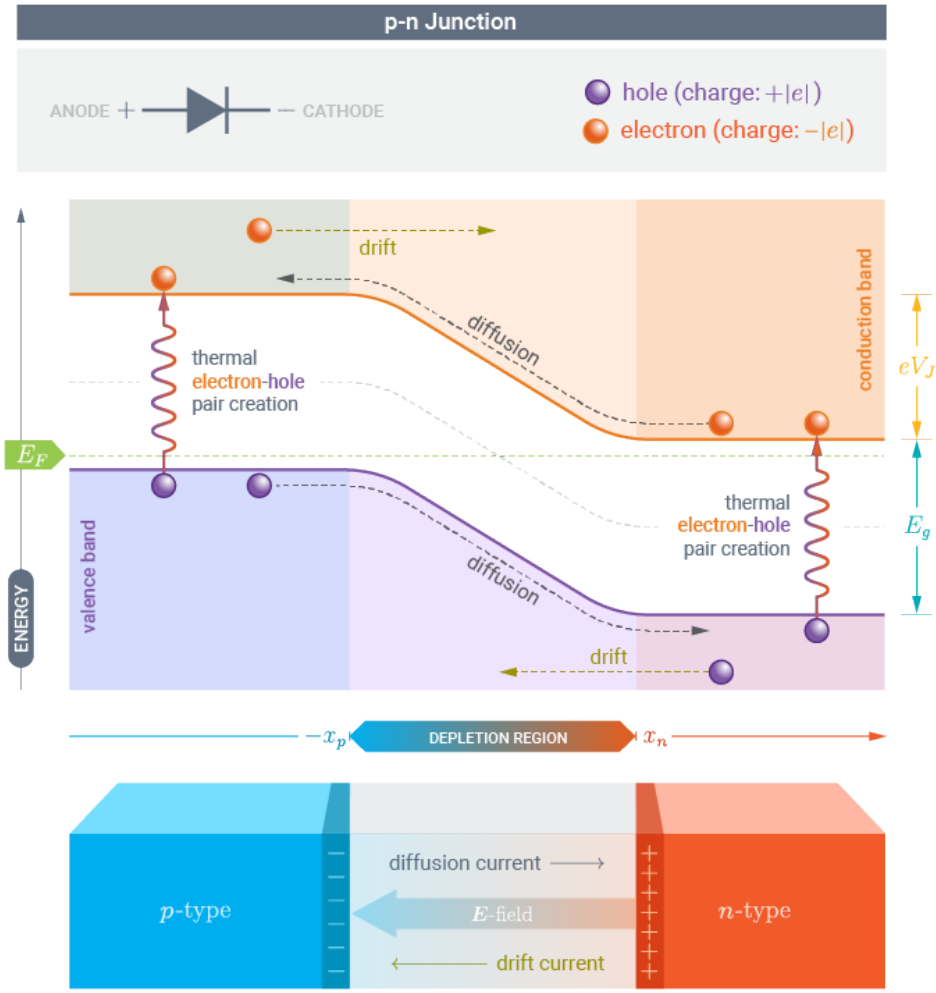


Figure 1.4: Schematic representation of a p-n junction in silicon. The depletion region is shown, where the electric field is generated by the fixed ions left behind after the diffusion of majority carriers. The arrows indicate the direction of the electric field and the movement of electrons and holes under the influence of this field [28].

the temperature, and q the elementary charge [22]. The diffusion mechanism becomes predominant in regions of the device where no electric field is present.

As a matter of fact, silicon pixel sensors are implemented by means of custom engineered p-n junctions. A p-n junction is formed by joining two regions of silicon doped respectively with p-type and n-type impurities. At the junction, the majority carriers (electrons in the n-region and holes in the p-region) diffuse into the opposite region as a result of the concentration gradient between the two regions. This diffusion leads to the recombination of free carriers and leaves behind, in the crystal lattice, the uncompensated dopant ions: negatively ionized acceptor atoms in the p-region and positively ionized donor atoms in the n-region. These fixed ions, being bound to the lattice, generate an internal electric field oriented from the n-region to the p-region (see Figure 1.4 for a schematic representation). The field thus generated opposes further diffusion of the majority carriers, bringing the system to a state of equilibrium where diffusion and drift balance each other. The area affected by this phenomenon is called the depletion region, as in it the free carriers are removed, leaving only the fixed ions. The width of

this region can be modulated by applying a voltage across the junction: specifically, applying a reverse bias (positive voltage to the n-side and negative to the p-side) increases the depletion width by driving majority carriers away from the junction and expanding the region depleted of free carriers. Its width depends on the concentration of dopants and the sum of the applied voltage and the built-in voltage [22]. In a silicon detector, a reverse bias is typically applied to completely deplete the active region (full depletion condition), generating an internal electric field strong enough to cover the entire sensitive area. The full depletion condition is often a design requirement to ensure efficient charge collection, especially as device sizes decrease. The strong electric field quickly separates the generated charges: by drift, electrons move towards the cathode, holes towards the anode, thereby significantly reducing the probability of recombination before collection. The induced current on the electrodes is proportional to the total number of generated e-h pairs, which in turn is proportional to the energy deposited by the particle.

As already mentioned, the width of the depletion region, or the active sensitive volume, depends on the applied reverse bias voltage and the doping concentration. Increasing the reverse bias voltage causes the depletion region to widen, allowing the electric field to penetrate deeper into the material and extend the active volume in which the electron-hole pairs generated by an ionizing particle can be collected.

In particular, the depletion width, W, increases with decreasing doping concentration, N, of the lightly doped side of the junction, following an inverse square root relationship:

$$W \propto \frac{1}{\sqrt{N}} \tag{1.2}$$

This behavior is fundamental for the design of silicon detectors. By using high-resistivity silicon (i.e., low doping), it is possible to fabricate detectors with a thick sensitive volume that can be fully depleted at relatively low bias voltages. Full depletion ensures a uniform electric field across the entire active region, enabling efficient and rapid charge collection, minimizing recombination losses, and improving both the timing and energy resolution of the detector.

The properties seen so far are the starting point for the design of silicon detectors. They require segmenting their sensitive area in order to obtain precise information about the position of the incident particle. This segmentation divides the surface of the sensor into smaller units, which can be strips or pixels. The achievable spatial resolution is determined by the pitch of the sensors. The historical starting point in the use of segmented semiconductors for particle tracking is silicon strips [29]. In this configuration, the pn junctions are implanted on the silicon wafer in the form of strips, providing a one-dimensional readout of the particle position [25]. One of the limitations of these sensors, especially in high particle density environments, is the potential ambiguity in the three-dimensional track reconstruction. This problem is addressed by combining multiple measurements in different directions on different planes.

An alternative is to modify the sensor geometry and switch to pixel sensors, offering a direct two-dimensional readout of the particle position. A pixel sensor is essentially an array of very small diodes, allowing for rapid localization. Pixels can be fabricated using either monolithic or hybrid architectures.

1.2.1 Monolithic Pixels

As shown in Figure 1.5b, in Monolithic Active Pixel Sensors (MAPS), the sensitive element and the readout electronics are integrated on the same silicon chip. These devices leverage

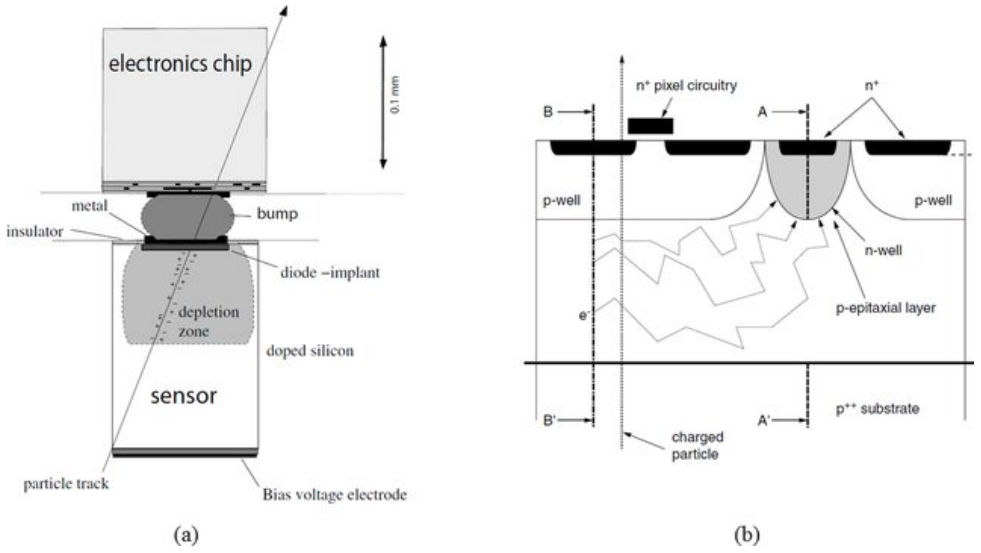


Figure 1.5: Graphical representation of the differences between monolithic and hybrid pixel sensors. In the monolithic architecture (b), the sensitive element and the readout electronics are integrated on the same silicon chip, while in the hybrid architecture, they are realized on different substrates and connected through bump bonding (a). Images adapted from [30].

standard CMOS processes, allowing for a high degree of integration. Initially, in MAPS, the collection of charge generated by the interaction of the particle occurred by diffusion in a thin epitaxial layer [31]. MAPS can be fabricated with thinner layers, reducing the amount of material that particles must traverse, as well as allowing for a smaller pitch, thus higher granularity. However, the low resistivity of the substrate in standard CMOS processes (about $10\,\Omega \cdot \mathrm{cm}$) limited the extent of the depletion layer [32]. Even with epitaxial layers or high voltage, the depletion is often limited to a few micrometers, leaving the rest of the silicon undepleted [32], [33]. The collection of charge by diffusion is slow, which limits the time resolution and makes the sensor more vulnerable to radiation damage [31], [34]. Furthermore, in standard CMOS processes, the well configuration can limit the complexity of the integrated electronics within the pixel [32].

To overcome these issues, Depleted MAPS (DMAPS) were introduced as an evolution of traditional MAPS. DMAPS utilize a high resistivity substrate [32], [35], which allows for a fully depleted detection volume by applying a dedicated bias voltage. The presence of an electric field promotes charge collection by drift, enabling faster signal formation with greater amplitude. Moreover, the introduction of structures such as deep p-wells has made it possible to integrate more complex CMOS electronics within the pixel, further improving system performance. DMAPS can use modified commercial CMOS processes, allowing for the integration of more complex electronics. The combination of these structural improvements leads to both enhanced radiation tolerance [32], [35] and a reduced equivalent capacitance of the sensor. The ALICE experiment at CERN in Geneva has planned to employ tracking systems based on monolithic pixels fabricated using a 65 nm CMOS technology for the upcoming upgrades of the detector, with operational readiness expected from early 2026 [36].

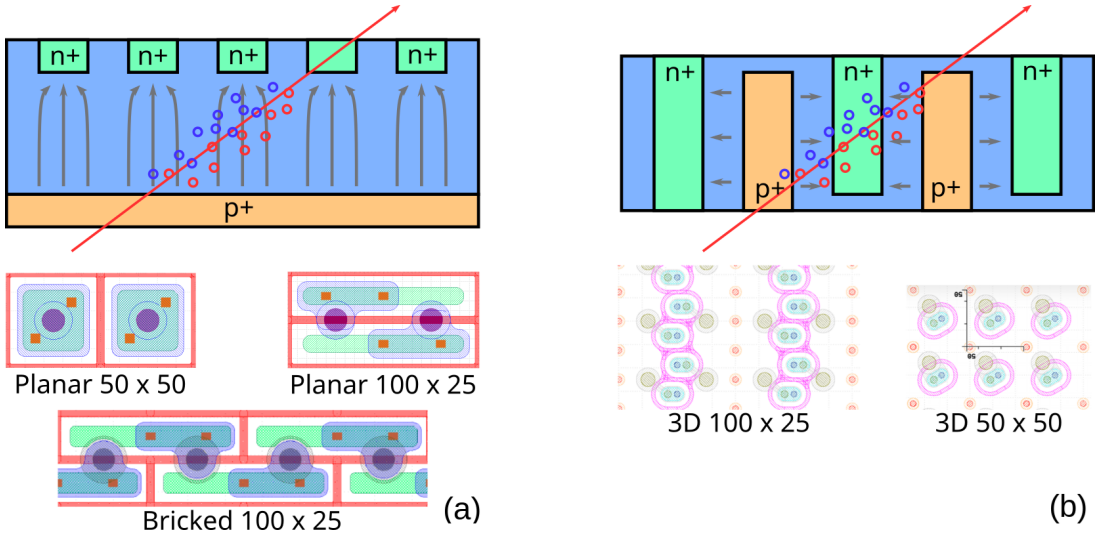


Figure 1.6: Top: side schematic of a planar (a) and one type of 3D (b) pixel sensor. Bottom: layout top view of some types of planar (a) and 3D (b) pixel configurations [39]. All dimensions are in μm.

1.2.2 Hybrid Pixels

In hybrid pixels, sensor and readout circuit are placed on different substrates. As one can see in Figure 1.5a, the sensor consists of a passive device, typically fabricated on high-resistivity silicon to allow for the application of high bias voltages and ensure efficient charge collection even after irradiation [37]. The readout ASIC contains the electronics for signal amplification, processing, and data acquisition. The two chips are typically bonded together using bump-bonding technology, creating an electrical connection for each individual pixel. The advantage of this approach is the ability to separately optimize the sensor and readout electronics according to specific requirements. Furthermore, it is also possible to design readout circuits suitable for different types of sensors. However, the connection via bump bonding is a complex and costly operation, which also imposes limitations on the minimum thickness for both components and the minimum achievable pixel pitch [38].

The sensors used with this type of architecture are referred to as passive. As such, they do not contain active electronics for signal amplification or processing within each sensitive element. They can be realized either through ad hoc production processes or through standard CMOS processes. The collection of charge generated by the passage of a particle depends crucially on the geometry of the electrodes implanted in the silicon. In Figure 1.6 are shown the two main geometries typically adopted in the design of hybrid pixels: planar and 3D, within some layout topologies reported as examples.

Planar In planar sensors, the electrodes are implanted parallel to the surfaces of the silicon wafer (Figure 1.6a). Typically, this consists of a thin segmented readout implantation (typically n+) on one surface of the wafer and a large area implantation on the opposite side (typically p+ for the bias). For sufficiently large readout electrodes, the electric field can be approximated as that of a single p-n junction oriented perpendicularly to the surface. They can be fabricated on n-type or p-type wafers. The bias voltage required to achieve full depletion depends on the thickness and resistivity of the material.

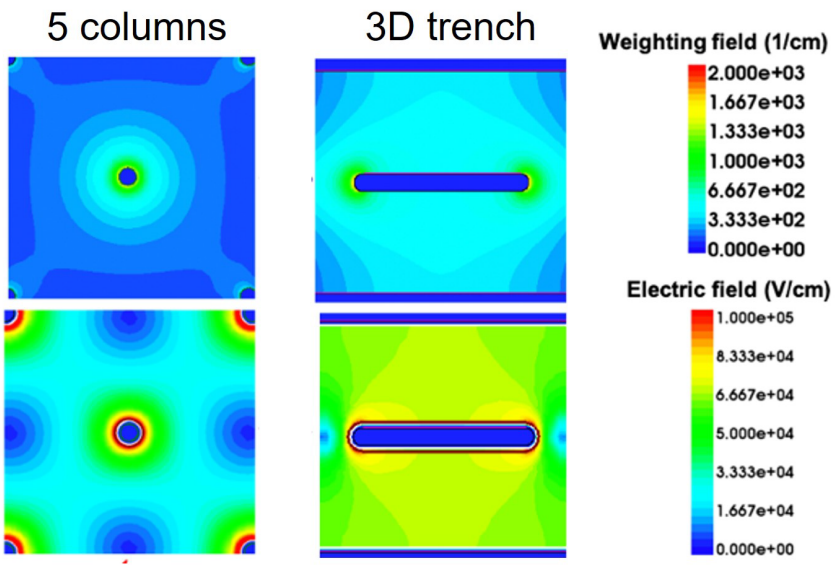


Figure 1.7: TCAD simulations of weighting field and electric field for a 3D detector with a 5 columns electrodes geometry (left) and for the TimeSPOT 3D-trench geometry (right) seen from the top of the sensor. Simulations have been done with a $V_{bias} = -150\,\mathrm{V}$ [41].

The manufacturing process is considered simple and well-established; however, there are some disadvantages to using these sensors. Since the electrodes are on the surfaces, the distance for charge collection is essentially the thickness of the detector, which can be critical in some applications. To deplete a planar sensor and ensure its efficiency, particularly after radiation damage that increases the effective space charge, high bias voltages are required, often up to 1500V [37]. In addition, irradiation creates defects in the silicon that act as trapping centers for charge carriers. In thicker sensors, charge carriers must travel greater distances to reach the electrodes, increasing the likelihood of being trapped [40]. This leads to a reduction in collected charge and detection efficiency, unless very high bias voltages are applied to accelerate drift [37]. Typical planar sensors have a thickness on the order of 100 µm to 200 µm.

3D 3D sensors represent an advanced architecture in which electrodes are not confined to surfaces, but consist of an array of implanted columns (or trenches) that penetrate perpendicularly deep into the sensor substrate (Figure 1.6b). These columns are realized with both p-type and n-type doping. Typical configurations include p+ columns serving as bias electrodes and n+ columns serving as readout electrodes. The p+ columns reach a low-resistivity substrate layer for bias contact, while the n+ columns can terminate just before this layer. The spacing between the columns can be optimized using p-spray or p-stop implantations for isolation. As one can see from Figure 1.7, specific layouts can vary, for example with a central n+ column and p+ columns at the corners of the pixel, or with columns arranged as parallel trenches. It is possible to have multiple readout columns per pixel. The crucial advantage of this architecture is that the distance between the electrodes is determined by the lithographic layout (the spacing between the columns) and not by the thickness of the sensor. This distance can be made significantly smaller than the thickness of the wafer.

For example, for the innermost layers of the ATLAS IBL, where the Insertable B-Layer (IBL) is the inner most pixel layer in the ATLAS experiment, which was installed at 3.3 cm radius from the beam axis, the distance between the electrodes was about 67 µm, with a sensor thickness of 230 µm. The reduced inter-electrode distance allows for complete depletion of the sensor using bias voltages significantly lower than those required for planar sensors of the same thickness [42], [43]. In particular, the depletion voltages for 3D sensors are roughly two orders of magnitude lower than for planar ones [43]. In ATLAS IBL, 3D sensors required 20 V of bias at the beginning of life and up to 180 V at the end of life, compared to 60 V/1000 V for planar sensors. This reduced bias voltage results in lower power consumption. The short distance that the charge carriers must travel to reach the electrodes translates into a much faster charge collection time compared to planar sensors. This is crucial for achieving excellent time resolution. The fast drift collection also minimizes the timing uncertainties due to carrier diffusion. The probability of a charge carrier being trapped by radiation-induced defects is reduced thanks to the short drift distance. 3D sensors demonstrated excellent radiation hardness, with high detection efficiency even after fluences, i.e. the number of equivalent neutrons passing through a surface per unit area, up to $3 \cdot 10^{16} neq/cm^2$ [40]. This feature makes them ideal candidates for the innermost regions of detectors.

However, the creation of electrodes that penetrate the bulk requires a more sophisticated and expensive manufacturing process compared to planar sensors. Furthermore, the electrodes themselves represent "dead" regions within the sensor that do not contribute to charge collection. Some electrode geometries, such as the "classic" column structure, may exhibit areas with very low or zero electric field, leading to geometric inefficiencies. These can be made negligible by tilting the sensor with respect to the particle beam, but they remain important for signal uniformity and time resolution [44]. Trench layouts or optimized geometries aim to improve field uniformity [42], [44], [45].

Regardless of the type of sensor, the reading of the signal generated by the collected charge is done through a dedicated circuit, which can be integrated into the sensor itself (as in MAPS) or external (as in hybrids). In silicon detectors, the sensor and the readout electronics form a tightly interconnected system. Overall performance largely depends on the interaction between the two subsystems. Front-end electronics, and in particular the input stage represented by the charge preamplifier, or Charge Sensitive Amplifier (CSA), plays a fundamental role in operating as an interface with the sensor. The intrinsic characteristics of the detector directly influence the design requirements and expected performance of the readout electronics. Parameters such as pixel geometry, doping profiles, sensor thickness, and biasing scheme determine key quantities such as the equivalent pixel capacitance, the amount of charge generated by the interaction with the incident radiation, and the leakage current. These properties impose stringent constraints on the design of the analog front-end, influencing critical aspects such as the signal-to-noise ratio, response time, and power consumption. For example, minimizing the input capacitance is an essential element for maximizing gain, reducing electronic noise, and improving amplifier speed. Furthermore, operation in hostile environments, such as those with high radiation levels, imposes severe radiation hardness requirements on both the sensor and the ASIC. Design choices related to the sensor, including electrode configuration and pixel isolation solutions, must therefore be compatible with the capabilities of the readout electronics and the resources available at the system level. The following section analyzes in detail the main physical and technological parameters of the sensor, including pixel capacitance, charge signal, leakage current, and biasing modes, and their

influence on design constraints and the performance of the front-end electronics in hybrid pixel detectors.

1.2.3 Signal Creation in Silicon Detectors

Understanding the characteristics of the signal generated by a silicon detector is fundamental for designing an adequate readout circuit. The interaction between the incident particle and the sensor material generate charge carriers that are collected by the electrodes and converted into a measurable electrical signal. The amount of charge, e-h pairs, generated depends on the energy deposited by the particle in the active volume of the sensor and the thickness of the volume itself. For relativistic particles, the energy loss is mainly due to effects of inelastic scattering on the outer shell electrons of silicon atoms, causing ionization and excitation of the lattice [37].

Sources indicate that a sensor with a thickness of 300 µm generates a charge on the order of 3.5 fC [29]. For a sensor with a thickness of 150 µm, the collected charge is about 11.3 keV [46]. A fully depleted 100 µm sensor can collect about 6600 eV, assuming a production of 73 eV/µm [47]. In a 3D sensor, the amount of deposited charge and the signal amplitude do not depend on the distance or shape of the electrodes [40].

Another important feature concerns the charge collection speed [24], [40]. A very fast signal is essential to ensure good time resolution. The charge collection speed is closely related to the drift velocity of charge carriers and the distance between the electrodes [48]. A uniform drift velocity throughout the active volume of the sensor is necessary to avoid variations in the signal shape that depend on the particle impact position. This is achieved by maintaining a sufficiently high and uniform electric field to saturate the drift velocity of charge carriers (at least 30 kV/cm for electrons in silicon) [24]. A shorter charge collection time also reduces the likelihood of carrier trapping due to radiation-induced defects. In planar sensors, the signal induced by the drift of electron-hole pairs in a fully depleted sensor is fast enough for tracking applications, on the order of a few nanoseconds [29]. The amplitude and shape of the charge signal directly influence the design of the readout electronics, which must be able to process the charge signal efficiently with minimal noise and cross-talk (i.e., the signal induced by an adjacent pixel).

1.2.4 Pixel capacitance

The capacitance of the pixel is a fundamental parameter, as it directly affects electronic noise and system response time. In a hybrid pixel detector, the sensor is commonly modeled as a current source, representative of the charge induced on the electrodes, in parallel with its equivalent capacitance. This capacitance, also known as detector capacitance, is an integral part of the sensor model used for front-end optimization. It is defined as the capacitance seen from the readout circuit, which includes both the bulk capacitance of the sensor and the parasitic capacitances associated with the pixel geometry and fabrication technology.

The equivalent capacitance of the detector, C_D, can be described as a combination of several contributions, each with a different dependence on the pixel geometry. In first approximation, the dominant component is represented by the capacitance between the collection electrode and the backplane through the depleted region. This capacitance is also called bulk capacitance and it is associated with the depletion region, created following the reverse biasing of the p-n junction. In this regime, the region near the

junction is depleted of mobile carriers and behaves like a dielectric, in which the fixed charges at the edges of the region respond to voltage changes. This region can thus be modeled as a parallel plate capacitor, with active area A and thickness d, in which silicon acts as the dielectric ϵ_{Si}. The bulk capacitance can be expressed as [22]:

$$C_{bulk} = \frac{\epsilon_{Si} A}{d}, \text{ with } w = \sqrt{\frac{2\epsilon_{Si}}{q \cdot N_{eff}} V_{bias}}, \tag{1.3}$$

where V_{bias} is the reverse bias voltage, N_{eff} is the effective doping concentration, and q is the elementary charge. As the bias voltage increases, the depletion region expands, leading to a reduction in bulk capacitance. Once the depletion region is fully developed with thickness d equal to the thickness of the detector, the bulk capacitance stabilizes at a minimum value. The full depletion voltage, $V_{depletion}$, is calculated as:

$$V_{depletion} = \frac{q \cdot N_{eff} \cdot d^2}{2 \cdot \epsilon_{Si}} \tag{1.4}$$

A low bulk capacitance is desirable for several reasons. The first concerns the reduction of electronic noise, improving the signal-to-noise ratio of the system. The voltage change produced by an injected charge at the input node partially depends on the total capacitance seen at the input, which includes both the detector capacitance and all parasitic capacitances from the circuit and layout. A lower total input capacitance results in a larger voltage change for the same injected charge, thus increasing the charge-to-voltage gain of the input circuit. It is therefore important to minimize the total capacitance at the input node, not just the detector capacitance, to maximize the signal amplitude and improve noise performance. Moreover, a low bulk capacitance allows for a faster response time, as the time constant of the input circuit is proportional to the input capacitance. However, bulk capacitance is not the only contribution to the total capacitance of the pixel. Another significant contribution is the capacitance between adjacent pixels, which depends on the pixel pitch, geometric layout, i.e. the size of the electrode relative to the pitch, and the degree of lateral depletion. Finally, there are other parasitic contributions, such as the capacitance between metals in the CMOS stack (metal-to-metal), the capacitance through the insulating layers (oxide), and the fringing capacitance, due to the electric field spreading at the edges of the electrodes. The latter is particularly important in 3D sensors due to the trench geometry, which presents a non-uniform electric field.

The typical range of capacitance values for silicon pixel detectors varies from about 20 fF to over 100 fF depending on the specific configuration [6], [49], [50]. After irradiation, an increase in capacitance is observed, particularly in the inter-pixel component. This is because irradiation modifies the charge distribution in silicon and alters the properties of the substrate, such as the effective doping concentration [49], [51], [52]. However, the increase remains within an acceptable range, often below 100 fF per pixel. For some particularly optimized designs (e.g. 3D pixels or narrow geometries), the capacitance can also remain well below 50 fF, even after irradiation. In the design phase of a readout circuit, it is therefore essential to consider the types of sensors and their characteristics, in order to optimize it for specific application requirements.

1.2.5 Detector Leakage Current

The detector leakage current is another fundamental parameter for the design of the readout circuit. It is a continuous current that flows through the sensor when it is reverse-

biased [6], [26]. In an ideal reverse junction, the leakage current consists of a diffusion current. In a more realistic model, impurities, contamination, and defects induced by the manufacturing process, electronic states at the oxide-silicon interface, and other edge effects can contribute to the leakage current. All these effects make it difficult to realize detectors with a leakage current below $1\,\mathrm{nA\,cm^{-2}}$ [53]. The leakage current is considered a background noise, as it is independent of the interaction of the particle with the sensor. It can be generated due to mechanisms in the substrate or due to surface effects, mainly related to the structure of the oxide-silicon interface. The most critical effects are those related to ionizing radiation, which can generate electron-hole pairs and defects in the crystal lattice of silicon [23]. These can be intercepted by energy defects, which act as recombination centers, or transported to the electrodes by the electric field [37]. When the charges reach the electrodes, a current is generated that can be measured. The leakage current is proportional to the depleted volume $V_{depletion}$, the intrinsic charge density n_i, and the inverse of the carrier lifetime τ [24]:

$$I_{leakage} \propto \frac{q \cdot n_i \cdot V_{depletion}}{\tau} \tag{1.5}$$

with q being the elementary charge.

After irradiation, the current radiation-induced by these defects increases, becoming the dominant contribution [51]. The increase in damage, and thus in leakage current, is proportional to the fluence experienced by the sensor. Temperature also has a significant effect on the leakage current, especially after irradiation. In particular, an increase in temperature causes an increase in the kinetic energy of the charges, leading to a greater generation of electron-hole pairs. This phenomenon is described by the relationship:

$$I_{leakage} \propto T^2 \cdot e^{-\frac{E_a}{k_B T}} \tag{1.6}$$

where the exponential term is dominant, with E_a being the activation energy, approximately $1.21\,\mathrm{eV}$ for silicon [24], k_B the Boltzmann constant, and T the temperature in Kelvin. This increase is primarily driven by the exponential term in the relationship 1.6, related to the activation energy of silicon. The generation-recombination centers introduced by damage in the depleted volume significantly contribute to the generation rate of charge carriers and thus to the current [49]. For this reason, it is necessary to cool the detectors during their operation, typically between $-20\,^{\circ}\mathrm{C}$ and $-40\,^{\circ}\mathrm{C}$. Cooling is essential to reduce leakage current and prevent "thermal runaway", that is a positive feedback cycle in which an increase in current causes an increase in temperature, due to power dissipation (which is proportional to the leakage current and the bias voltage), which in turn further increases the current, leading to an exponential increase. At low temperatures, radiation-induced defects and leakage current are substantially stable over time.

Annealing periods at room temperature during operational breaks in experiments, such as maintenance periods, can have the beneficial effect of mitigating radiation damage and reducing leakage current [54]. However, annealing is a complex process that also influences the effective doping concentration [49]. There are beneficial annealing effects, which reduce the effective doping concentration and thus the depletion voltage for inverted-type materials, occurring on short time scales. Or reverse annealing effects, which increase the effective doping concentration and the depletion voltage, manifesting on longer time scales.

The increase in leakage current also directly impacts the power dissipation of the detector, as the dissipated power is proportional to the product $I_{leakage} \cdot V_{depletion}$, making active cooling strategies necessary to avoid thermal runaway phenomena. The design of the readout circuit must take into account not only the noise from electronic sources but also the component due to leakage current, which becomes significant in high-radiation environments with typical values ranging from $1nA$ to tens of nanoamperes [6], [49].

1.3 State-of-the-art in pixel readout circuits

The characteristics of the charge signal (amount, collection efficiency and velocity) are intrinsic properties of the sensor and its interaction with the particle. Sensor design (thickness, electrode geometry, doping) affects these characteristics, which in turn place stringent requirements on the front-end electronics in terms of gain, noise, bandwidth, and power consumption.

The challenge is to optimize the entire sensor-electronics system to achieve the best detection and temporal measurement performance, especially in high radiation environments.

The state of the art in the field of hybrid pixel readout is represented by the circuits developed within the international RD53 collaboration [55], established in 2013 to address the extreme requirements imposed by the High-Luminosity upgrade of the LHC (HL-LHC) at CERN. The main goal of the RD53 project is the development of fully custom readout integrated circuits, fabricated in 65 nm CMOS technology, to equip the new generations of pixel detectors for the two main LHC experiments: CMS and ATLAS. The RD53 framework has led to the realization of several prototype and pre-production versions, culminating in the ITkPix (ATLAS) and CROC (CMS) chips, currently in production and final testing. These circuits integrate analog front-end, high-speed digital readout logic, on-chip power regulation systems, and advanced radiation tolerance mechanisms. The required specifications, including support for hit rates on the order of $3\,\mathrm{GHz\,cm^{-2}}$, trigger latency up to 12.5 µs, and serial links at $5.12\,\mathrm{Gbit\,s^{-1}}$, place these ASICs at the forefront of custom electronics currently available for pixel detectors [56]. Although there are other important international research centers, such as Fermilab, Brookhaven National Laboratory and SLAC in United States, or KEK in Japan, none of them host currently operating experiments that impose levels of technological complexity, radiation, or data density comparable to those of CMS and ATLAS at CERN in Switzerland. Some of these laboratories actively participate in the development of circuits for pixel detectors (such as ASICs for X-ray experiments or precision spectrometry), but in less extreme contexts in terms of occupancy rate, radiation, and bandwidth.

For this reason, this section focuses on the RD53 project as an exemplary and representative case of the state of the art in integrated readout circuits for pixel detectors in high energy physics experiments.

1.3.1 RD53 Collaboration and the Analog Front-End (AFE) development

The Analog Front-End (AFE) development within the RD53 Collaboration is critical in the design of the pixel readout chips for the Phase-2 upgrades of the ATLAS and CMS experiments at the HL-LHC. As mentioned, the RD53 project aims to design and

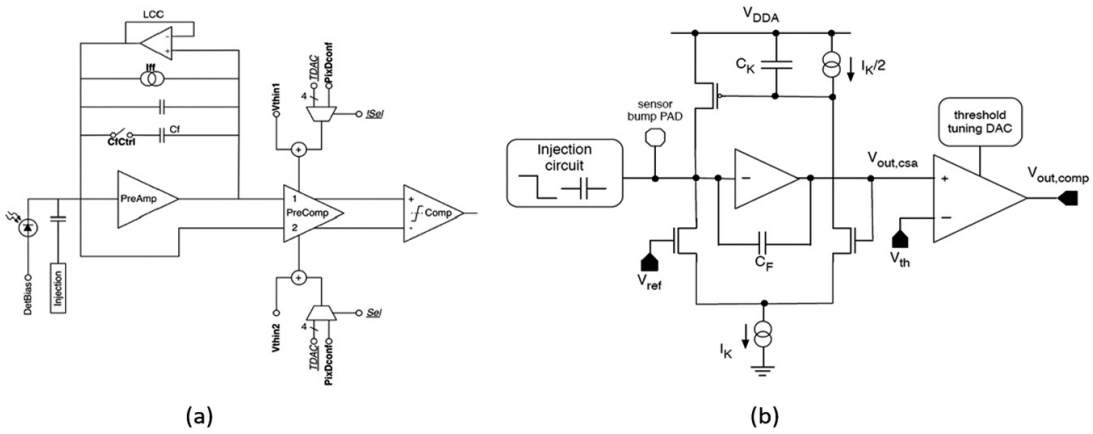


Figure 1.8: Schematic of Differential (a) and Linear front-ends [57].

qualify highly integrated radiation-hard readout ASICs for use in exceptionally harsh environments. These environments are characterized by total ionizing doses up to 1 Grad (SiO_2), hit rates exceeding 3.5 GHz cm^{-2}, aggregate data throughput beyond 5 Gbit s^{-1}, and strict power consumption constraints below 1 W cm^{-2} [57].

The readout ASICs must also comply with emerging technological constraints such as serial powering, which helps reduce material budget and cabling complexity. This is especially critical in the innermost tracking layers. Early RD53 efforts focused on radiation-tolerance studies of the selected TSMC 65 nm CMOS process [58], [59]. They also concentrated on the development and qualification of radiation-hardened building blocks (e.g. analog front-ends, ADCs/DACs, PLLs, regulators, and integrated monitoring circuitry).

The first demonstrator, RD53A, was submitted in 2017 and featured a matrix of 400×192 pixels. It implemented three different analog front-end designs and two readout architectures. This was crucial for evaluating architecture performance and guiding final design choices [60]. Based on RD53A test results and experiment-specific constraints, ATLAS and CMS opted for different analog front-end architectures: a Differential front-end for ATLAS, and a Linear front-end for CMS [5], shown in Figure 1.8. Both solutions share a similar structure comprising a charge-sensitive amplifier (CSA) with leakage current compensation and a discriminator. The threshold is globally tuned by a 10-bit DAC and equalized per pixel via a 5-bit local DAC.

The AFE output, upon signal detection, is processed by the pixel core, which performs time-over-threshold (ToT) measurements using a 6-bit counter. Of these 6 bits, 4 are retained for readout, with optional dual-slope encoding (a technique that improves dynamic range and linearity by using two different slopes for charge integration [5]). The system can be operated in single- or double-edge counting mode (where single-edge counts on one clock edge and double-edge counts on both rising and falling edges, effectively doubling the time resolution [57]) at 40 MHz or 80 MHz to balance precision and bandwidth [57].

From an architectural perspective, the pixel matrix is organized as a grid of 8×8 pixel core. These cores are tiled in rows and columns to build the full matrix, resulting in overall dimensions of 400×384 pixels for ATLAS or 432×336 pixels for CMS. This hierarchical organization is illustrated in Figure 1.9. The analog front-ends are laid out in analog islands (Figure 1.9) surrounded by synthesized digital logic, enabling efficient integration of analog and digital functions in close proximity.

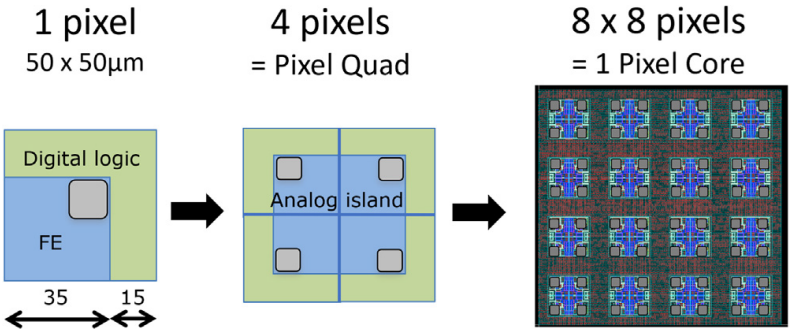


Figure 1.9: Pixel core floorplan [57].

Following RD53A, the RD53B generation introduced further refinements, culminating in the submission of RD53B-ATLAS (ItkPixV1) and RD53B-CMS (CROCv1) in 2020 and 2021, respectively. These pre-production chips served as validation platforms for the full-scale implementation of both front-end types. Final production versions, RD53C-ATLAS (ItkPixV2) and RD53C-CMS (CROCv2), were submitted to foundry in March and October 2023, respectively.

1.3.2 Medipix and Timepix readout circuits

Another important family of pixel readout circuits is represented by the Medipix and Timepix chips, developed by the Medipix collaboration (CERN, PSI, and several universities). The Medipix family is a reference platform for direct imaging of photons and ionizing particles, and is widely used in X-ray spectroscopy, electron microscopy, and space dosimetry [63]. Unlike RD53, which is optimized for high-rate particle tracking in extreme radiation environments, Medipix chips are designed for applications that require high spatial and energy resolution, typically in lower-rate or imaging contexts. Originally conceived for LHC experiments, Medipix chips have since found broad application in medical imaging, space dosimetry, and advanced X-ray imaging [66].

Several generations of Medipix chips have been developed, as summarized in Table 1.1, with each new version offering improvements in pixel count, pixel pitch, noise performance, and readout capabilities. Key features of the Medipix family include high granularity, low noise, adjustable thresholds, per-pixel threshold trimming, and, in later versions, continuous readout and charge sharing correction. The latest generations achieve readout bandwidths up to 160 Gbit s^{-1} (Medipix4) [64], [67].

To address the need for precise time measurements, the Timepix series was introduced as an extension of the Medipix architecture. Timepix chips add time-of-arrival (ToA) and time-over-threshold (ToT) measurement capabilities to the basic photon counting functionality, enabling applications such as 3D particle tracking and time-resolved imaging. Table 1.2 summarizes the main features of the Timepix chips, which have evolved from Timepix1 to Timepix4, with significant improvements in time resolution, energy resolution, and data throughput [61].

Not all Medipix and Timepix chips support Time-over-Threshold (ToT) or Time of Arrival (ToA) measurements. Early Medipix chips, such as Medipix1, Medipix2, and Medipix3, are pure photon counters: each pixel increments a counter when the signal exceeds a threshold, but does not measure how long the signal stays above threshold (ToT) or when the event occurred (ToA). Medipix3 adds features like charge summing and window discrimination for improved energy resolution, but still does not provide ToT

Table 1.1: Summary of main features for Medipix chip generations. Power and noise values are included where available. The table highlights key specifications for comparison across generations [61], [62], [63], [64], [65].

	Medipix1	**Medipix2**	**Medipix3 / 3RX**
Node	1 µm	0.25 µm	130 nm
Year	1997	1999	2005
Pixels	64×64	256×256	256×256
Pitch	170 µm	55 µm	55 µm
ENC [e^- rms]	–	$\sim$110 e^-	$\sim$80 e^- (single-pixel), $\sim$174 e^- (charge summing)
Power (analog / digital)	–	–	analog: 9 µW/pix (single), 15 µW/pix (CSM) $\approx$600 mW/chip; digital $\approx$250 mW @200 MHz
Key Features	Preamplifier, discriminator, 15-bit counter, shutter mode	Two thresholds, Krummenacher front-end, spectroscopic imaging	Charge summing mode, continuous readout, configurable counters, improved alignment

or ToA information.

The first Timepix chip, derived from Medipix2, allows each pixel to operate in Counting, ToT, or ToA mode, but only one mode per pixel per frame. Frame-based readout introduces dead time.

In ToA mode, the time resolution is 10 ns at a 100 MHz clock, with a dynamic range of about 118 µs. However, timewalk (variation of measured arrival time with signal amplitude) can reach up to 275 ns for small signals, due to limited overdrive at the discriminator input, as observed in testbeam data [61], [62].

Timepix3 is a major step forward: it uses an asynchronous, data-driven architecture, so each pixel sends its data off-chip immediately after a hit, minimizing dead time. Each pixel can simultaneously record both ToT and ToA for every event, with improved time resolution down to 1.56 ns. Fine ToA (FToA) is achieved using a shared voltage-controlled oscillator (VCO) at 640 MHz among super-pixels (groups of adjacent pixels that share certain resources, such as timing circuits, to optimize area and power). This enables precise particle tracking, 3D imaging, time-of-flight measurements, and advanced medical and scientific imaging applications [63], [66]. Timepix4, the latest generation, is fabricated in 65 nm CMOS and further improves timing, with TDC (Time-to-Digital Converter) bins of 195 ps and effective resolution below 200 ps. Timepix4 supports simultaneous measurement of both ToT and ToA for each pixel, and the chip is designed for large, tileable detector arrays using TSV (Through Silicon Via). This makes Timepix4 suitable for applications requiring extremely high time and energy resolution, such as advanced photon science, biology, and medical imaging [66], [67].

Table 1.2: Summary of main features for Timepix chip generations, including noise, time resolution, power consumption, and bandwidth. Key specifications are highlighted for comparison across generations [61], [62], [63], [67].

	Timepix	**Timepix3**	**Timepix4**
Node	0.25 µm	130 nm	65 nm
Year	2006	2013	∼2021
Pixels	256 × 256	256 × 256	512 × 448
Pitch	55 µm	55 µm	55 µm
ENC [e^- rms]	∼100 e^- (post-calibration)	∼60 e^-	–
Time resolution	–	∼1.2–1.6 ns (beam tests)	∼200 ps (binning)
Power (analog / digital)	–	analog: ∼500 mA/chip, digital: ∼400 mA @1.5 V (∼1.35 W)	digital: ∼25% less than Timepix3; analog: ∼5% more
Max rate / Bandwidth	frame-based; ∼60 Hz (Timepix telescope)	up to ∼80 MHz hits/s/chip @5.12 Gbps link	max ∼10.8 kHz/pixel (∼357 Mhits/cm^2/s); CRW mode ∼800 Ghits/cm^2/s, bandwidth ∼160 Gb/s
Key Features	Counting, ToT or ToA (one mode/pixel/frame), frame-based, dead time during readout	Data-driven, simultaneous ToT and ToA, fine ToA (FToA), dead-time free, high rate	Sub-200 ps TDC, simultaneous ToT/ToA, TSV for tiling, high bandwidth, advanced calibration

Timepix and Medipix are solutions that have been widely used in various applications, including medical imaging, radiation detection, and particle physics. Their ability to provide both spatial and temporal information makes them versatile tools for advanced imaging and detection tasks. One of the interesting fields in which systems like that may be used is in the field of photon science and X-ray imaging, where the ability to detect and analyze X-ray photons with high precision is crucial for understanding material properties, biological structures, and fundamental physical processes. The next section will discuss the specific requirements and challenges of photon detection in X-ray imaging, particularly in the context of Free Electron Lasers (FELs), and how advanced pixel readout circuits address these challenges.

1.4 Photon science and X-ray imaging

Although high energy physics is a primary driver for the development of silicon pixel sensors and dedicated microelectronics, many other scientific fields also require the detection

Table 1.3: Support for ToT and ToA features in Medipix and Timepix chip generations.

Chip Generation	**ToT Support**	**ToA Support**
Medipix1	No	No
Medipix2	No	No
Medipix3	No	No
Timepix1	Yes (one mode/pixel/frame)	Yes (one mode/pixel/frame)
Timepix3	Yes (simultaneous)	Yes (simultaneous)
Timepix4	Yes (simultaneous)	Yes (simultaneous)

of particles, especially photons, with high spatial, temporal, and energy resolution. Notable examples include photon science and X-ray imaging, which are essential in medical diagnostics, industrial inspection, and large-scale synchrotron light laboratories.

In these contexts, silicon pixel detectors are widely used for X-ray photon detection across a broad energy spectrum, from soft X-rays (hundreds of eV) to hard X-rays (tens of keV). These detectors may operate in triggered or continuous acquisition modes, the latter being increasingly important for modern applications. Compared to high energy physics, X-ray imaging applications impose somewhat different requirements. Detectors must have high quantum efficiency (the ability to convert incoming photons into measurable signals), low noise, and wide dynamic range (to accurately measure both low and high photon counts). Fast readout speeds and, in some cases, energy discrimination capability are also required. All these features must be achieved while maintaining high spatial and temporal resolution. The associated readout circuits are specifically designed to address the unique characteristics of X-ray photons and the demands of imaging systems.

A key challenge in X-ray imaging is the need to detect single photons with high precision. For example, in applications such as X-ray fluorescence spectroscopy or coherent diffraction imaging, the ability to count individual photons is crucial for accurate measurements. However, this capability is fundamentally limited by the statistical nature of photon emission and detection, known as the *quantum limit* or *Poisson limit*. This is a fundamental physical limit imposed by the laws of quantum mechanics and not a technical limitation of the detector or electronics. The quantum limit refers to the intrinsic statistical fluctuations that occur when counting discrete events like photons. These fluctuations follow a Poisson distribution, meaning that the variance in the number of detected photons equals the mean number detected. This sets a fundamental noise floor, called *shot noise*, that cannot be reduced by any improvement in detector or electronics technology, because it originates from the discrete and random nature of photon arrival itself, rather than from imperfections or limitations in the electronic readout.

For a pixel detecting on average μ photons, the standard deviation (quantum or shot noise) is $\sqrt{\mu}$. For example, if a pixel detects on average 100 photons of 9 keV each, the quantum-limited noise is 10 photons. Since the energy necessary to generate an electron-hole couple in silicon is 3.6 eV, then each 9 keV photon generates about 9000 eV/3.6 eV $\approx$ 2500 electron-hole pairs, a 10-photon noise corresponds to $10 \times 2500 = 25000$ electrons.

The electronic noise of the readout circuit, typically quantified as Equivalent Noise Charge (ENC), must be much smaller than the quantum-limited noise to avoid degrading the signal-to-noise ratio (SNR) set by photon counting statistics. This requirement can be formalized as:

$$\mathrm{ENC} \ll \sqrt{\mu} \times \frac{E_\gamma}{w}$$

where E_γ is the photon energy and w is the energy required to create an electron-hole pair in silicon (3.6 eV). For the example above:

$$\text{ENC} \ll 10 \times 2500 = 25000 \text{ electrons}$$

In practice, for applications requiring single-photon sensitivity, the SNR for the minimum signal of interest (i.e., a single photon) with respect to the electronic noise should be at least 10–15 [68], [69]:

$$\text{SNR} = \frac{Q_{\text{photon}}}{\text{ENC}} > 10$$

where Q_{photon} is the charge generated by a single photon. For a 9 keV photon, $Q_{\text{photon}} \approx 2500$ electrons, so the ENC should be below 250 electrons for SNR = 10.

Ensuring that the electronic noise is much lower than the quantum-limited noise for the expected photon count guarantees that the detector operates at the quantum limit. This is important because it means the detector's resolution is fundamentally limited only by unavoidable photon counting statistics (shot noise), rather than by imperfections in the electronic readout. Additionally, keeping the noise much lower than the charge generated by a single photon ensures single-photon sensitivity.

In detectors with analog pipelines (such as AGIPD), signals are stored on capacitors. An analog pipeline is a series of storage cells (capacitors) within each pixel that temporarily hold analog signals before they are digitized and read out, allowing the detector to capture multiple frames at high speed. It is crucial that any signal loss due to capacitor or switch leakage is much smaller than the Poisson statistical uncertainty, so that the electronics do not introduce errors larger than the unavoidable fluctuations from photon counting. In digital pipelines, this issue is essentially absent. Even in detectors with dynamic gain switching (such as JUNGFRAU), the charge injected during switching must be negligible compared to the statistical noise of photon counting. A brief overview of these systems, mainly conceived for FEL applications, will be provided later in this section.

1.4.1 Free Electron Lasers (FEL) working principles and applications

The concept of Free Electron Lasers (FEL) was first proposed by John Madey and later experimentally demonstrated by his group at Stanford University in the 1970s [70]. FELs are sources of coherent light, meaning they emit photons that are not only in phase with each other but also share the same frequency and direction; in other words, coherence in FELs refers to both the phase relationship and the uniformity of frequency among the emitted photons, which is essential for producing highly focused and intense beams. These instruments exploit the relativistic motion of a beam of free electrons—not bound to a crystal lattice, meaning they are free to be accelerated to very high energies, unlike electrons in solids whose motion is restricted by the lattice structure—to generate electromagnetic radiation. In this type of laser, light amplification occurs through the interaction between an accelerated electron beam and a periodic magnetic field, called an *undulator* or *wiggler* [70], [71]. The resulting emission can cover a wide frequency spectrum, from microwaves to hard X-rays, with high brilliance. A key metric for FELs, formally defined as the power density of the emitted radiation per unit area per unit solid angle and temporal resolution down to the femtosecond regime. These properties make FELs fundamental tools in photon science, especially for studies requiring ultrashort pulses and high intensity.

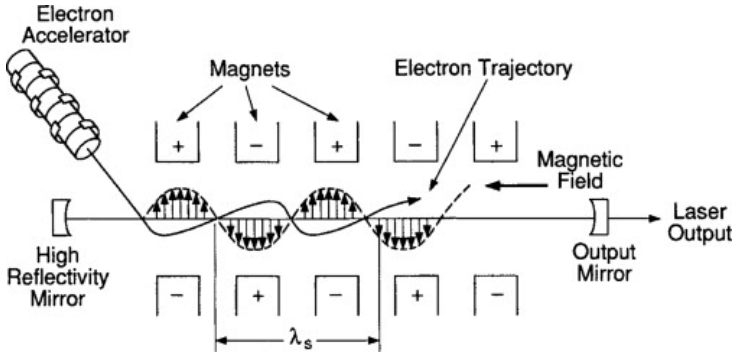


Figure 1.10: Functional scheme of a Free Electron Laser (FEL) [72]. The electron beam is accelerated in a linear accelerator and then passes through an undulator, where it emits coherent radiation.

Referring to Figure 1.10, the operation of a FEL can be described by considering the use of an accelerator, typically a linac, required to generate a beam of electrons with relativistic energies, typically on the order of GeV, with low emittance (i.e., a narrow angular distribution) and high peak current. This accelerated electron beam is made to interact with a periodic magnetic field, called an undulator, which induces a transverse oscillatory motion in the electrons, causing the emission of synchronous radiation, i.e., radiation emitted in phase with the motion of the electrons. To achieve the required high energies, the acceleration of the electrons takes place in special resonant cavities made of superconducting material.

The core of FEL operation is the process of Self-Amplified Spontaneous Emission (SASE). The radiation emitted by the electrons, being faster than the electrons themselves along the path into the undulator, overtakes them and interacts with them. This interaction accelerates some electrons and slows down others, gradually causing them to organize into "microbunches". In other words, microbunching means that electrons group together at intervals matching the wavelength of the emitted radiation, so that all electrons in a micro-bunch emit photons coherently (in phase). This collective, synchronized emission causes the intensity of the radiation to grow exponentially as the electron beam travels through the undulator.

As the amplification process continues, the FEL eventually reaches a saturation regime, where the growth of the emitted radiation intensity no longer increases significantly with distance along the undulator. This occurs because the average energy of the electron beam decreases as energy is transferred to the radiation, and the energy spread of the beam increases. These effects alter the resonance conditions, causing the gain rate to become negligible. At this stage, energy begins to oscillate between the wave and the electrons, meaning that energy is periodically exchanged back and forth between the electron beam and the emitted radiation, rather than accumulating solely in the wave. Under these conditions, the emitted radiation is coherent and highly directional, with characteristics similar to those of an optical laser, but extended to much shorter wavelengths. For example, while typical optical lasers emit in the range of hundreds of nanometers, FELs can reach wavelengths as short as a fraction of a nanometer, including the soft and hard X-ray regime.

X-ray FELs have revolutionized numerous scientific fields thanks to their ability to produce short and brilliant pulses. The main applications include single-pulse crystallography, which enables the study of the three-dimensional structure of biomolecules without

damaging them; femtosecond microscopy, which allows observation of atomic dynamics and phase transitions in materials on ultrafast timescales; and nonlinear X-ray spectroscopy, which investigates electronic states and transients in complex systems. These techniques have opened new frontiers in the understanding of fundamental processes in physics, chemistry, structural biology, and materials science.

The high brilliance of FELs, combined with the rapid repetition rate of pulses (up to MHz), imposes very stringent requirements on photon detection systems. Detectors must be able to handle tens of millions of photons per pixel per pulse without saturation or damage, while also being capable of low-noise operation and single-photon precision.

The global landscape of X-ray free-electron lasers (FELs) is dominated by four major research infrastructures: the European XFEL (also known as EU-XFEL) in Germany, the Linac Coherent Light Source (LCLS) at the Stanford Linear Accelerator Center (SLAC) in California, the SPring-8 Angstrom Compact free electron LAser (SACLA) in Japan, and the SwissFEL at the Paul Scherrer Institute (PSI) in Switzerland. The European XFEL, operational since 2017, is the largest facility of its kind in the world and is capable of producing about 27,000 X-ray pulses per second thanks to its superconducting accelerator [73]. In the United States, the LCLS at SLAC, active since 2009, was the first FEL to achieve emission at wavelengths on the order of an ångström [74]. In Japan, SACLA (operational since 2012 at the SPring-8 Center) generates X-rays with the shortest currently available wavelength (0.06 nm) [75]. Finally, it is worth mentioning the SwissFEL at the Paul Scherrer Institute (PSI) in Switzerland, which is a compact X-ray free-electron laser facility that started operations in 2017 and is designed to produce high-brilliance X-ray pulses for a wide range of scientific applications [76].

To meet the challenges posed by X-ray imaging at FELs, such as extremely short wavelengths (on the order of one Ångström) and intense laser beams enabling nanometer-scale imaging, hybrid pixel detector solutions have been developed.

In the context of the EU-XFEL, three distinct detection systems have been developed, each optimized for specific requirements in terms of X-ray energy, peak frame rate, and dynamic range: DSSC (DEPFET Sensor with Signal Compression), LPD (Large Pixel Detector), and AGIPD (Adaptive Gain Integrating Pixel Detector). While sharing the common goal of supporting the high intensity and repetition rate of XFEL pulses, each system has specific characteristics. The DSSC is optimized for low-energy X-rays (soft X-rays) and is based on DEPFET technology with signal compression and in-pixel digitization [77]. The LPD, on the other hand, is designed for high-energy X-rays (hard X-rays) and features large pixels and an analog memory for each pixel [78]. The AGIPD instead is designed with a three gain adaptive amplifier and a memory for each pixel, allowing it to handle a wide dynamic range and high frame rates [79]. The following sections focus on DSSC and AGIPD, as two different examples of systems that implement dynamic compression and represent state-of-the-art solutions for pixel readout in X-ray imaging applications.

1.4.2 DSSC detector

The DSSC (DEPFET Sensor with Signal Compression) is a two-dimensional solid-state detector designed for soft X-rays (approximately 0.25 keV–6 keV). Development began in 2009 as a collaboration between DESY, the University of Heidelberg, Politecnico di Milano, and the University of Bergamo. The first 1 Mpixel version uses passive hexagonal mini-SDD (Silicon Drift Detector) silicon sensors with a side length of 136 µm; a

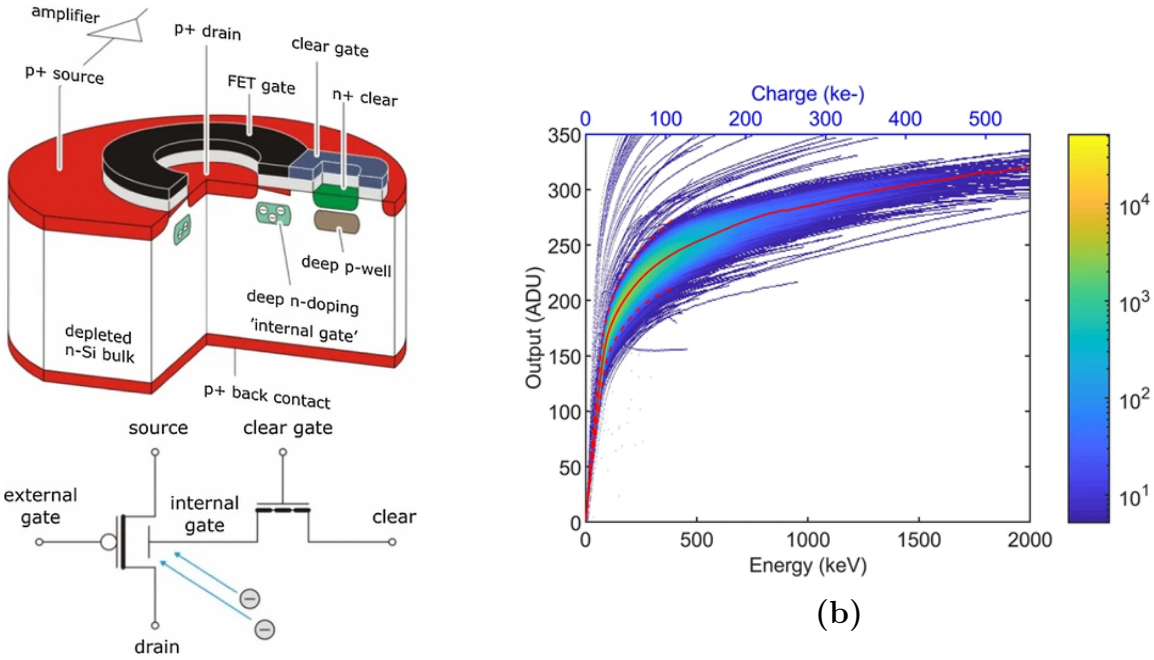


Figure 1.11: (a) Structure (top) and circuit representation (bottom) of a conventional spectroscopy-grade DEPFET cell [80], with the gate buried in the silicon substrate for high charge collection efficiency and signal compression; (b) Superposition of DEPFET characteristics (dashed curves) with the average characteristic (red curve) [77].

second version has been developed featuring active DEPFET sensors with intrinsic signal compression. DEPFET sensors incorporate an active MOSFET transistor directly into each pixel, which acts as a charge amplifier. This design results in extremely low input capacitance, a key factor for achieving excellent single-photon energy resolution.

As shown in Figure 1.11a, a distinctive feature of the DEPFET is its internal gate, buried within the silicon substrate, which collects the charge generated by incoming X-ray photons. The substrate doping profile is carefully engineered so that the DEPFET sensor exhibits an intrinsically logarithmic response to the collected charge. As illustrated in Figure 1.11b, the superposition of the transfer characteristics from multiple DEPFET cells demonstrates both the logarithmic behavior at high signal levels and the excellent linearity at low energies, enabling the detector to achieve high dynamic range without compromising single-photon resolution. As the collected signal increases, the effective gain of the amplifier decreases, allowing the pixel to handle a much wider range of signal intensities. In practical terms, this means that a single pixel can accurately measure signals ranging from individual photons up to approximately 10^4 photons of 1 keV, all without saturation. The DEPFET sensors used in the DSSC detector are fabricated on thick, high-resistivity silicon wafers (approximately 725 µm in thickness). This increases the amount of charge collected from each photon (improving quantum efficiency) and provides effective shielding for the integrated transistors against ionizing radiation.

Figure 1.12 shows the channel diagram of the DSSC detector. Each DSSC ASIC channel includes a bias current subtraction stage, an analog filter, a single-slope ADC, and a static memory. The ADC is calibrated so that, in the linear region of the DEPFET sensor, each photon corresponds to a distinct ADC code; in the compressed region, multiple

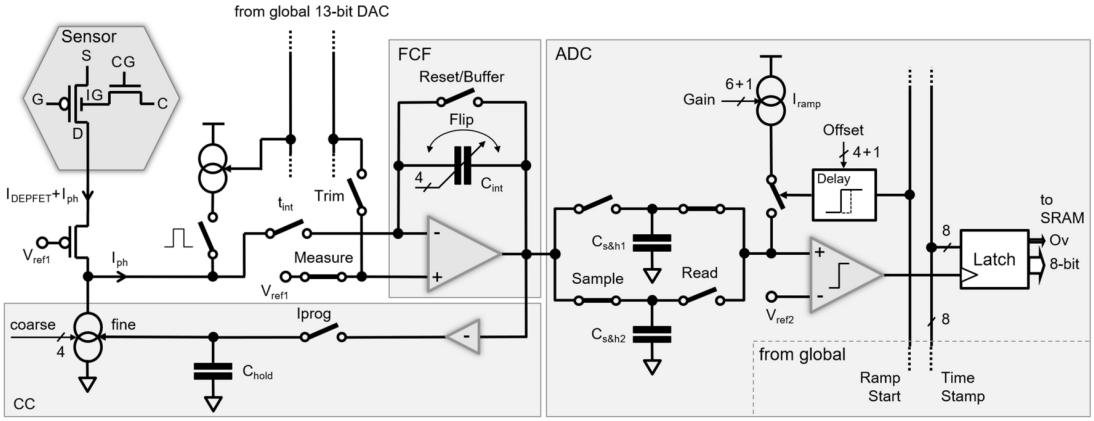


Figure 1.12: Channel diagram of the DSSC detector, illustrating the signal flow from the DEPFET sensors through the readout ASICs to the data acquisition system [77].

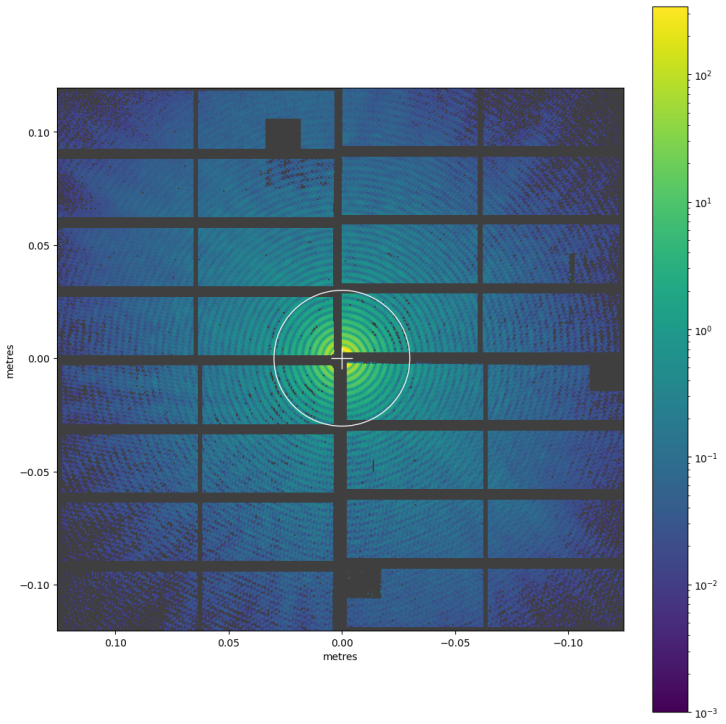


Figure 1.13: Azimuthal view of the DSSC detector ladders, highlighting the arrangement of the pixel modules and their connection to the readout electronics.

photons are mapped to the same code. Therefore, good DNL (Differential Nonlinearity, which measures the uniformity of step sizes between adjacent ADC codes) performance of the ADC is crucial, while INL (Integral Nonlinearity, which quantifies the overall deviation from the ideal transfer function) is less critical. The DEPFET bias current is subtracted using a 4-bit DAC and finely adjusted in closed-loop before each XFEL burst. To compensate for residual variations, correlated double sampling is used. The integrator filter performs optimal trapezoidal weighting for series white noise, with three integration phases that allow baseline cancellation. The filter gain is adjustable via combinations of feedback capacitors and integration times programmed by the digital sequencer. At the ADC input, two sample-and-hold circuits operate in pipeline: while one is charging, the other is being digitized. The digitized signal is stored in a custom in-pixel SRAM. The SRAM is organized in blocks shared among groups of pixels and read out serially to reduce routing complexity. The DSSC detector is designed to operate at a maximum frame rate of 4.5 MHz and can handle up to 10 000 photons per pixel per pulse without saturation, with a dynamic range of about 1000 in the linear region. The readout system is capable of processing data at a rate of 10 Gbit s^{-1} per channel, allowing for high-speed data acquisition and real-time processing. The final DSSC detector consists of a megapixel array comprising 1024×1024 hexagonal pixels, each with a side of 136 µm, covering an area of about 210 mm×210 mm. The array is organized into 16 independent ladders, with each ladder containing 512×128 pixels (for a total of approximately 64k pixels per ladder). These ladders are arranged to leave a central hole for the primary X-ray beam, as illustrated schematically in Figure 1.13. Each ladder consists of a focal-plane module with two monolithic DEPFET sensors, bump-bonded to four CMOS readout ASICs fabricated in a 130 nm technology. In total, the full detector comprises 16 ladders × 65 536 pixels per ladder (1 048 576 pixels), with each ladder further organized into 8 octants of 32×32 pixels per sensor. Every pixel has its own dedicated analog and digital readout channel, enabling fully parallel readout across the entire array. The DSSC detector has been successfully used in various experiments at the European XFEL, including studies of biological samples, materials science, and fundamental physics. Its ability to provide high-resolution images with low noise and high dynamic range has made it a valuable tool for researchers in these fields [80], [81].

1.4.3 AGIPD detector

The AGIPD (Adaptive Gain Integrating Pixel Detector) was developed for applications such as coherent diffraction imaging (CDI) and X-ray photon correlation spectroscopy (XPCS) at the European XFEL. It features a pixel size of 200 µm, optimized for an angular resolution of 0.1 mrad at typical sample-to-detector distances. The detector must handle a high dynamic range, from single-photon sensitivity up to more than 10,000 photons per pixel. It must also tolerate radiation doses up to 1 GGy over a 3 years operational lifetime [82].

A key requirement is the ability to store images at the XFEL's high repetition rate of 4.5–5 MHz during the 0.6 ms pulse train. Indeed, in the XFEL pulse structure, a burst of closely spaced X-ray pulses is delivered over a short interval (the pulse train), followed by a much longer gap before the next train. This timing is crucial because it allows the detector to rapidly capture and temporarily store hundreds of images during the pulse train, with readout and digitization occurring in the subsequent 99.4 ms interval when no new data is arriving [83], [84]. This is achieved by integrating an analog memory pipeline

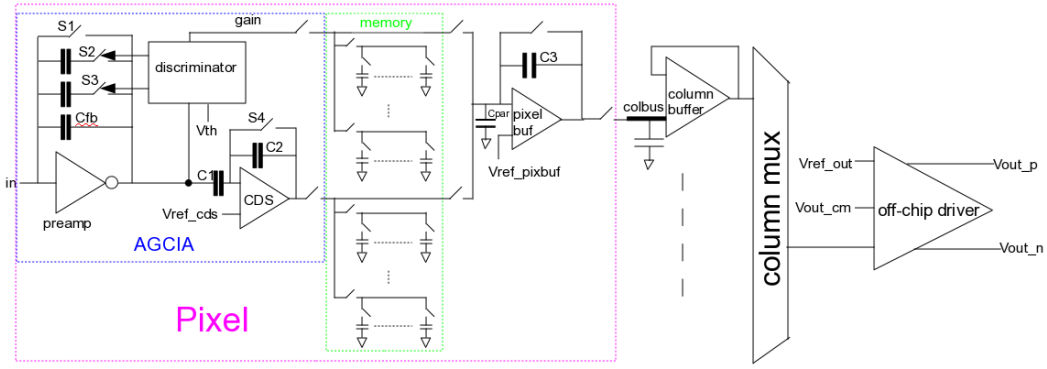


Figure 1.14: The block diagram of the AGIPD analog readout chain.

within each pixel, capable of storing up to 352 images per train.

The AGIPD achieves its wide dynamic range through an adaptive gain amplifier in each pixel, which automatically switches between three gain settings (high, medium, low) depending on the input signal. The gain state is selected by local comparators based on the collected charge and is stored for each pixel together with the signal, enabling accurate calibration and signal reconstruction. This allows for single-photon resolution at energies above 6 keV in high gain, while preventing saturation at high photon counts. The combination of radiation-tolerant sensor and ASIC design (for reliability under high doses), fast analog storage (enabling high frame rates), and adaptive gain (providing wide dynamic range) makes AGIPD a state-of-the-art solution for high-rate, high-dynamic-range X-ray imaging at FEL facilities.

Figure 1.14 shows the block diagram of the AGIPD analog readout chain. The basic architecture of each pixel cell consists of an integrator with selectable feedback capacitors and an analog memory pipeline. By selecting feedback capacitors of different sizes, the integrator can be adapted to handle a wide input dynamic range. In adaptive gain mode, the pixel local comparators monitor the input signal and automatically switch between feedback capacitors during charge integration, thereby adjusting the gain to prevent saturation and maintain sensitivity; the selected gain setting is stored together with the data for accurate reconstruction (see also [85]). The charge collected in each pixel is temporarily stored in an analog memory pipeline, capable of operating at the XFEL repetition rate of 5 MHz during the 600 μs pulse train. To achieve the required memory depth (up to 352 images per pixel), the storage capacitors must be small enough to fit within the limited pixel area (200 µm × 200 µm). At the same time, they must be large enough to minimize charge loss during the hold time and ensure high analog resolution. The technology used for the AGIPD ASIC is IBM 130 nm CMOS, chosen for its radiation tolerance (up to 1 Grad over three years of operation), further enhanced by dedicated rad-hard layout techniques [83]. The sensor consists of a p^+ implant on an n-type silicon substrate with a thickness of 500 µm and pixel dimensions of 200 µm × 200 µm, offering quantum efficiency above 98 % up to 12.4 keV. The readout electronics use FPGA boards for ASIC control, image digitization (with 14 bit resolution), and data transmission via 10 Gbit s^{-1} optical links. An external veto signal, which is generated by the experiment control system, enables selective overwriting of images during the pulse train; this mechanism is used to discard unwanted or uninformative frames (for example, those not corresponding to valid experimental conditions), thereby maximizing the number of useful images stored and read out for analysis. AGIPD performance includes an equivalent noise charge (ENC) of

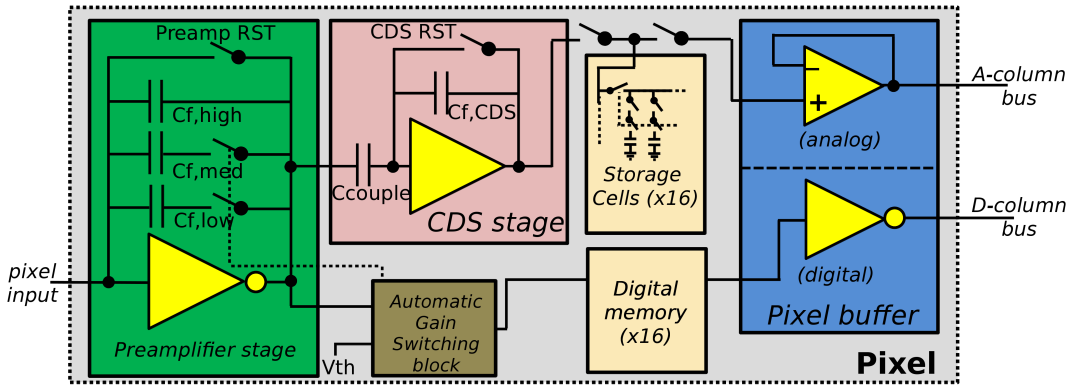


Figure 1.15: Block view of a JUNGFRAU02 pixel [86].

about 320 electrons in production and below 300 electrons in prototypes, ensuring single-photon resolution with a signal-to-noise ratio above 10 for a 12.4 keV photon in high gain. The dynamic range reaches 10 000 photons of 12.4 keV per pixel, with non-linearity below 0.44 % up to 5000 photons.

Internal calibration sources, such as the current source and pulsed capacitor, are essential features integrated directly into the AGIPD ASIC. These sources enable rapid and automated calibration of the detector's dynamic range, eliminating the need for slow and cumbersome external calibration methods (e.g., using X-ray sources like molybdenum foils). This is particularly important given the enormous number of calibration parameters—over 2.8 billion for a one-megapixel system—which would make external-only calibration impractical.

Since 2017, AGIPD has been successfully used in user experiments, including the first MHz femtosecond serial crystallography and coherent diffraction imaging (CDI) and X-ray photon correlation spectroscopy (XPCS), where its high dynamic range, fast frame rate, and single-photon sensitivity have enabled groundbreaking scientific results and new experimental capabilities.

1.4.4 JUNGFRAU detector

Another important example of a hybrid pixel detector for X-ray imaging is the JUNGFRAU (adJUstiNg Gain detector FoR the Aramis User station) detector, developed at the Paul Scherrer Institute (PSI) in Switzerland for the SwissFEL X-ray free-electron laser. Although originally designed for SwissFEL, which operates at a 100 Hz repetition rate, JUNGFRAU is now widely used at advanced synchrotron facilities as well [87], [88].

JUNGFRAU is a modular system. Each module consists of a $4 \times 8\,\mathrm{cm}^2$ silicon sensor bump-bonded to eight readout ASICs. The pixel pitch is 75 µm, similar to leading photon-counting detectors for synchrotrons. Each ASIC contains a 256×256 pixel matrix, and multiple modules can be combined to build large-area detectors with tens of millions of pixels [86], [87], [88].

Each pixel, whose architectural diagram is shown in Figure 1.15, includes a preamplifier with dynamic gain switching, which automatically selects one of three gain levels using local comparators based on the collected charge. This enables both single-photon sensitivity (down to energies below 800 eV) and a very high dynamic range, up to about 10^4 photons of 12 keV per pixel (about 110 dB). The first gain stage (G0) covers single-photon signals up to ∼20–25 photons at 10 keV, the second (G1) extends the range to

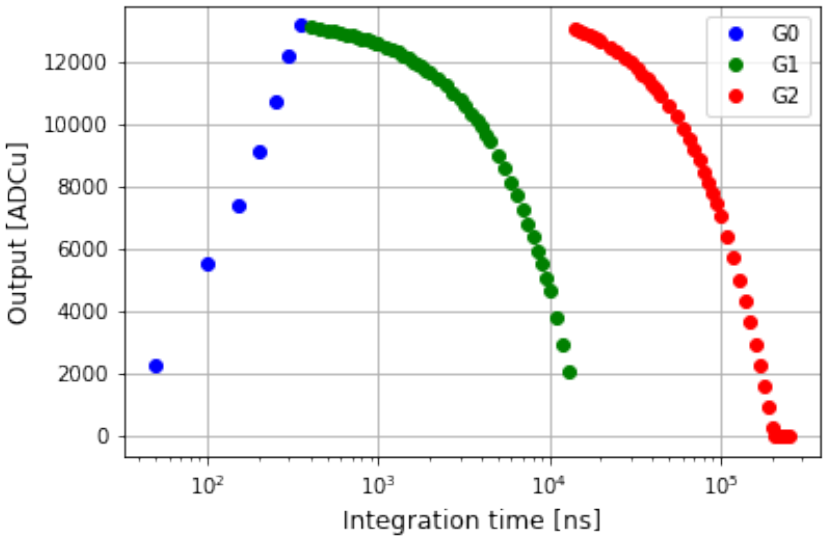


Figure 1.16: Example of pixel switching gains during an internal current source scan, when the pixel gain switching mechanism is calibrated by providing a constant current and increasing the integration time [88]. The gain switching is controlled by the pixel's internal logic, which selects the appropriate gain based on the collected charge.

500–600 photons, and the third (G2) up to 8000–10000 photons. The selected gain for each pixel is stored, producing a "gain map" for every frame to enable accurate signal reconstruction [86], [87]. Figure 1.16 shows an example of gain switching during an internal current source scan, where the pixel gain switching mechanism is calibrated by providing a constant current and increasing the integration time.

A local analog memory with 16 cells is integrated in each pixel, allowing fast image sequences to be captured before readout. In continuous mode, the system supports dead-time-free operation up to 2.2 kHz, corresponding to the maximum frame rate at which data can be read out without loss. In burst mode, the analog memory enables the detector to capture up to 16 consecutive frames at rates as high as 4.5 MHz before readout, making it suitable for experiments requiring rapid acquisition of short image sequences. The typical energy range spans from $\sim$ 2 keV to several tens or hundreds of keV. The detector achieves linearity above 99%, and maintains single-photon sensitivity up to 4 keV.

The readout ASIC (ROC) is fabricated in UMC 110 nm CMOS technology. Early prototypes (JUNGFRAU0.1, 48×48 pixels) demonstrated the expected performance in terms of power, noise, linearity, and speed, with improvements made in later versions [86], [87].

1.5 FALAPHEL and PiHEX projects

In the context of research and development of advanced integrated circuits for high-energy physics (HEP) and high-intensity scientific imaging applications, such as those based on Free-Electron Lasers (FELs), the FALAPHEL and PiHEX projects represent two landmark initiatives at the national level. Although distinct in their specific objectives, the two projects complement each other within a shared technology strategy: FALAPHEL, funded by the Istituto Nazionale di Fisica Nucleare, focuses on developing ultra-high-

speed photonic data links and 28 nm, rad-hard CMOS electronics, while PiHEX, funded by the Ministero dell'Università e della Ricerca in the context of the PRIN 2022, advances pixel-level front-end architectures and signal processing techniques. Together, they drive the adoption and maturation of the 28 nm CMOS node for high-performance, radiation-tolerant applications. Both particle physics and photon science rely on advanced detection systems to study fundamental processes. As mentioned, silicon detectors, whether pixel or strip-based, are equipped with specialized readout circuits to capture and process the electrical signals generated by particle interactions. Projects such as FALAPHEL and PiHEX specifically advance these technologies by developing next-generation, radiation-tolerant front-end electronics and photonic data links, enabling higher speed, improved timing accuracy, and robust operation in extreme environments.

The choice of the 28 nm CMOS technology from TSMC for both the projects proved strategic, as it allows for the realization of high-density digital blocks and analog circuits with greater bandwidth than previous nodes, while maintaining good robustness to total ionizing dose (TID) effects. In particular, SerDes circuits and drivers for optical modulators with a target of 25 Gb/s have been developed, along with PLL frequency synthesizers, CDR circuits, analog references, and front-ends for pixel cells of $25 \times 50\,\mu\text{m}^2$. The photonic architectures investigated are Mach-Zehnder modulators and ring resonators, with a specific focus on wavelength division multiplexing (WDM) to achieve aggregate transmission capacities of up to 100 Gb/s on a single fiber. From the perspective of rad-hardness, FALAPHEL set the ambitious goal of surpassing the limits of previous developments in 65 nm technology (such as LpGBT and Versatile Link+), aiming for TID tolerances greater than 1 GRad and neutron fluences exceeding $5 \times 10^{16}\,\text{n/cm}^2$.

PiHEX focuses on the development and optimization of circuit architectures dedicated to signal processing in hybrid pixel detectors. The project pays particular attention to requirements imposed by extreme environments, such as radiation, speed, and timing accuracy. The design activities did leverage the 28 nm CMOS technology to develop rad-hard preamplifiers. These preamplifiers are equipped with active reset mechanisms for compensating leakage currents. The project also includes discriminators with integrated DACs for threshold definition and digital counters for measuring Time-over-Threshold (ToT) and Time-of-Arrival (ToA). In the first submitted demonstrator, an 8-bit ToA counter (clocked at about 640 MHz) and a 5-bit ToT one (40 MHz) are shared among groups of pixel columns.

The solutions proposed by PiHEX also aim to ensure full operability even under extreme radiation conditions, with TID robustness targets exceeding 10 GRad and single-event effects (SEE) tolerance.

For both projects, the design approach for the implementation of front-end channels is shared. The design of the main analog building blocks is based on the classical shaperless front-end for readout of pixel sensors. The architecture of the front-end is shown in Figure 1.17. The analog processor includes, as the very first stage, a charge sensitive amplifier, also referred to as the preamplifier, which is connected to the pixels sensor and which provides amplification and charge-to-voltage conversion of the signal delivered by the detector. The conversion depends on the value of the capacitor C_F. The preamplifier also includes a feedback network, which usually serves a double fold purpose: on one hand, such a network is exploited to restore the preamplifier output baseline after signal arrival, on the other hand it can be designed in such a way to compensate for the detector leakage current, which is expected to increase with radiation [89]. Different solutions have been proposed for leakage compensation, with the Krummenacher topology being

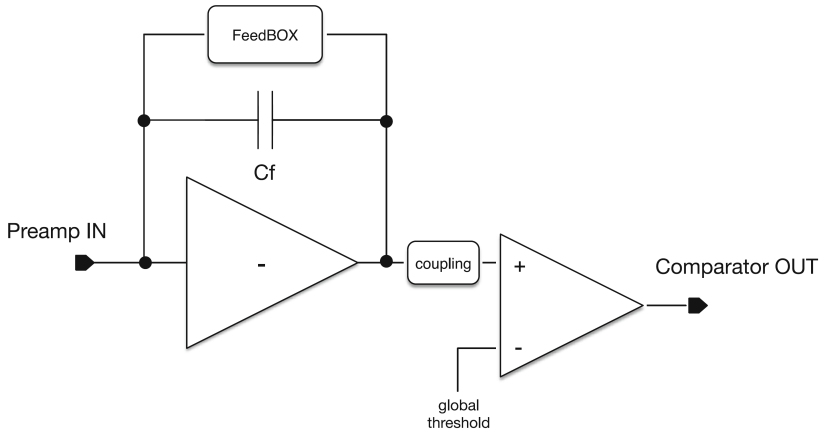


Figure 1.17: Block diagram of a typical shaperless front-end for the processing of the signal delivered by a pixel sensor [89]

one of the most used in the High Energy Physics (HEP) domain [90]. The core of the charge sensitive amplifier is an inverting gain stage, which should provide sufficiently high open loop gain in order to minimize the input impedance of the preamplifier and the pixel-to-pixel crosstalk. The noise optimization of the gain stage is crucial: definitely, the minimum threshold at which the front-end can be operated is strongly related to the noise performance of such a stage. The signal from the preamplifier is then fed to a threshold discriminator, which compares the CSA signal with a global threshold that can be eventually adjusted at the pixel level to achieve high uniformity, from pixel to pixel, in the front-end response. The threshold discriminator, or comparator, can be AC or DC coupled to the preamplifier output, depending on the application and the comparator architecture.

The research activity of this thesis has focused specifically on the development of the analog front-ends for the FALAPHEL and PiHEX projects. The architectures, circuit solutions, and experimental results related to these front-ends will be described in detail in chapters 3 and 4.

Chapter 2

Characteristics of 28 nm CMOS Technology

Understanding the technological characteristics of the 28 nm CMOS process is a fundamental step in this research, as the developed readout channels is based on this technology. In particular, understanding its noise performance and radiation hardness is crucial to ensure the suitability and reliability of the circuits in high-radiation environments.

The 28 nm CMOS technology is the last bulk planar process before the introduction of FinFET transistors [1]. The research and development phase of this technology node began around 2009, with prototypes related to a low power (LP) version, rapidly progressing to mass production in the second half of 2011. The Taiwan Semiconductor Manufacturing Company (TSMC) was the first to introduce this technology [91], followed by other manufacturers such as GlobalFoundries [92] and Samsung [93]. This technology process was quickly adopted in consumer products, especially System on Chip (SoC) for mobile devices, Graphical Processing Unit (GPU) and Field Programmable Gate Array (FPGA). For example, Apple used the 28 nm CMOS for the Apple A6 processor in 2011 to be integrated into the iPhone 5 smartphone. Another example is Xilinx, which used this technology for the 7-series FPGA family, such as the Artix-7 model, launched in 2012.

The 28 nm CMOS node was largely a linear shrinkage of 90% from the 32 nm node, meaning a reduction in transistor size compared to the previous node while maintaining the same basic architecture [94]. However, the peculiarity of this technology lies in the High-k Metal Gate (HKMG), which involves the use of a metal contact for the gate and the introduction of a new dielectric material between the gate and the substrate, replacing the traditional silicon oxide (SiO_2) in the high-performance (HP) and High Performance Low Power (HPL) variants [95], [96]. This new high-k dielectric material, which can be hafnium dioxide (HfO_2), allows for reduced leakage current and improved transistor performance, enabling thinner gate thicknesses without compromising electrical performance. In fact, a thinner gate thickness allows for a reduction in the transistor threshold voltage, enabling operation at lower voltages and improving energy efficiency. The threshold voltage is inversely proportional to the gate capacitance. The latter is described by the relationship:

$$C_{gate} = \frac{\varepsilon_{ox} A}{t_{ox}} \tag{2.1}$$

where C_{gate} is the gate capacitance, ε_{ox} is the dielectric constant of the gate dielectric material, A is the gate area, and t_{ox} is the thickness of the gate oxide. This means that, keeping the gate area constant, a higher dielectric constant ε_{ox} or a thinner gate oxide thickness t_{ox} lead to a greater gate capacitance. For a given gate thickness, the

use of a standard dielectric material would risk creating an opening in the gate, creating a conductive channel between the gate and the transistor channel, making it unusable. The use of a metallic material for the gate, instead of polysilicon, allows for a reduction in gate resistance and improved transistor performance, particularly for high-speed and low-power applications, helping to lower the threshold voltage.

Thanks to these innovations, the 28 nm CMOS technology has achieved significantly better performance compared to previous nodes, with a reduction in supply voltage and an increase in integration density. To date, it is still widely used in a variety of industrial applications, despite the existence of more advanced nodes. This is because it offers a good compromise between cost, performance, and reliability: for the same yield, 28 nm lithography requires fewer processing steps, also offering a significantly lower wafer cost compared to more advanced technologies. For example, 16 nm FinFET production costs at least 50% more [97]. Furthermore, the 28 nm process is now mature and, after years of volume production, yield is high and consolidated, widely tested IP blocks are now available, reducing design and production risks. In non-consumer areas such as automotive, aerospace, and industrial applications, this technology node is still very competitive. Not surprisingly, the European Semiconductor Manufacturing Company (ESMC), a joint venture by TSMC, Bosch, Infineon, and NXP, is currently being established, which is building a semiconductor fab in Dresden, Germany [98] with the aim of producing 28 nm/22 nm CMOS chips, as well as 16 nm/26 nm FinFET, to meet the demand for semiconductors in Europe.

The main advantage for which this technology node was chosen in this research project is its promising robustness against ionizing radiation effects. Several recent studies have analyzed the properties of 28 nm CMOS transistors in high-radiation environments [99]. Irradiation campaigns have shown that the observed degradation is mainly due to the Total Ionizing Dose (TID) rather than displacement damage, i.e., a deformation of the silicon crystal structure due to collisions with high-energy particles, suggesting that with appropriate design countermeasures the node may be suitable for the realization of electronics for detectors in particle physics experiments [100].

2.1 Effects of Ionizing Radiation in CMOS Devices

The TID effect is caused by the accumulation of electric charges in dielectric materials. In MOSFET transistors, this charge accumulation occurs primarily in the gate oxide and in the isolation oxides such as shallow trench isolation (STI). As one can see in Figure 2.1, the isolation oxides are used to isolate the transistor channel from the substrate and from other devices, preventing unwanted leakage currents. This phenomenon is cumulative, so high doses lead to greater effects [1], [99].

When a MOSFET device is exposed to ionizing radiation, electron-hole pairs are generated within the insulating layers. Electrons, due to their high mobility, are quickly removed from the oxide structure, within a few picoseconds. Holes, on the other hand, are less mobile and tend to remain trapped within the dielectric, causing an accumulation of positive charges [2]. Alternatively, in some cases, holes may react with hydrogen-related defects present in the oxide, generating protons (H^+) that can diffuse towards the oxide-silicon interface and break the passivating hydrogen-silicon bonds, creating electrically active interface defects, also known as interface traps. These defects are negative in nMOSFETs and positive in pMOSFETs. The formation of interface traps is generally a slower process than the direct trapping of holes in the oxide substrate, but it has a

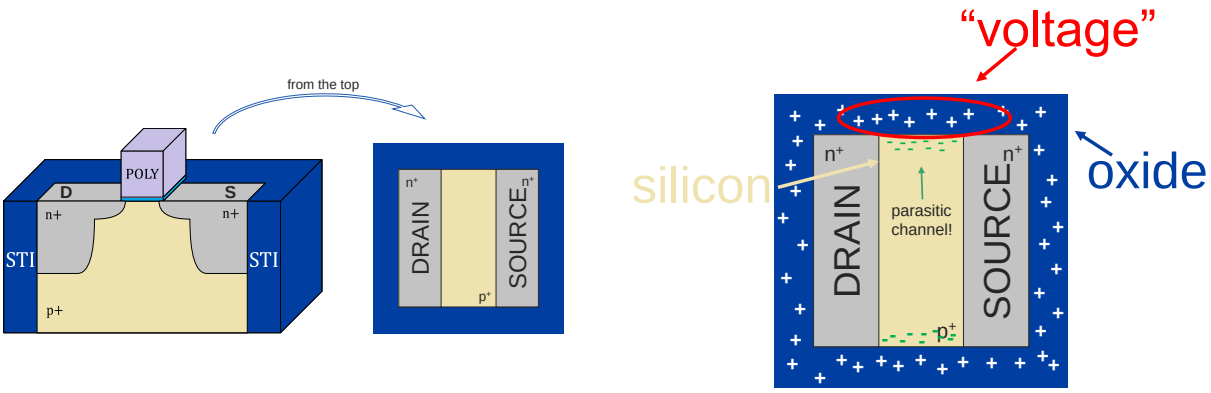


Figure 2.1: Representation of the Shallow Trench Isolation structure in a MOSFET and the formation of parasitic channels after irradiation. The accumulation of positive charge in the STI oxide due to TID attracts electrons at the channel edges, leading to the creation of lateral parasitic conduction paths, particularly in nMOS devices. Figure adapted from [101].

significant impact on transistor performance.

In 28 nm technology, as in previous nodes, the reduction of the gate oxide thickness has made transistors less sensitive to ionizing radiation [2]. However, the overall response to radiation is increasingly dominated by the presence of auxiliary oxides that are necessary at the structural and functional level [1]. In particular, shallow trench isolation oxides, and side spacers, which are used to improve transistor performance and reduce leakage losses, are particularly sensitive to ionizing radiation, much more so than gate oxides. The accumulation of charges in these oxides can lead to several deleterious effects that must be taken into account in the design of integrated circuits for high-radiation environments.

2.2 Influence of Device Geometry and Operating Conditions

In nMOSFETs, the positive charges trapped in the oxide cause a reduction in the threshold voltage, while the interface traps (which are negative) tend to increase it. The interaction of these two effects can produce non-monotonic behaviors and partial compensations, especially at low doses [102], [103].

In pMOSFETs, both the trapped charges and the interface traps are positive, thus synergistically contributing to increase the absolute value of the threshold voltage, shifting it towards more negative values. The shift can exceed 350 mV in narrow and long channel devices [103], [104]. In short-channel MOSFETs, the effect of halo implants in the channel helps mitigate the threshold shift, improving tolerance to TID [105]. As shown in Figure 2.2, halo implantation are lateral doping regions that help control the electrostatic potential in the channel, thus improving the transistor's performance and robustness against radiation effects. This is obtained thanks to the overlapping of the halo implants with the channel, which increases the lateral doping and mitigates the electrostatic effects of trapped charges. An higher doping concentration means that the number of carriers in the channel is higher, this making it less sensitive to the electrostatic potential variations induced by the trapped charges.

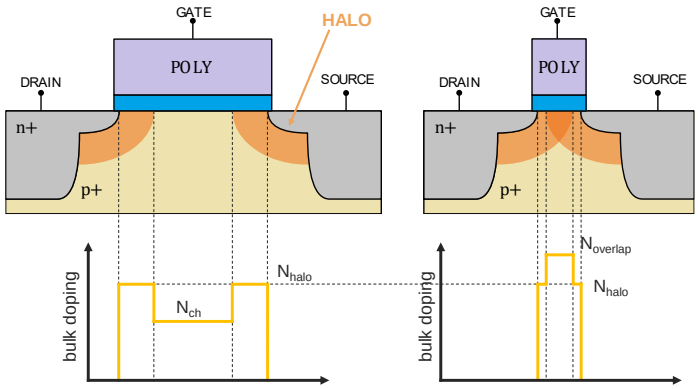


Figure 2.2: Representation of halo implants in short-channel MOSFETs. The halo implants are shown as the shaded regions around the channel, indicating the areas of lateral doping that help control the electrostatic potential. In the case of short channel devices, these implants overlaps, creating a stronger doping profile that improves the transistor's performance and robustness against radiation effects.

One of the most critical effects in 28 nm CMOS technology is the increase in drain leakage current, especially for n-channel MOSFETs [1], [103]. The positive charge accumulated in the STI oxides can induce lateral parasitic channels between source and drain, even with zero gate-to-source voltage, causing a drastic increase in leakage current by up to 3 orders of magnitude [106]. This effect is poorly controlled by the gate and becomes dominant at high doses. The increase depends on the channel length but is almost independent of the width [107]. Thermal annealing (especially at 100 °C) has proven effective in reducing the parasitic current, suggesting that accelerated tests at high doses may overestimate the severity of this phenomenon under real operating conditions, where annealing is continuous and doses are lower. In pMOSFETs, the increase in leakage current is generally negligible: the positive charge in the STI tends to accumulate electrons, inhibiting the formation of p-type parasitic channels [108]. A slight increase may still result from junction currents between drain and substrate.

The effects induced by total ionizing dose in MOSFET devices are strongly influenced by variables related both to device geometry and to operating conditions during irradiation, as well as environmental parameters such as temperature and dose rate. Narrow-channel MOSFETs are particularly sensitive to TID effects due to the so-called RINCE (Radiation-Induced Narrow Channel Effect), which is attributable to the accumulation of positive charge in the STI oxides at the channel edges [103]. These charges promote the formation of parasitic channels, significantly increasing the leakage current [102], [108]. Interestingly, in 28 nm technology, short-channel devices show greater tolerance to TID compared to long-channel ones, reversing the trend observed in previous nodes (e.g., 65 nm), where RISCE (Radiation-Induced Short Channel Effect) predominated [105]. This behavior is attributed to the presence of more aggressive and overlapping halo implants in short channels, which increase lateral doping and mitigate the electrostatic effects of trapped charges [105]. I/O transistors, characterized by thicker gate oxides and higher operating voltages, generally show greater vulnerability to TID compared to "core" devices, due to their higher susceptibility to charge trapping [1].

The influence of electrical bias during irradiation has been extensively studied in CMOS technologies, as it can affect the mechanisms of separation and trapping of electron-

hole pairs generated by radiation. In 28 nm technology, however, this effect is less pronounced than observed in previous technology nodes [1], [109]. In particular, the diode configuration, where $|V_{GS}| = |V_{DS}| = V_{DD}$, is often considered the most critical, as it imposes the maximum electric field across the oxides (gate and STI), promoting charge separation. In this condition, electrons are rapidly collected, while holes can remain trapped in the dielectrics, increasing the accumulation of positive charge and thus degrading device performance. Nevertheless, the differences between the various bias conditions applied during irradiation (e.g., "ON", "OFF", "diode") are less marked than in more mature technologies. The "OFF" configuration—where the device is off, typically with $V_{GS} = 0$ and $V_{DS} = V_{DD}$—tends to show the best tolerance to TID, since in the absence of strong electric fields the charge yield is reduced, thus limiting the number of carriers actually trapped in the dielectrics.

Temperature also plays an important role in the dynamics of degradation mechanisms induced by Total Ionizing Dose, as it directly affects both the generation and release of trapped charges in the dielectrics. At low temperatures, the effects of TID tend to be less pronounced in the short term, due to lower hole mobility and a reduced probability of thermal activation of defects. However, the reduction in temperature also slows down spontaneous annealing processes, i.e., the natural release of charges from shallow traps [99]. This can lead to greater residual sensitivity in the long term, especially in cases where the device is exposed to very low dose rates over time, as occurs in many space or medical applications. Conversely, thermal annealing at high temperatures significantly accelerates the recovery of electrical performance, promoting the release of charges trapped in sites with low activation energy. In particular, marked improvements are observed in leakage current and threshold voltage shift, helping to partially restore the original device behavior [1]. Generally, tests are performed at high dose rates, but real applications involve lower dose rates, which may allow greater annealing of the damage. Low dose rates could also increase the leakage current rise at low temperature [1].

2.3 Variability and Mismatch

The radiation response of CMOS technology is strongly dependent on the technological process and can show significant differences even within the same nominal node. CMOS devices fabricated with 28 nm technology but from different manufacturers, or even from different fabrication facilities of the same manufacturer, can exhibit markedly different behaviors when subjected to Total Ionizing Dose [1]. Moreover, pre-irradiation electrical performance can vary significantly, conditioning the measurement of relative degradation.

Even within a single production lot, or between nominally identical chips from the same wafer, significant device-to-device variability can be observed, even before irradiation. This variability is particularly evident in pMOSFETs, which are often more sensitive to local fluctuations in doping or interface formation. Figure 2.3 illustrates this device-to-device variability, showing the pre-irradiation I_D-V_G characteristics for 20 minimum size nMOS and pMOS transistors from two different chips [1]. The significant spread in the curves highlights the inherent mismatch present even before exposure to radiation.

Variability in MOS devices is a property strongly influenced by multiple technological and operational factors, which interact with each other and with radiation-induced effects, generating complex and sometimes counterintuitive behavior. Among the main elements that modulate variability, channel geometry plays a key role. In the most scaled technological nodes, small transistors, particularly those with minimum lengths and widths,

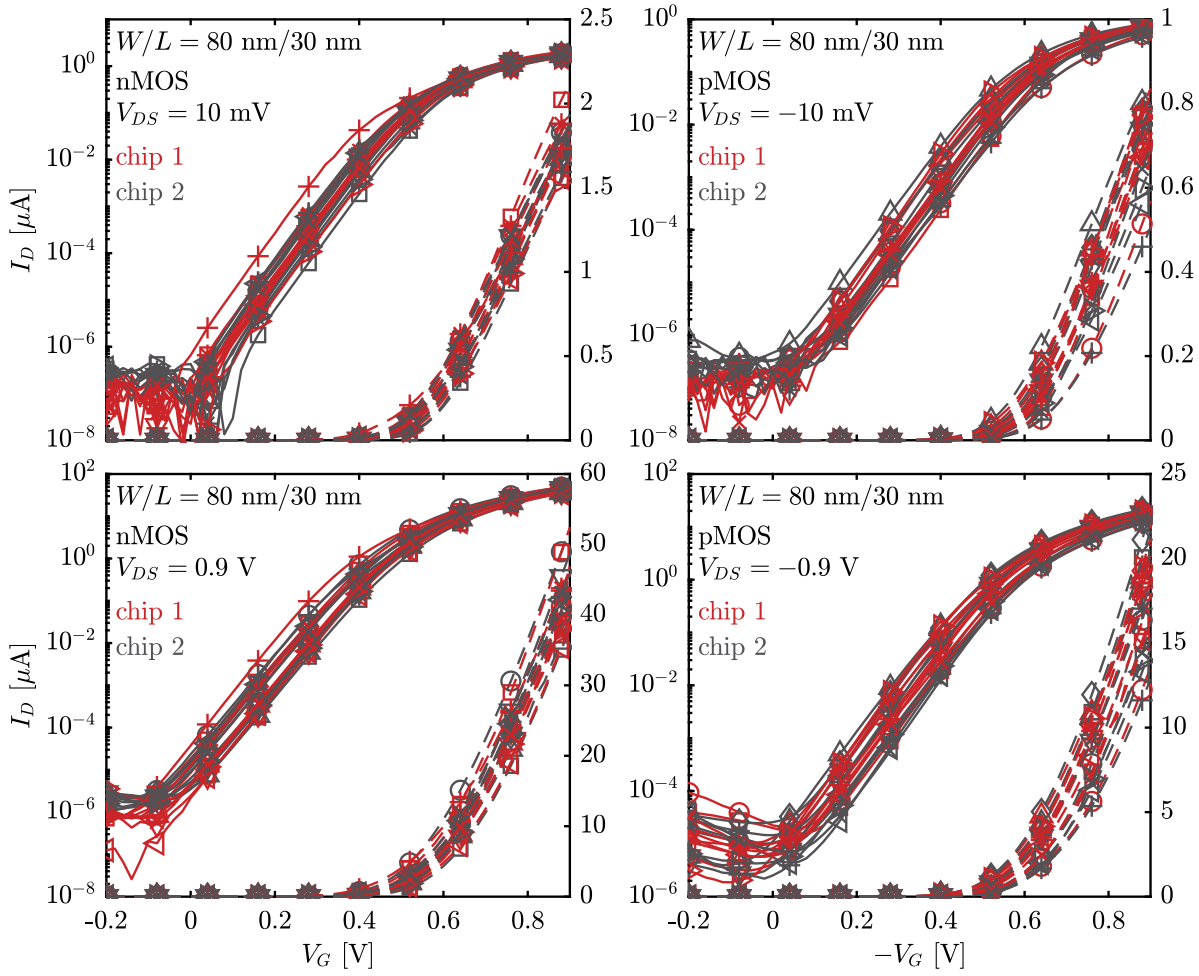


Figure 2.3: Pre-irradiation ID (VG) characteristics for 20 minimum size nMOS (left) and pMOS (right) transistors from 2 different chips in a LP flavor, measured in linear (top row) and saturation (bottom row) region. Solid lines report the curve in logarithmic scale while the dashed lines are for the characteristics in linear scale. The device-to-device variability is significant even before irradiation. [1]

exhibit greater dispersion of electrical characteristics among nominally identical devices. This effect is further amplified in the presence of radiation, which induces an increase in leakage current especially in smaller devices, where process tolerances and edge effects are more prominent.

The distinction between nMOSFET and pMOSFET has a significant impact on post-irradiation variability. In some processes, the response of pMOS to radiation is almost independent of channel width [1]. This behavior opens up the possibility of improving resistance to Total Ionizing Dose through a reduction in channel length, while maintaining a constant W/L ratio, without incurring an increase in variability. However, this strategy is not generalizable, as in other technological processes, the opposite behavior is observed, with significantly greater degradation as the width of the device decreases.

The bias conditions during irradiation represent another critical factor [103]. It has been observed that the "OFF" condition, i.e., with gate-to-source voltage set to zero, results in less degradation compared to other bias conditions, for both nMOSFET and

pMOSFET. This suggests a greater tolerance to TID when devices are not actively functioning during exposure. In more recent nodes, moreover, the differences between the various bias conditions tend to decrease, indicating a greater intrinsic robustness of modern processes compared to older ones.

Temperature and annealing phenomena play a crucial role in modulating variability after irradiation. High-temperature thermal annealing, in fact, can promote the recombination of trapped charges in the oxides and at the edges, thereby helping to reduce the leakage current induced by radiation. In many cases, this process allows the electrical parameters of the device, and in particular the variability, to return to values close to the original ones, mitigating the degrading effects of the absorbed dose [1].

Finally, the type of device also significantly influences variability. Transistors characterized by different threshold voltages (Low-VTH, High-VTH) or intended for different supply domains (Core vs I/O) can exhibit different behaviors regarding variability. For example, in devices from a tested manufacturer [1], Low-VTH and High-VTH transistors show a response similar to that of standard devices, with the exception of Low-VTH pMOSFETs characterized by narrow and long geometries, which undergo more pronounced degradation. Furthermore, transistors designed for I/O interfaces, due to the greater thickness of the gate oxide and higher operating voltages, are significantly more vulnerable to radiation than Core devices, resulting in an increase in both absolute degradation and variability among samples [1].

The mismatch associated with the device threshold voltage is another important figure of merit for analog circuits, especially in applications where precision is required. It can be defined as the standard deviation of the difference in the threshold voltage of two matched transistors, $\sigma(\Delta V_{TH})$ [89], [110], [111], [112]:

$$\sigma(\Delta V_{TH}) = A_{\Delta V_{TH}} \cdot \frac{1}{\sqrt{WL}} = k \cdot \frac{t_{ox}}{\epsilon_{ox}} \sqrt[4]{N} \cdot \frac{1}{\sqrt{WL}} \tag{2.2}$$

where k is a constant not depending on the scaling, t_{ox} and ϵ_{ox} are the gate oxide thickness and dielectric constant, respectively, and N is the density of dopants in the device channel. According to the equation 2.2, the dispersion is inversely proportional to the square root of the transistor gate area. It is worth noting that the ratio $\frac{t_{ox}}{\epsilon_{ox}}$ is expected to decrease with the scaling down process, whereas the parameter N increases, but at a slower rate. This means that for the same device size, scaling has in principle a beneficial impact on transistor threshold voltage matching.

Ionizing radiation tends to increase variability among devices, particularly regarding the saturation current $I_{DS,sat}$, where there is an increase in percentage variability. In fact, while showing a qualitatively similar response, the transistors exhibit different quantitative shifts in $I_{DS,sat}$ as TID increases. The normalized standard deviation of this variation increases with dose, indicating that relative dispersion worsens with irradiation.

2.4 Analog Performance and Noise in Irradiated Environments

Noise analysis on the selected 28 nm technology for the development of FALAPHEL and PiHEX front-end channels has highlighted an excess of white noise in minimum channel length pMOSFETs and an increase in the 1/f noise coefficient as channel length decreases. This suggests avoiding such configurations in low-noise designs. Conversely, minimum

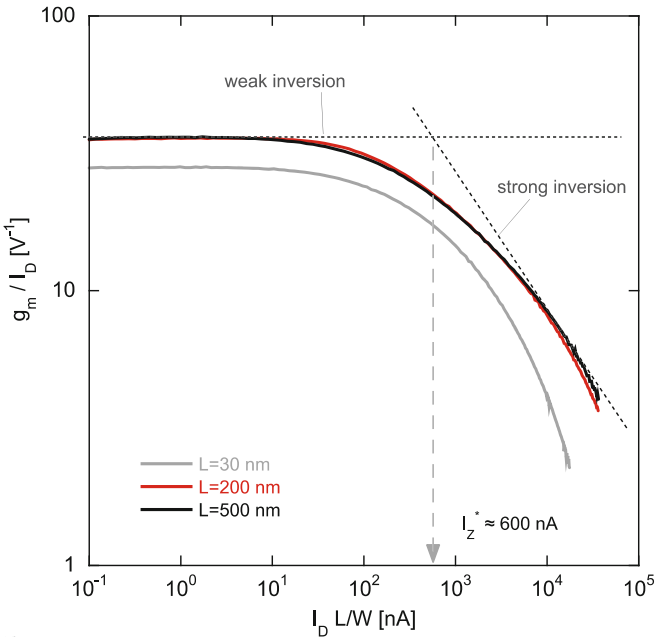


Figure 2.4: Simulated transconductance efficiency as a function of the normalized drain current for NMOS transistors in the 28 nm technology. The plot is relevant to n-channel devices featuring a width $W = 3\,\mu m$ and different channel lengths [89].

channel length nMOSFETs are preferable for noise minimization [4], [104]. Subsequent post-irradiation characterization showed excellent robustness to Total Ionizing Dose, confirming the technology's suitability for high-radiation environments. The degradations observed in analog parameters are contained: transconductance (gm) decreases by less than 10% in nMOSFETs and 20% in pMOSFETs, while maximum drive current drops by about 25% for nMOSFETs and approximately 35% for pMOSFETs [4], [104].

Regarding intrinsic gain, a slight increase is observed in nMOSFETs (more evident in long-channel devices) and a moderate reduction in pMOSFETs. This behavior is different from other variants of the 28 nm technology, probably due to differences in the manufacturing process [4], [104].

Noise characterization shows that channel thermal noise is little affected by TID. However, in nMOSFETs, 1/f noise increases at low doses (up to about 50 Mrad), especially at low current densities, due to the activation of parasitic channels induced by STI. This effect tends to decrease at higher doses, probably due to saturation or compensation effects. In pMOSFETs, on the other hand, the increase in 1/f noise is very limited [4], [104].

An important figure of merit for the design of analog circuits in nanoscale technologies is the so-called transconductance efficiency, defined as the ratio between the device transconductance g_m and the drain current I_D. Such an efficiency is strictly related to several analog parameters, including the intrinsic gain, and it is the basis of the g_m/I_D methodology for transistor sizing [89].

Figure 2.4 illustrates how transconductance efficiency (g_m/I_D) varies with normalized drain current for n-channel standard-threshold devices, all with a fixed width of $W = 3\,\mu m$ and different gate lengths L. The plot highlights two distinct regions: in the weak inversion region (at low normalized drain currents), the transconductance efficiency

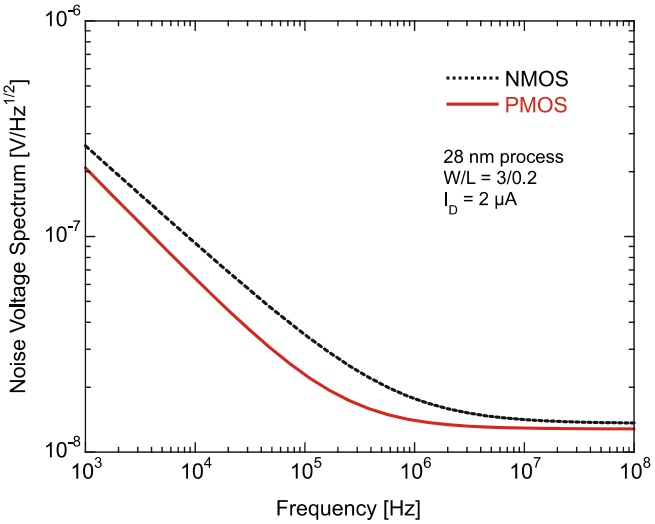


Figure 2.5: Simulated gate-referred noise voltage spectrum for NMOS and PMOS transistors. The devices feature a W/L of 3/0.2 with a drain current of 2 μA.

remains approximately constant; in the moderate and strong inversion regions (at higher drain currents), the transconductance efficiency decreases as the drain current increases. Notably, minimum channel length devices show lower transconductance efficiency, likely due to velocity saturation effects, while longer channel devices display nearly overlapping curves. The transition between weak and moderate inversion occurs at a normalized drain current I_Z^* of about 600 nA, which is relatively high for this technology [89]. This value is useful for calculating the Inversion Coefficient I_{C0}, defined as the ratio of normalized drain current to I_Z^*.

The maximum gain achievable from a single transistor, also known as intrinsic gain, is defined as the ratio between g_m and the output conductance g_{ds} of the device. It has been shown that the intrinsic gain of the 28 nm technology increases with the gate length and was found to be smaller than 20 V/V.

For what concerns the noise performance it is interesting to compare the noise figure of n-channel and p-channel devices. In less scaled processes, PMOS devices typically feature a lower $1/f$ noise, and this is generally ascribed to a buried channel conduction. In this case the probability of the channel carriers to interact with the gate oxide traps is lower [89], [113]. For the 28 nm process it is still true but to a limited extent, as shown in Figure 2.5, which shows similar simulated $1/f$ noise contributions for NMOS and PMOS devices, improving the design flexibility. In particular, the plot shows the noise voltage spectrum for n-channel and p-channel devices with a gate width of 3 µm and a length of 0.2 µm, biased at a drain current of 2 µA. This is compatible with the bias conditions and the sizing of the input transistor of charge sensitive amplifiers for the readout of hybrid pixel detectors in High Energy Physics applications, which determines the overall noise performance of the front-end circuit.

It is possible to conclude that the combination of robust analog performance, low noise, and excellent radiation tolerance makes 28 nm CMOS technology a promising choice for front-end circuits in high-radiation environments.

Chapter 3

Zero-deadtime front-end with autozeroed comparators

This chapter describes the front-end architecture developed within the *Falaphel* project, based on a flash-type analog-to-digital converter, optimized for zero dead-time operation in high event-rate environments.

Future High Energy Physics experiments, such as High Luminosity-Large Hadron Collider and Future Circular Collider, will require highly integrated readout systems capable of operating in extreme environments, with Total Ionizing Dose exceeding 1 Grad (SiO_2) and very high particle rates. In this context, the 28 nm CMOS technology represents a key node, thanks to the reduction in cell size, increased speed of digital logic, good noise performance, and improved radiation hardness compared to previous nodes such as the 65 nm CMOS.

The developed architecture exploits a flash ADC converter inside the pixel, enabling direct digitization of the signal synchronously and without dead-time. The system is specifically designed to operate in environments with 25 ns bunch crossing periods and non-negligible probability of consecutive hits.

3.1 The Charge Sensitive Amplifier

Figure 3.1 shows the schematic of the Charge Sensitive Amplifier integrated into the developed readout channel. In this configuration, the detector can be modelled as a current source I_D, delivering a charge Q_{in}, togheter with the capacitance C_D, which represents the detector capacitance, mainly given by its depletion region. The CSA consists of an inverting forward gain stage surrounded by a fast negative feedback including a capacitance C_F and an NMOS transistor M_F. The transistor M_F is biased to operate in the weak inversion (subthreshold) region, where its drain current is highly sensitive to the gate-to-source voltage. Weak inversion is chosen because it enables precise control of very small currents with low power consumption, which is essential for accurately discharging the feedback capacitor in low-noise, low-power analog front-end circuits. This configuration allows M_F to precisely regulate the discharge current of C_F, ensuring a controlled return-to-baseline for the CSA output signal. Additionally, a second slow negative feedback loop is included to compensate for the detector leakage current. Such a feedback includes the amplifier A_1, a low-pass filter featuring R_L and C_L, and the PMOS transistor M_L.

The gain stage investigated in this architecture is based on a regulated cascode configuration. Even though it is simple and compact, it is able to cope with the reduced

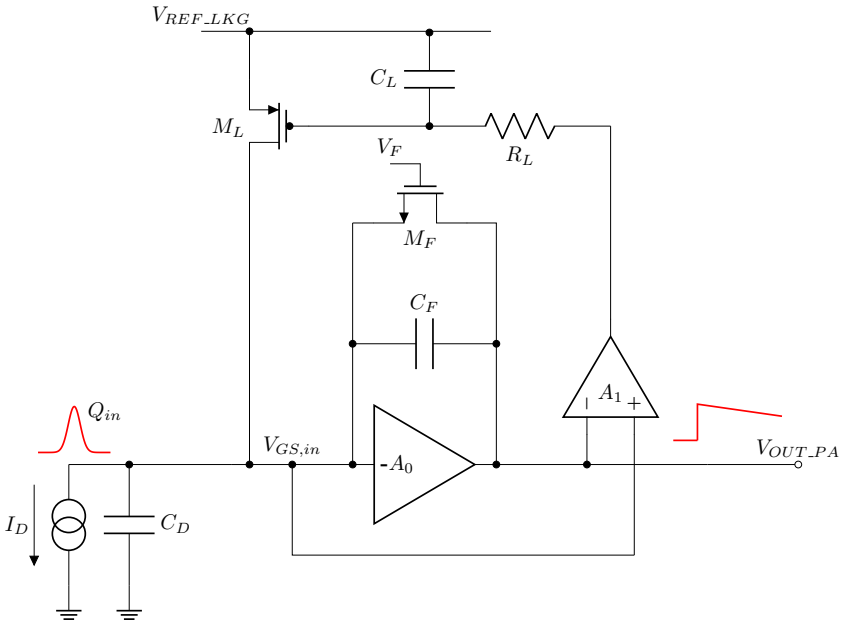


Figure 3.1: Schematic diagram of the charge sensitive amplifier used in the zero-deadtime front-end [114]. The gain stage is shown as an inverting stage.

core supply voltage of 0.9 V in the 28 nm CMOS process. This is challenging for analog gain stages because lower supply voltages reduce the available voltage headroom, making it more difficult to achieve high gain and proper transistor operation. Considering Figure 3.2, which illustrates the inverting gain stage composed of a regulated cascode configuration and a source follower buffer, in typical operating conditions (as from simulations), the main branch of the amplifier, including M_1 transistor, has been biased with a current of 2 µA, while the second branch, featuring M_5, has been biased with a current of 200 nA. These values are compatible with the low-power requirements typical of high-rate, pixelated detectors in HEP experiments. The low frequency gain refers to the amplifier voltage gain in the frequency range where the response is flat and unaffected by capacitive or frequency-dependent effects. This represents the maximum achievable gain before roll-off occurs. The low frequency gain, A_{LF}, of the regulated cascode can be calculated as:

$$A_{LF} \simeq -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}}\frac{g_{ds3}}{g_{m3}} + g_{ds4}} \tag{3.1}$$

with g_{mi} and g_{dsi} being respectively the transconductance and the drain-source conductance of the transistor M_i. The presence of the local feedback implemented by means of M_2 and M_3 allows to boost the gain of the structure. In fact the term $\frac{g_{ds3}}{g_{m3}}$, that is the inverse of the intrinsic gain of the transistor M_3, reduces the conductance seen at the output node of the regulated cascode, thus increasing the gain of the stage [89].

The input-referred noise power spectral density of the regulated cascode can be shown to be [89]:

$$\frac{\overline{de_{rc}^2}}{df} \simeq \frac{4kT\Gamma}{g_{m1}} \cdot \left(1 + \left(\frac{g_{ds3}}{g_{m3}}\frac{g_{ds1}}{g_{m1}}\right)^2 + \frac{g_{m1}}{g_{m3}}\left(\frac{g_{ds1}}{g_{m1}}\right)^2 + \frac{g_{m5}g_{m1}}{g_{m3}^2}\left(\frac{g_{ds1}}{g_{m1}}\right)^2 + \frac{g_{m4}}{g_{m1}}\right) \tag{3.2}$$

where k is the Boltzmann constant, T the absolute temperature and Γ parameter

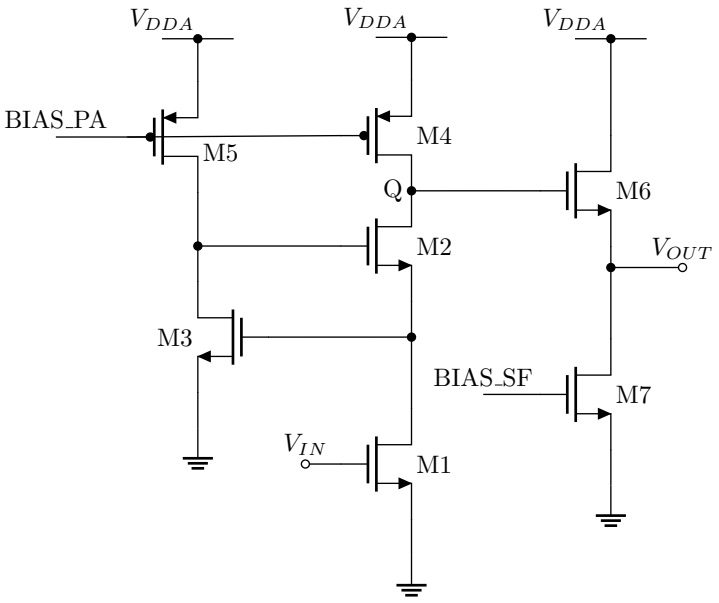


Figure 3.2: The inverting gain stage composed of a regulated cascode configuration and a source follower buffer [114].

depends on the operating region of the transistor. For MOSFETs, Γ is known as the thermal noise coefficient, with typical values ranging from 1/2 in weak inversion to 2/3 in strong inversion [89]. Equation 3.2 has been obtained under the assumption that transistors M_1 and M_2 are operated in weak inversion at the same current level. Under these conditions, they feature the same transconductance.

The regulated cascode design features a large number of transistors, which introduces more noise sources compared to simpler solutions; however, these additional sources do not have a significant impact on the overall noise. In fact, their contribution is attenuated by the intrinsic gain of the input transistor M_1. It is also worth noticing that the noise contribution from transistor M_2 is proportional to $\left(\frac{g_{ds3}}{g_{m3}}\frac{g_{ds1}}{g_{m1}}\right)^2$; the local feedback implemented by M_3 effectively reduces this term by increasing the effective output resistance, thereby attenuating and minimizing the impact of M_2 on the overall noise. The regulated cascode design thus allows to achieve a good compromise between noise and gain, with low power consumption. With respect to simpler solutions, pixel-to-pixel cross-talk is minimized because the higher gain of this configuration increases the amplitude of the main signal compared to parasitic signals from neighboring pixels, thus making the effect of cross-talk less significant relative to the desired signal [89].

The regulated cascode is connected to a source follower, in order to buffer the output signal and to provide a low output impedance for driving subsequent stages. Therefore, considering simplistically a unitary gain for the source follower, the low frequency gain A_0 of the stage can be described by:

$$A_0 = -g_{m1}\left(\left((1 + g_{m3}(r_{O3} \parallel r_{O5})) \cdot g_{m2} r_{O2} r_{O1}\right) \parallel r_{O4}\right), \tag{3.3}$$

where g_{mi} and r_{Oi} denote, respectively, the transconductance and the output resistance of each transistor M_i in the gain stage. The parallel notation ($r_{O3} \parallel r_{O5}$) indicates the combined output resistance of transistors M_3 and M_5, while each term reflects the contribution of the respective transistor to the overall gain: g_{m1} is the input stage

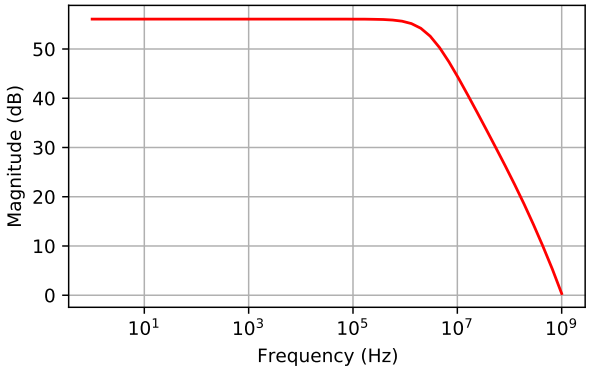


Figure 3.3: The simulated open loop gain of the CSA gain stage.

transconductance, g_{m3} and r_{O3} relate to the local feedback, g_{m2}, r_{O2}, and r_{O1} describe the cascode chain, and r_{O4} sets the dominant output resistance.

In a first approximation, and by neglecting the smaller contributions from other transistors and feedback paths, Equation 3.3 can be reduced to:

$$A_0 \approx -g_{m1} r_{O4} \tag{3.4}$$

It is reasonable to study the transfer function $F(s)$ of the gain stage with a first dominant pole approximation:

$$F(s) = \frac{A_0}{1 + s\tau}, \tag{3.5}$$

where A_0 is the gain of the inverting amplifier given by (3.4) and $\tau = \frac{1}{R_{OUT} C_{EQ}}$ is the time constant defined by the output resistance, R_{OUT}, of the gain stage and the capacitance C_{EQ}.

$$R_{OUT} \sim r_{O4} \tag{3.6}$$

is approximated by the output resistance of the regulated cascode stage whereas

$$C_{EQ} \sim C_{DB2} + C_{GD6} + C_{GD4} + C_{GD2} \tag{3.7}$$

is the equivalent capacitance given by the gate-drain and gate-bulk capacitors of the transistors connected to the node Q in Figure 3.2. From simulations (Figure 3.3) the dominant pole occurs at 2 MHz, whereas the DC gain is close to 58 dB. Simulations were carried for the typical-typical (TT) corner for a temperature of $-20\,^{\circ}\mathrm{C}$ which corresponds to the operating conditions of the electronics in a cooled-down detector.

When a signal is delivered by the detector, the CSA output is a step signal with an amplitude equal to Q_{in}/C_F, where the amplitude is determined by the ratio of the input charge (Q_{in}) to the feedback capacitance (C_F). This relationship arises because the CSA integrates the input current pulse onto the feedback capacitor, resulting in a voltage step proportional to the delivered charge. This expression assumes ideal charge collection and negligible parasitic effects, providing a simplified context for understanding the CSA response. Upon signal arrival, the transistor M_F, whose source potential is fixed by the gate-to-source voltage of the CSA transistor M_1, turns on operating in weak inversion region with a subthreshold drain current, I_D, which can be modelled by means of:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{V_T}\right) \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right], \tag{3.8}$$

with I_0 being a process-dependent parameter, typically defined as $I_0 = 2n\mu C_{ox}\left(\frac{kT}{q}\right)^2$, where n is the subthreshold slope factor, μ is the carrier mobility, and C_{ox} is the gate oxide capacitance per unit area; W/L is the aspect ratio of M_F, V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltages, V_{TH} is the threshold voltage of the transistor, and V_T is the thermal voltage.

The feedback capacitance discharge current, I_D, is thus given by:

$$I_D = K \cdot \left(1 - \exp\left(-\frac{V_{OUT}}{V_T}\right)\right), \tag{3.9}$$

where $K = I_0 \frac{W}{L} \exp\left(\frac{V_{GS}-V_{TH}}{V_T}\right)$, which acts as the pre-factor for the subthreshold current in the weak inversion region. If a charge Q_{in} is delivered by the detector at time $t = 0$, the CSA return-to-baseline is thus described by the solution of this system of equations:

$$\begin{cases} I_D + C_F \cdot \frac{dV_{OUT}(t)}{dt} = 0 \\ V_{OUT}(0^+) = Q_{in}/C_F \end{cases} . \tag{3.10}$$

Therefore, given a charge Q_{in} at its input, the CSA output signal, $V_{OUT}(t)$, can be approximated by a voltage step of amplitude Q_{in}/C_F followed by a linear return-to-baseline with a slope of $\sim -I_D/C_F$.

As mentioned above, the CSA features a second, slower, negative feedback loop. It is conceived for compensating the leakage current that may come from the sensor. The negative feedback around the gain stage stabilizes the CSA output voltage by referencing it to the gate-to-source voltage of the input transistor M_1, ensuring consistent operating conditions. If a detector leakage current is present, the A_1 output tends to move, resulting in a baseline shift. Nonetheless, the gate of the M_L transistor is driven in such a way to carry the whole leakage current, avoiding the saturation of the CSA. The low-pass $R_L - C_L$ filter acts to filter out high-frequency noise and stabilizes the DC operating point of the M_L transistor.

Finally, the CSA current consumption per channel has been simulated to be $\sim 3\mu A$ under typical bias settings (main branch current of 2 µA, second branch current of 200 nA and the rest consumed by the source follower) and at a temperature of 27 °C.

3.2 The Comparator

The CSA output is AC-coupled to three comparators (implementing a 2-bit flash ADC) via coupling capacitors, which block DC offsets and allow only the signal variations to pass; no additional DC restoration circuit is implemented, as baseline restoration is instead achieved by the auto-zeroing mechanism within the comparators themselves, which periodically samples and cancels offset to maintain a stable operating baseline. Figure 3.4 shows the structure of the clocked, auto-zeroed comparator. Auto-zeroing is employed in this comparator to periodically sample and cancel its own offset voltage, significantly reducing offset and low-frequency noise, which is crucial for achieving precise and uniform threshold levels across all channels in a matrix of front-end circuits.

The comparator consists of two cascaded common-source amplifiers followed by two inverters. Every comparator requires two input signals: the CSA output signal, which can be approximated as a step signal with a long recovery time, and a threshold signal generated as a negative voltage step, as qualitatively highlighted in Figure 3.4.

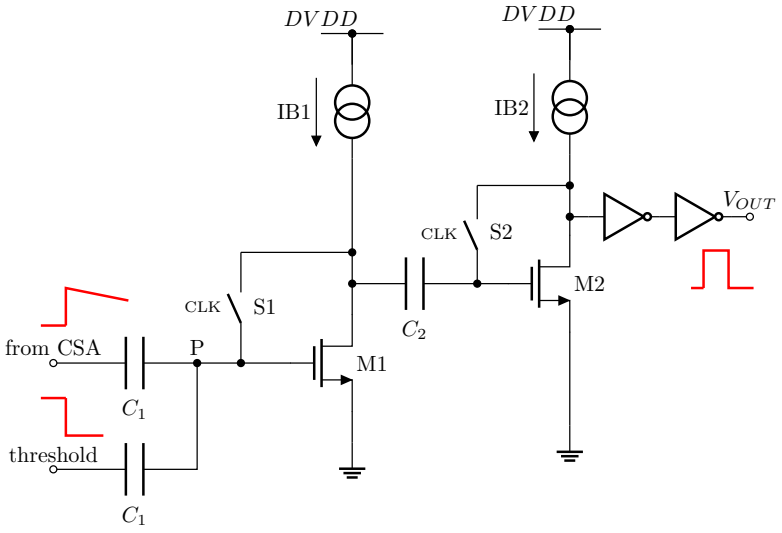


Figure 3.4: Schematic simplified diagram of the clocked, auto-zeroed comparator stage.

The threshold signal is produced by a dedicated on-chip circuit that generates a negative step toggling from two programmable references. The use of a negative voltage step for the threshold signal ensures that the comparator can reliably detect positive-going signals from the CSA, as the comparison is made between the rising edge of the CSA output and a falling-edge reference.

The threshold signal serves as a reference level for discrimination and is synchronized with the falling edge of the 40 MHz clock of the system, controlling S_1 and S_2 switches connected between gate and drain terminals of M_1 and M_2. In this system, it is assumed that the CSA output signal and the threshold signal are synchronous, meaning they are both referenced to the same clock edge. This condition is typically met in synchronous machines, ensuring that the comparator evaluates the CSA output against the threshold in a well-defined and repeatable timing window.

Both input signals are injected at the gate of the input transistor M_1, and the clock controls the opening and closing of the switches S_1 and S_2. The operation of this block consists of two phases:

1. Reset: switches S_1 and S_2 are closed. During this phase, offsets related to M_1 and M_2 transistors are stored respectively in the C_1 and C_2 capacitors.

2. Active comparison between the inputs (CSA output and threshold signal): switches S_1 and S_2 are open.

During phase 2) the node P behaves like a summing node. If the CSA signal amplitude is larger than the threshold, then a positive going signal is present at the M_1 gate, amplified by two common source stages and fed to output inverters that consolidate the output logic levels.

The schematic shown in Figure 3.5 includes a number of parasitics and additional components useful for the analytical analysis of the comparator performance. In Figure 3.6 it is shown the operation of the comparator with the time diagram of the involved signals. In the diagram, the signals are step signals with opposite polarities, applied to the gate of transistor M_1 via the capacitors C_1 at the falling edge of the clock. The signal from the CSA converts the charge delivered by the sensor at time t_{INJ} into a voltage at the

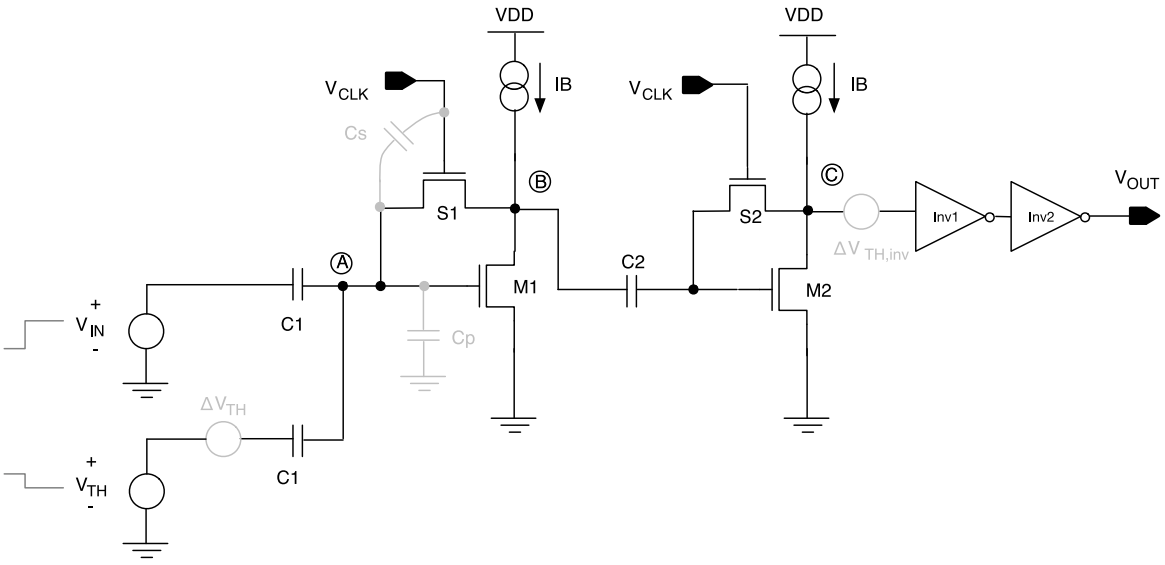


Figure 3.5: Schematic diagram of the synchronous comparator. Devices in light gray are parasitic/additional components that support the voltage dispersion analysis (i.e., the study of threshold variations and mismatch effects among channels) [115].

comparator input. The threshold signal is periodic with the same frequency of the clock signal, and it represents the global threshold, common to all the front-ends integrated in a multichannel readout system. As mentioned before, if the amplitude of the CSA output signal is larger than the threshold, then a positive going signal is present at node A. If the overall gain of the stages making up the comparator is large enough, then V_{out} saturates for small differences between the amplitude of the signal from the CSA and the threshold. In the timing diagram (Figure 3.6) the comparator get reset at the time t_{RESET}, which is the rising edge of the clock signal.

It is interesting to study the shape of the signal, V_A, at node A, which primarily sets a constraint for the maximum operating frequency of the clock signal. In particular, it can be shown [115], that for $t_{INJ}^{-} < t < t_{RESET}^{-}$:

$$V_A(t) \simeq U(t - t_{INJ}) \cdot \left[\frac{C_1}{C_T} \left(V_{CSA}^* - V_{TH}^* \right) - \frac{C_S}{C_T} V_{CLK}^* \right] - \frac{I_{OFF}}{C_T} \left(t - t_{INJ} \right) \tag{3.11}$$

where $U(t)$ is the Heaviside function, I_{OFF} the off-current of the NMOS switch S_1 and V_i^* is the amplitude of the signal V_i. The capacitance C_T is given by

Each term in this equation has a specific physical meaning:

- $\frac{C_1}{C_T} \left(V_{CSA}^* - V_{TH}^* \right)$: This term represents the contribution of the difference between the CSA output and the threshold voltage, scaled by the ratio of the coupling capacitance C_1 to the total capacitance C_T at node A. It determines how much of the input signal is transferred to node A.

- $-\frac{C_S}{C_T} V_{CLK}^*$: This term accounts for the clock feedthrough effect, where C_S is the gate-to-drain capacitance of the switch S_1 and V_{CLK}^* is the clock amplitude. It describes how the clock signal can couple into node A through parasitic capacitance.

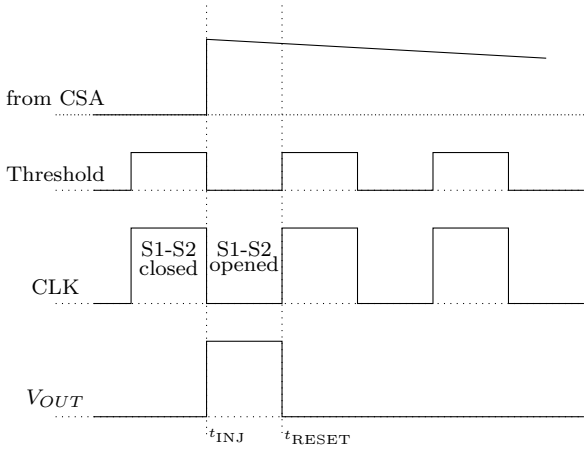


Figure 3.6: Operation of the comparator with the time diagram of the involved signals. It is shown the instant when an injection signal greater than the threshold voltage is detected.

- $-\frac{I_{OFF}}{C_T}(t - t_{INJ})$: This term models the linear voltage drop at node A due to the off-current I_{OFF} of the NMOS switch S_1, divided by the total capacitance C_T. It represents the slow discharge of node A over time after the injection event.

Here, C_T is the total capacitance at node A, including all relevant parasitic and coupling capacitances.

$$C_T = 2C_1 + C_P + C_S \tag{3.12}$$

with C_S being the gate-to-drain capacitance of S_1 and C_P the one shunting the gate of the transistor M_1. Hence, assuming $C_1 \gg C_P + C_S$, and neglecting the contribution, $(C_S/C_T)\, V^*_{CLK}$, associated with clock feedthrough in S_1, a step signal with amplitude close to $\frac{1}{2}\,(V^*_{IN} - V^*_{TH})$ is generated at time $t = t_{INJ}$. This assumption is justified because, in the design, C_1 is a MoM capacitance with a value of 15 fF, while parasitic capacitances C_P and C_S are typically much smaller, with at least a decade of difference, ensuring that their effect on the total capacitance is negligible.

As mentioned, at time $t = t_{RESET}$ the comparator gets reset and the voltage at node A, assuming $C_1 = C_2 = C_{IN}$, returns to its baseline value according to the following equation.

$$V_A(t) \simeq V^*_A \cdot \cosh\left(\frac{\sqrt{2}g_m}{C_{IN}}(t - t_{RESET})\right) \cdot e^{-(t-t_{RESET})\left(\frac{2g_m}{C_{IN}}\right)} \tag{3.13}$$

with $V^*_A = V_A(t^-_{RESET})$ and g_m the transconductance of equally sized transistors M_1 and M_2, biased with the same current I_B. Here, t^-_{RESET} denotes the instant immediately before the reset event at t_{RESET}, so V^*_A is the value of V_A just prior to the reset phase.

This functional form arises from the solution of the second-order differential equation describing the discharge of the capacitive nodes through the transconductance stages during the reset phase. The "cosh" term reflects the underdamped response of the cascaded amplifier-capacitor system, while the exponential decay represents the dominant return-to-baseline behavior governed by the transconductance (g_m) and the total input capacitance (C_{IN}). This combination captures both the fast initial response and the slower exponential settling of the node voltage.

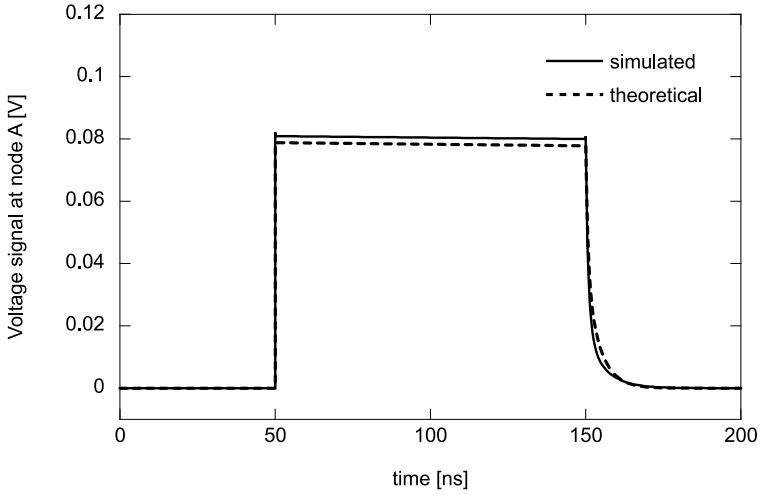


Figure 3.7: Transient signal at node A during the reset and comparison phases.

Figure 3.7 shows a comparison of the voltage at node A over time, as predicted by the theoretical result obtained by combining Equations 3.11 and 3.13, and as obtained from a SPICE simulation of the implemented circuit. In the simulation, an ideal CSA provides a step signal with an amplitude of 200 mV at the comparator input, whereas the threshold signal amplitude is set to 25 mV. By assuming for the CSA a charge sensitivity of 25 mV/ke$^-$, this translates to an input signal of 8000 electrons, with a threshold set to 1000 electrons. The supply voltage in the simulation is set to 0.9 V whereas I_B (namely the bias current for the two stages making up the comparator) is set to 1 µA. As described by Equation 3.13, the return-to-baseline of the signal at node A depends on both the transconductance of transistors M_1 and M_2, as well as the C_{IN} capacitance value. Proper operation of the comparator is ensured if the following condition on the clock frequency is satisfied:

$$\frac{g_m}{C_{IN}} \gg 2f_{CLK} \tag{3.14}$$

In the design of a multichannel system for the readout of pixelated sensors threshold dispersion minimization is a key point. Random variations of process and geometrical device parameters may lead to non uniformities in the response of nominally identical readout channels operated with the same threshold. With reference to Figure 3.5, this effect can be modelled by means of a voltage source, ΔV_{TH}, which accounts for channel-to-channel deviations of the comparator threshold, and which adds to the global comparator threshold amplitude V_{TH}. Here, V_{TH} always refers to the comparator threshold voltage amplitude. To avoid confusion, the inverter threshold voltage is denoted as $V_{\mathrm{TH,inv}}$ throughout the following analysis. The term V_{TH} is therefore treated as a random variable with standard deviation $\sigma_{V_{TH}}$, commonly referred to as threshold dispersion.

For the proposed comparator, it can be shown that

$$\sigma^2(V_{TH}) \simeq (2V^*_{TH})^2 \left[\frac{1}{2} \cdot \frac{\sigma^2(\Delta C_1)}{C_1^2}\right] + (V^*_{CLK})^2 \left[\frac{\sigma^2(\Delta C_S)}{C_1^2}\right] + 4 \cdot \frac{\sigma^2(\Delta V_{\mathrm{TH,inv}})}{A_G^2} \tag{3.15}$$

where ΔC_i represents the deviation from the nominal value capacitor C_i and A_G is the voltage gain of the cascade of the two common-source amplifier stages in the comparator,

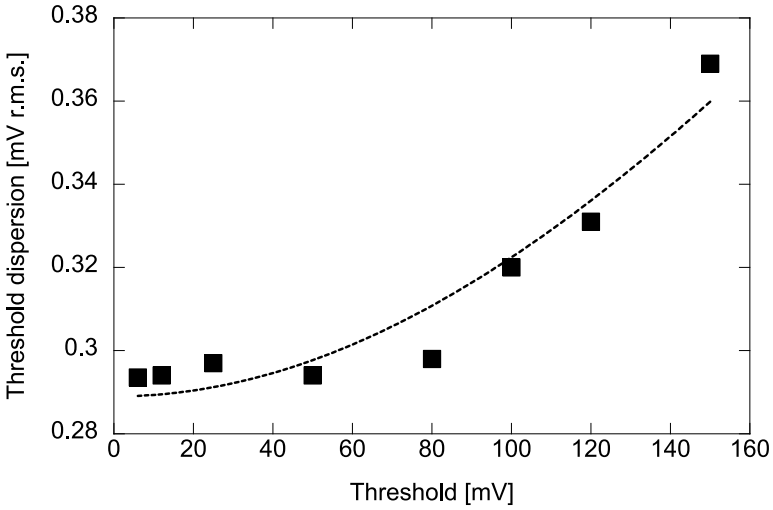


Figure 3.8: Simulated threshold dispersion as a function of the threshold voltage. Each point in the plot has been obtained from a set of 500 Monte-Carlo simulations of the comparator efficiency curve [115].

specifically during the comparison phase when switches S_1 and S_2 are open. This definition of A_G refers to the effective signal amplification provided by the comparator during active comparison, and should be distinguished from other gain definitions (such as the open-loop gain of the CSA or buffer stages) used elsewhere in this document. Hence, according to Equation 3.15, there are three main contributions to the threshold dispersion. The first one, which is threshold-dependent, is related to mismatch of the capacitors C_1, while the second and third ones are associated with clock feedthrough and mismatch of the first inverter threshold. $V_{TH,inv}$ respectively.

Figure 3.8 shows the simulated threshold dispersion (solid squares), as a function of the threshold voltage. The figure also reports the data fit (dashed line) as obtained with the following fitting function, derived from Equation 3.15, having p_0 and p_1 as fitting parameters:

$$\sigma(\Delta V_{TH}) = \sqrt{\left(2V_{TH}^{*}\right)^2 \frac{1}{2} p_0^2 + p_1^2} \tag{3.16}$$

the parameter p_0 was found to be equal to $1.01 \cdot 10^{-3}$, in fairly good agreement with simulated mismatch, $\frac{\sigma(\Delta C_1)}{C_1}$, of the capacitor C_1, close to 0.1%. Assuming low threshold operation, as in the case of front-end channels for pixel readout and a charge sensitivity of about $25\,\mathrm{mV/ke^-}$, the simulated threshold dispersion of $290\,\mu\mathrm{V}$ r.m.s. corresponds to approximately 12 electrons r.m.s., calculated by dividing the voltage dispersion by the charge sensitivity.

Up to now the discussion has been focused on an ideal CSA response behaving like a step signal. However, in a real scenario, the CSA response may exhibit a more complex behavior due to various non-idealities, such as finite rise and fall times, noise, and distortion. In order to account for these effects, the CSA output signal can be modelled with a more realistic shape as follows:

$$V_{out,CSA} = U(t)\left[V_{MAX} \cdot \left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}\right)\right] \tag{3.17}$$

with V_{MAX} proportional to the charge delivered by the sensor, $\tau_1 = 5\,\mu\mathrm{s}$, accounting

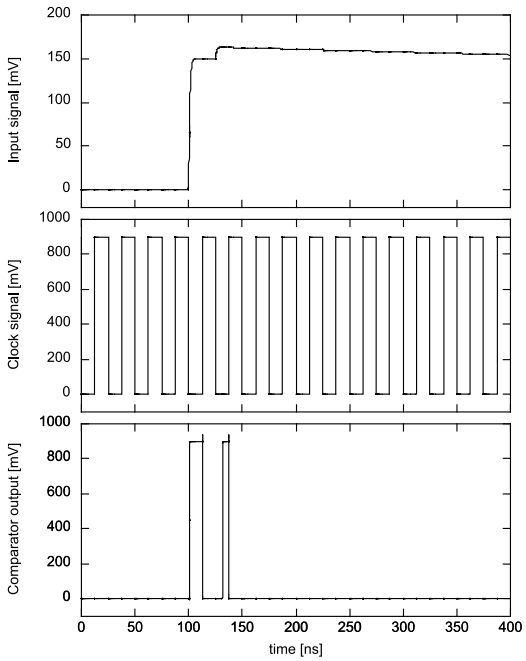


Figure 3.9: Simulated comparator input (CSA output), comparator output, and clock signals as a function of time in the presence of two consecutive hits. The first hit is generated at time $t = 100\,\text{ns}$, the second one at $t = 125\,\text{ns}$. The plot also shows the clock signal controlling S_1 and S_2 switches.

for the CSA time to return-to-baseline, and $\tau_2 = 1\,\text{ns}$ shaping the rising edge of the signal (as from circuit simulations).

Figure 3.9 shows the simulation of the comparator output in response to a charge signal of 6000 electrons delivered by the sensor at time $t = 100\,\text{ns}$, followed in the subsequent bunch crossing period by a signal slightly exceeding 500 electrons, corresponding to the threshold level. A frequency of 40 MHz is used for the clock signal (i.e. the bunch crossing frequency at the LHC). Table 3.1 reports additional details related to the simulated circuit. The simulation demonstrates the zero dead-time capability of the front-end by showing two distinct comparator output pulses for these consecutive hits, indicating that both events are successfully detected without loss. The plot also reports the V_{IN} signal generated by the CSA and the comparator clock signal. It is worth noting that a large CSA signal implies a large overdrive (difference between CSA amplitude and threshold signal amplitude), with a faster comparator response. On the other hand, CSA signals with an amplitude close to the threshold level result in a reduced overdrive at the comparator input, which causes a slower and delayed comparator response; as a consequence, the output pulse is shorter because the comparator takes longer to switch and the output remains high for a reduced duration. Under typical operating conditions, the minimum overdrive—defined as the smallest voltage difference between the CSA output and the threshold signal that can reliably trigger the subsequent logic at the comparator output—is close to 4 mV from circuit simulations. This minimum overdrive represents the lowest signal amplitude above the threshold at which the comparator can consistently register a hit, ensuring that small fluctuations or noise do not cause false triggers or missed detections. A sufficient overdrive is crucial for robust operation, as it guarantees that the comparator output transitions cleanly and within the required timing constraints, even

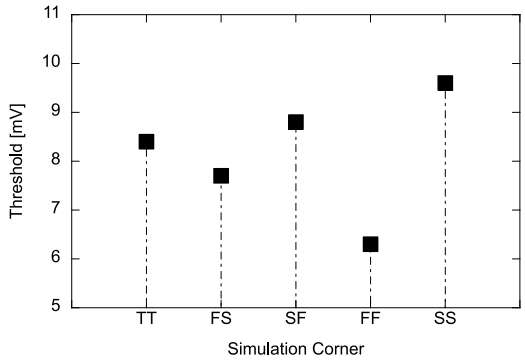


Figure 3.10: Simulated threshold, corresponding to a charge threshold of 500 electrons, in different corners [115].

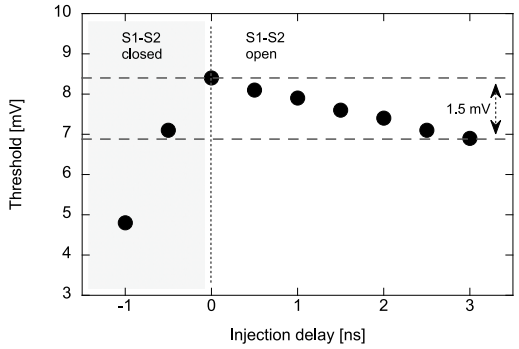


Figure 3.11: Simulated threshold corresponding to a charge threshold of 500 electrons as a function of the injection delay [115].

in the presence of process variations and electronic noise.

Figure 3.10 shows the threshold (in millivolts) needed to fire the discriminator in different simulation corners (TT, FS, SF, FF, and SS, with a temperature set to 27 °C), when an input signal with a fixed amplitude of 12.5 mV (i.e., 500 electrons) is provided by the CSA. The threshold was found to be quite stable across corners, with variations lying in a range not exceeding 3.3 mV.

The timing sensitivity of the comparator has been evaluated by purposely introducing a delay between the voltage step of the CSA output (generated at time $t = t_{INJ}$, referred to as injection time) and the clock signal falling edge. This delay simulates the effects of clock skew and uncertainties in the precise timing of charge arrival from the sensor, both of which can impact the comparator's ability to correctly register hits. As shown in Figure 3.11 (for simulation) and later on this chapter in Figure 3.29 (for measurement), variations in the relative timing between the CSA signal and the clock can lead to changes in the effective threshold and detection efficiency, highlighting the importance of synchronization for optimal comparator performance. As a reference, the full-size pixel readout chips developed by the CERN RD53 collaboration for the high-luminosity upgrades of the CMS and ATLAS experiments at the LHC, features a clock skew not exceeding 1 ns [116].

For the comparator described here, it is worth noticing that the threshold signal can be reasonably assumed to be in phase with the clock. This is because the threshold can easily be locally generated with a couple of switches controlled by V_{CLK}, starting from two DC levels. Figure 3.11 shows the behavior of the threshold, in millivolt, corresponding

Component	Size / Value	Notes
M_1	1/0.25	Ultra-low threshold voltage
M_2	1/0.25	Ultra-low threshold voltage
S_1	1/0.25	Ultra-low threshold voltage
S_2	1/0.25	Ultra-low threshold voltage
I_B	1 µA	PMOS current mirror
C_1	16 fF	MoM capacitor
C_2	35 fF	MoM capacitor
INV_1	-	Ultra-high threshold voltage NMOS
	-	Ultra-high threshold voltage PMOS
INV_2	-	Ultra-high threshold voltage NMOS
	-	Ultra-high threshold voltage PMOS

Table 3.1: Details of the simulated circuit. Transistor sizes are in μm (W/L) [115].

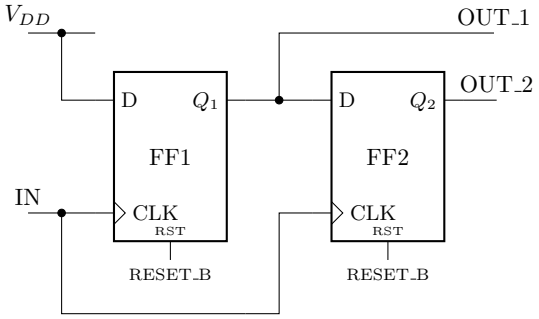


Figure 3.12: The digital double-hit detection stage.

to a charge signal of 500 electrons, as a function of the injection delay, illustrating how the effective threshold changes when the timing between the CSA output and the clock signal is varied. For positive delays, that is for t_{INJ} occurring later with respect to the clock falling edge, the threshold monotonically decreases with a maximum variation found to be close to 1.5 mV (corresponding to 60 electrons) for a delay of 3 ns. On the other hand, the decrease in the threshold is much more pronounced for negative delays, which can significantly increase the likelihood of missed detections or unreliable comparator operation. For this reason, and for optimum operation of the comparator, negative delays should be avoided. In practical terms, this means that the system timing must be designed to ensure that the charge injection always occurs after or synchronously with the threshold signal, thereby guaranteeing reliable hit detection and minimizing the risk of missed events.

3.3 Double hit detection system

This front-end channel is designed for environments with very high event rates and a significant probability of hits in adjacent bunch crossings. In order to test this zero dead-time front-end, a simple read-out block based on a double flip-flop structure has been integrated, providing the capability to store events from two subsequent bunch crossing periods of 25 ns. Thus, following the comparator, the block shown in Figure 3.12 has been integrated. This circuit implements the double hit detection mechanism using a double

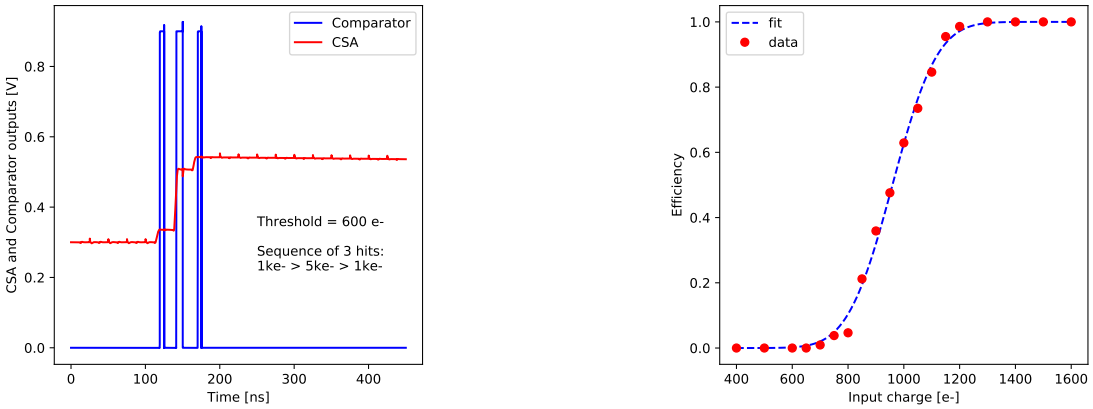


Figure 3.13: (Left) CSA output signal and comparator output response to three sequential charges with threshold set to $600e^-$. (Right) Simulation results of the s-curve for a detector capacitance of 50 fF at a temperature of 27°C, as obtained from transient noise simulations.

flip-flop approach. The two logical output signals, OUT_1 and OUT_2, are needed to independently record and distinguish hits occurring in two consecutive bunch crossing periods, ensuring detection of both events even if two hits arrive in consecutive bunch crossings.

It receives a signal from the comparator as input (IN) and reads a global reset signal (RESET_B). The behavior of this block is straightforward and is described by a four-steps flow:

1. Before signal arrival the input signal is low. The first flip-flop FF1 does not change its output signal Q1. The output signals OUT_1 and OUT_2 are both low level.

2. Upon first hit detection, CSA signal exceed threshold, and the input signal toggles to high for the first time. FF1 changes its output state. The Q1 output signal is high, then the second flip-flop FF2 is ready to change its state. The output signals are OUT_1 at high level and OUT_2 at low level.

3. If a second hit is detected, the input signal toggles high for the second time. Now also FF2 changes its state. So the output signals OUT_1 and OUT_2 are both to high level.

4. Finally, after data readout, the reset signal is provided to the circuit. Both the output signals of the flip-flops are reset. The output signals OUT_1 and OUT_2 are again both to low level.

The output signals OUT_1 and OUT_2 are connected to a tristate inverter, which allows the output of the channel to be decoupled from the output bus. This is useful for testing purposes, as it allows reading the output of a single channel without interference from other channels in the matrix.

3.4 Front-end simulation results

The flash-FE behavior has been simulated under typical conditions (temperature of 27 °C and detector capacitance of 50 fF), and the main results—including Equivalent Noise

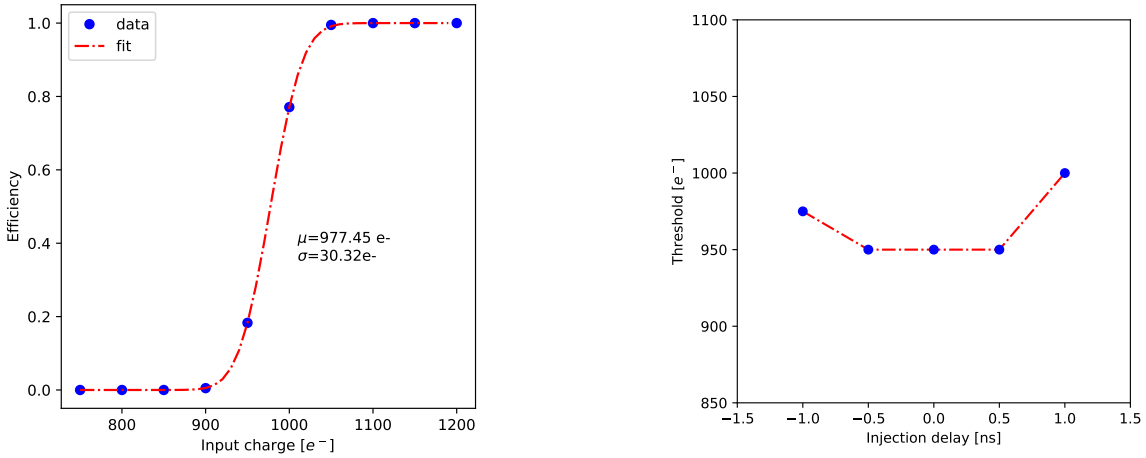


Figure 3.14: (Left) Simulation results of the s-curve obtained from 200 Monte Carlo runs with a threshold set to $600e^-$. (Right) Threshold behavior against injection delay, where the delay is referred to the time interval between the clock of the comparator and the injection signal given as input to the channel.

Charge, threshold dispersion, and zero dead-time operation—are summarized in Figures 3.13 and 3.14. The Equivalent Noise Charge, evaluated at the CSA output for a detector capacitance of 50 fF, is close to 73 e^- r.m.s. simulated at the temperature of 27 °C and 67 e^- r.m.s. with a temperature of −20 °C [117].

In particular, Figure 3.13 (left plot) shows the zero dead-time behavior of the front-end with injections of $1000e^-$, $5000e^-$, and again $1000e^-$ in sequential bunch crossing periods (25 ns), with a threshold set to $600e^-$. As shown in the figure, the comparator is able to successfully process the three consecutive signals.

The ENC evaluated at the comparator output has been obtained from the comparator hit efficiency curve (Figure 3.13, right). Such a curve, obtained through a set of 200 transient noise simulations, can be fitted by means of an error function of the form $\eta_{hit} = \frac{1}{2}\left[1 + \mathrm{erf}\left(\frac{Q_{in}-p_1}{p_2\sqrt{2}}\right)\right]$, where in this context p_1 represents the threshold value at which the hit efficiency is 50%, and p_2 corresponds to the Equivalent Noise Charge. Using least-squares fitting, this provides a noise close to $126e^-$ r.m.s. Similarly, the threshold dispersion can be evaluated starting from the comparator hit efficiency, defined as the fraction of events where the comparator output exceeds the threshold in response to an injected charge, resulting from a set of 200 Monte Carlo simulations. A hit is counted when the comparator output transitions to a logic high state following an injection event. The fit of the curve (Figure 3.14-left) reveals a threshold dispersion close to $30e^-$ r.m.s. Moreover, the plot in Figure 3.14-right shows that the threshold is pretty stable with respect to injection delay (i.e. the time difference between injection and clock edge), with a threshold variation not larger than 50 electrons in response to a delay ranging from -1 up to +1 ns.

3.5 The Prototype Chip

Based on the described structures, a prototype chip featuring a matrix of readout channels has been designed. The full chip prototype (Figure 3.15) consists of a 4×8 matrix of

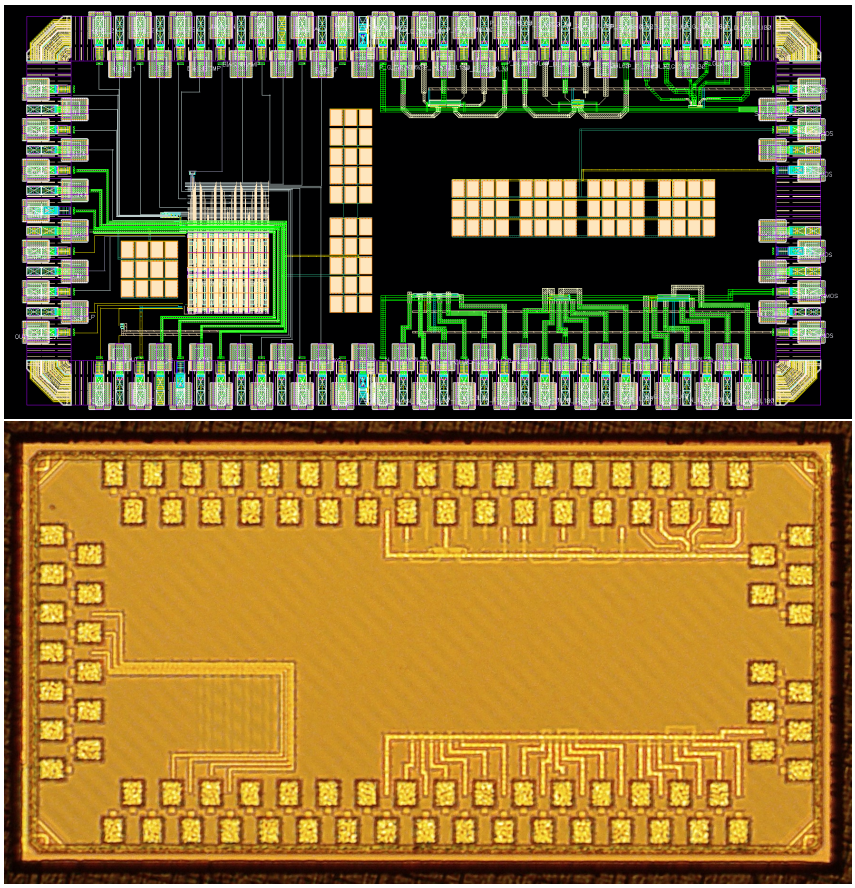


Figure 3.15: (Top) Layout of the prototype chip; (Bottom) Microscope photo of the prototype chip (1×2 mm^2). The left side of the chip contains the 4×8 pixel matrix, bias management periphery, and a CSA output source follower, which buffers the output of the charge sensitive amplifier to provide a low-impedance signal for testing and characterization purposes. The right side includes stand-alone MOS test structures. The remaining chip area is occupied by filtering capacitors to reduce noise coupling.

front-end channels (shown in Figure 3.18). Bias blocks for the charge sensitive amplifiers and the comparators integrated in the readout matrix are placed in the periphery of the chip. The CSA output signal is made available, for testing purposes, to a dedicated PAD for one pixel of the matrix. The signal for this pixel is buffered by means of a cascade of two source followers. Moreover, a set of single transistors with different sizes has been integrated. This will allow for static and noise characterization of the 28 nm technology. The matrix is composed of analog islands of 2×2 pixels, as shown in Figure 3.17, following the design approach of the RD53 collaboration. An analog island is a group of neighboring pixels that share analog front-end circuitry, optimizing area and power consumption. By sharing analog resources among multiple pixels, this approach minimizes the overall silicon area required for each pixel, reduces total power consumption, and helps suppress noise coupling between analog and digital domains—key advantages for high-density pixel matrices in modern readout chips. During the layout design, particular attention was paid to implementing this approach. To facilitate connectivity, the pixels were mirrored and rotated during placement, allowing the inter-block connections to align automatically

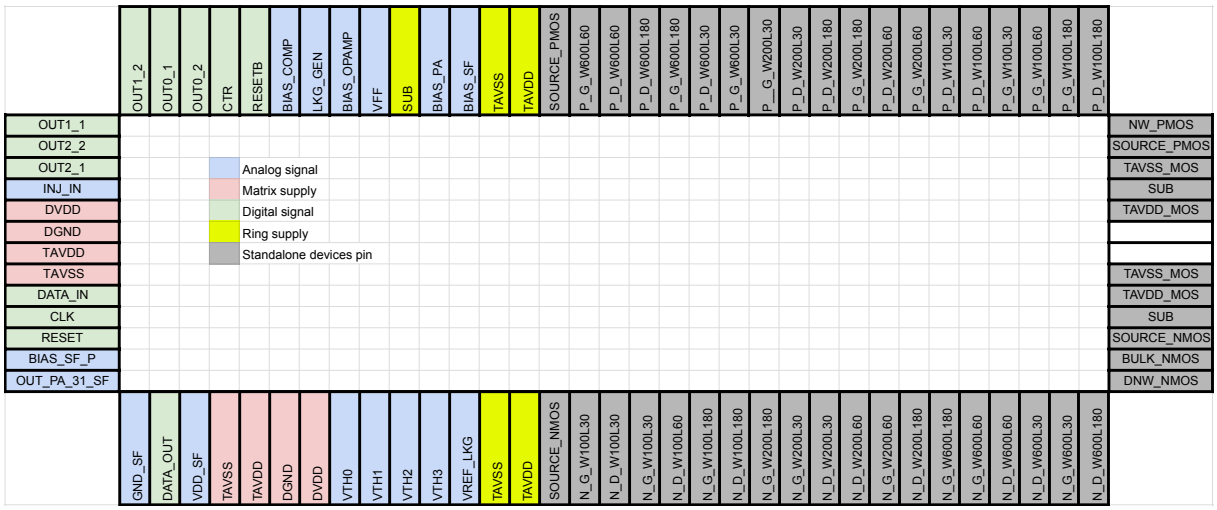


Figure 3.16: Pinout map of the prototype chip showing the assignment of external signals to the bond pads. The diagram includes bias management signals, configuration interfaces, and output connections for testing and characterization. Gray pads are relevant to single MOS structures not described in this work.

and simplifying matrix assembly. This strategy reduces routing complexity and ensures consistent connectivity across the pixel array. The analog island approach also allows for a modular design, where each island can be placed to form a larger matrix. This modularity makes it easier to integrate the front-end channels into larger readout systems, such as those used in high-energy physics experiments. Each analog island is composed of four front-end channels (pixels), and each pixel contains its own Charge Sensitive Amplifier, comparators, and double-hit detection stage. The pixel matrix is surrounded by filtering capacitances that decouple and suppress noise between analog and digital domains. Figure 3.16 shows the pinout of the chip, which includes bias management signals, configuration interfaces, and output connections for testing and characterization.

Every channel of the pixel matrix is provided with programmable structures. The diagram of a prototype channel is shown in Figure 3.19. The main configurable settings for each front-end channel include enabling or disabling the input signal, emulating sensor leakage current, selecting detector-emulating capacitances (25 fF, 50 fF, or both), and controlling the connection of each output signal to the shared bus via tristate inverters; these features can be activated individually using a set of switches and logical configuration signals. When disabled, the input is connected to ground. In this way, only the enabled pixel is tested with the injection signal, and the other channels of the matrix are insensitive to possible swings on the injection bus. As mentioned, a circuit that emulates the presence of a leakage current from the sensor is also available. This is implemented using a dedicated MOSFET (LKG) in each pixel, which can be enabled via the shift register; the bias current for leakage emulation is set by a peripheral current mirror and scaled down to the CSA input through a double-stage mirror, allowing precise control of the emulated leakage current.

Since the output signal of every channel is connected to a shared bus, every Double Hit Detection block output is connected to a tristate inverter. The 2-bit flash ADC is implemented as a trio of comparators. Each comparator output is processed by a double-hit detection stage that produces two outputs, so every channel has six output signals

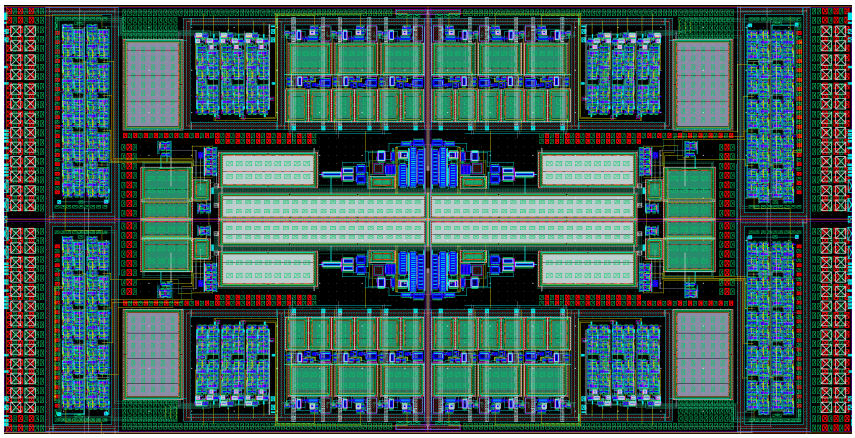


Figure 3.17: Layout of a analog island of 2x2 pixels.

(three comparators × two outputs each). Thus six digital control signals are needed to connect or disconnect their column driver from the output bus. A chain of 10-bit shift registers distributed through the matrix makes it possible to configure each front-end channel (see Figure 3.20). Table 3.2 explicitly defines the correspondence between each bit of the 10-bit configuration register and the control signals for every pixel, ensuring clarity for readers unfamiliar with the mapping convention. The mapping between the 10-bit configuration register and the actual control signals for each channel is summarized in Table 3.2. The layout of a channel of the prototype is reported in Figure 3.18 and highlights the main blocks described here. The channel cell size is $25 \times 50 \mu m^2$.

The shift register output of any pixel is connected to the input of the next one, so a 320-bit serial signal is needed to configure the whole matrix (10 bit × 32 pixels in the readout matrix). The first 10 bits configure the first pixel, the next 10 bits configure the second pixel, and so on, until all pixels are set. Within each pixel, the bit order follows Table 3.2. Figure 3.24 shows an example of the configuration signal pattern for a pixel, illustrating how the serial configuration is applied across the matrix.

Regarding the bias management of the pixels, a peripheral block is integrated in the chip. It provides the necessary bias currents to the various components of the pixel matrix, ensuring proper operation and performance. In order to achieve this, the peripheral block includes a set of current mirrors with proper multiplication factors to generate the required bias levels. The implemented approach leverages on the connection of the current mirror loads to the pads of the chip, which are then connected to external fixed resistors in series to a trimmer. This allows for a fine tuning of the bias current, which is essential for optimizing the performance of the front-end channels. Another important aspect of the use of the trimmers is to perform analog sweeps on the bias voltages and currents, which can be useful for characterizing the front-end channels and optimizing their performance in various conditions. In order to maintain measurable bias currents with the available laboratory instruments without having to use dedicated probe stations, the current mirrors have been designed to provide currents in the order of microamperes. The implemented structure is shown in Figure 3.21. The fixed resistor, or reference resistor, is connected to the pad of the chip, and the trimmer is connected in series to it. The current mirrors are connected to the pads, and the external trimmer allows for fine-tuning of the bias levels. Across the fixed resistor test points are present for measuring the bias currents and voltages, which can be accessed using standard laboratory equipment. For the characterisation activity, the peripheral block has been configured to provide the

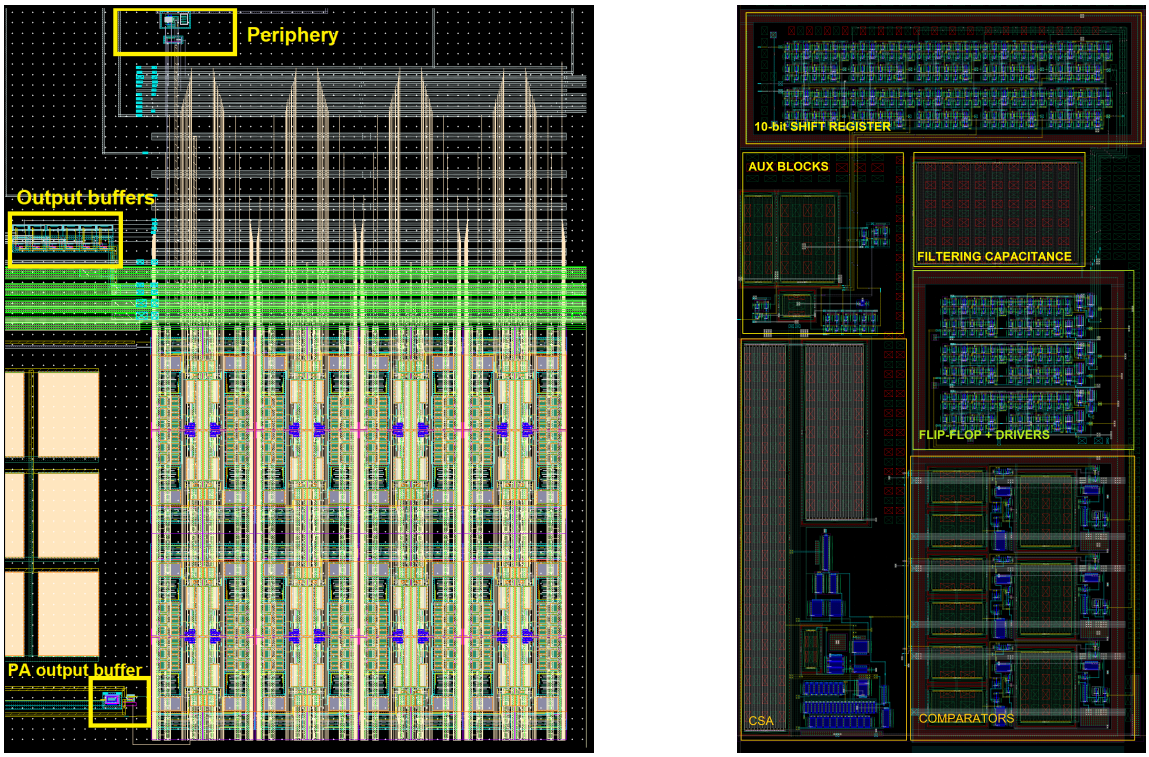


Figure 3.18: (Left) Layout of the matrix in the prototype chip ($200 \times 200 \mu m^2$). (Right) Layout of a cell of the prototype chip ($25 \times 50 \mu m^2$), highlighting CSA, Comparator, Flip-flop with tristate inverter, and 10-bit Shift register stages.

following bias levels:

- `LEAKAGE`=1 µA. The leakage current emulation uses a double current mirror approach, implemented as two cascaded current mirrors with scaling ratios of 20:1 and 20:1, resulting in a total scaling factor of 400:1 between the peripheral bias current and the current delivered to the input node of each pixel's CSA. This means that the current set at the periphery is mirrored and divided by 400 before reaching the pixel input, allowing precise control of small leakage currents using larger, more easily measurable peripheral currents. The presence of this emulated leakage current at the CSA input can be, as already mentioned, enabled or disabled for each pixel via the `LEAKAGE_EN` control signal, which is managed by the 10-bit shift register of each pixel previously described.

- `BIAS_PA`=26 µA. At the periphery, a current of 26 µA is supplied; after a scaling factor of 10:1 in the current mirrors, this provides 2.6 µA to the main branch of the gain stage of the CSA (see Figure 3.2). The secondary branch of the regulated cascode (the branch including transistor M_5) receives a current further scaled by a factor of 16:1.

- `BIAS_COMP`=4 µA: At the periphery this bias current supplies to every comparator of the matrix the proper bias current to the two common-source active load transistors. In Figure 3.4, these are shown as IB1 and IB2 current sources. In this case the mirror factor is 10:1.

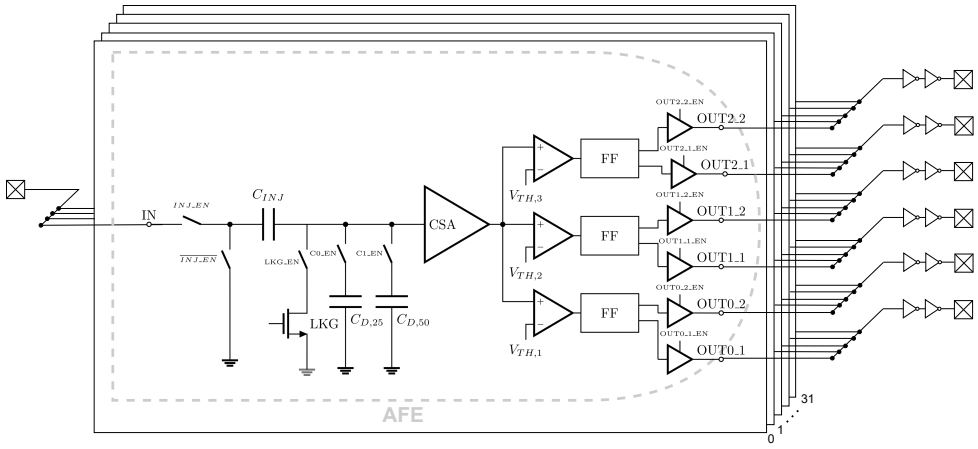


Figure 3.19: Diagram of 32 pixel matrix. In the foreground is shown the channel of a pixel within its building blocks and configuration signals. It is highlighted the presence of shared buses for both the input and output signals.

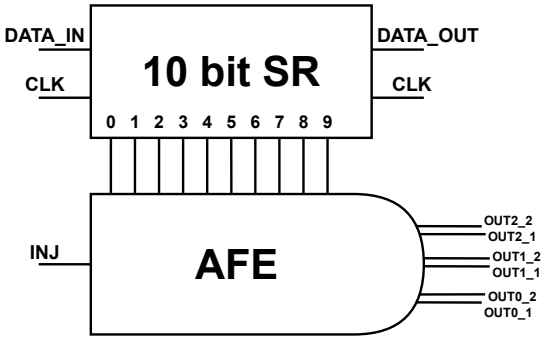


Figure 3.20: Diagram for the 10 bit shift register integration with the analog frontend channel.

- `BIAS_OPAMP`=2.6 µA. Also this bias has a 10:1 mirror factor. This bias is needed for the proper working of the feedback operational amplifier (labeled A1 in Figure 3.1), which is responsible for detecting the presence of leakage current at the input node of the CSA.

- `BIAS_SF`=13 µA. This bias current is supplied to the active load of the source follower that acts as output stage of the gain stage of the CSA (see Figure 3.2). The mirror factor is 10:1, meaning that a current of 13 µA is supplied at the periphery to provide 1.3 µA to the source follower.

- `BIAS_SF_P`=50 µA and `OUT_PA_31_SF`=1 mA: these currents are used to properly bias the output buffer of a dedicated test pixel in the matrix (pixel 31), which is dedicated solely to providing direct access to the CSA output for testing and characterization purposes, rather than for normal matrix operation. This design choice allows the CSA output to be routed to a dedicated pad, enabling precise analog measurements that would not be possible if all pixels were used exclusively for standard readout. The buffer is designed with two source follower stages, each sized to drive a 5 pF load. The total gain of the buffer is close to 0.9.

Another important level of tuning is available through the voltage reference `VFF`,

SR bit	Enabled signal
0	OUT2_1_EN
1	OUT2_2_EN
2	OUT1_1_EN
3	OUT1_2_EN
4	OUT0_1_EN
5	INJ_EN
6	C1_EN
7	C0_EN
8	LKG_EN
9	OUT0_2_EN

Table 3.2: Shift register code and control signal pairing for each pixel. Consider that OUT0_1_EN, OUT0_2_EN, OUT1_1_EN, OUT1_2_EN, OUT2_1_EN, and OUT2_2_EN are the six output drivers of the channel. INJ_EN is the input signal enable, C0_EN and C1_EN are the detector-emulating capacitance enable signals, and LKG_EN is the leakage current enable signal. For a matrix of 32 pixels, a 320-bit serial configuration signal is needed, with each pixel controlled by a 10-bit shift register.

which is responsible to manage the current discharging the feedback capacitance of the CSA. By moving this voltage reference, it is possible to change the fall time of the CSA output signal. However, within the standard operating range of the channel, the power consumption depends only weakly on this current. The voltage reference `VFF` is generated on the PCB and connected to a pad of the chip. This allows for an external tuning of this voltage level, which can be useful for optimizing the performance of the front-end channels in various conditions, such as after irradiation operations.

3.6 Data Acquisition System

The digital output of the comparator is the only element that can be used to evaluate the main analog performance parameters of the prototype chip. In order to characterize its behavior, it is possible to measure the probability of the discriminator to fire in presence of a charge at the input of the pixel: this operation is performed through *charge scans*. Given a fixed threshold, in order to properly reconstruct the comparator efficiency curve (also referred to as s-curve), it is necessary to repeat charge injections for an appropriate number of times. As mentioned in the previous section, for each channel, it is possible to fit the s-curve using the function:

$$\eta_{hit} = \frac{1}{2}\Big[1 + \mathrm{erf}\Big(\frac{Q_{in} - p_1}{p_2\sqrt{2}}\Big)\Big], \tag{3.18}$$

where η_{hit} is the comparator hit efficiency, Q_{in} the injected charge, p_1 is the threshold value (the charge at which the hit efficiency is 50%), and p_2 is the Equivalent Noise Charge (ENC, representing the noise width of the transition). Thus, by evaluating η_{hit} for every pixel, it is possible to have an information about the ENC and the threshold distributions. The injected charge signal at the input of the CSA is obtained by means of a negative

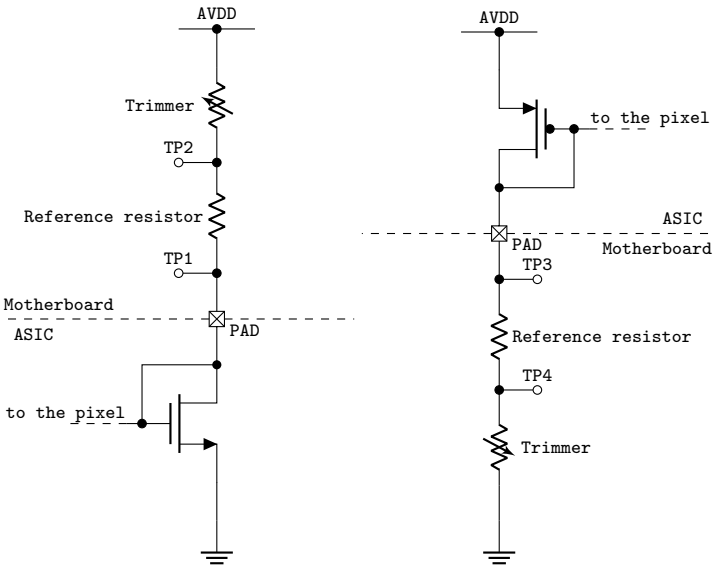
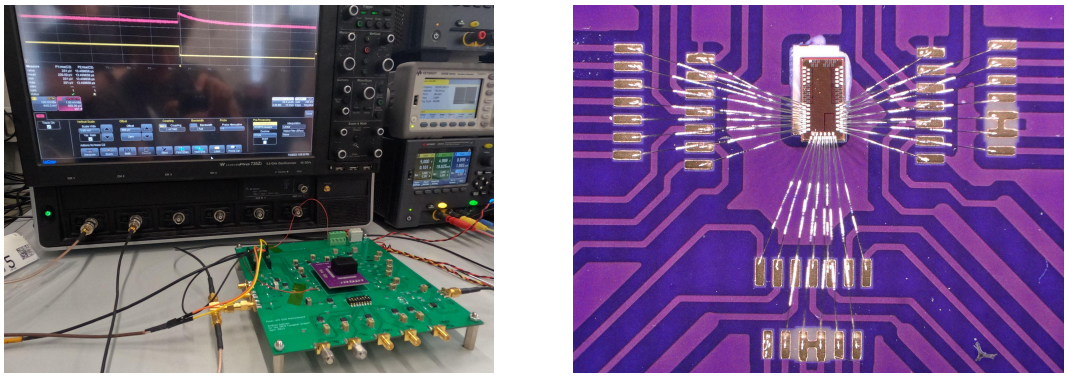


Figure 3.21: Diagram of the implemented approach for the peripheral block for bias management. It shows the current mirrors and their connections across the pads, as well as the external trimmer for fine-tuning the bias levels.

step signal, referenced to ground, and an injection capacitance ($C_{INJ} = 5\,\text{fF}$) in series with the input node. In this context, the amplitude ΔV_{in} refers to the absolute value of the voltage step applied at the CSA input. Thus, the input charge is calculated as $Q_{in} = C_{INJ} \cdot \Delta V_{in}$.

The objective of the characterization of the prototype chip is to reconstruct the main analog performance parameters and compare them to the simulated ones. In order to do it a Data Acquisition (DAQ) system has been developed. The DAQ system has to manage the 40 MHz clock signal needed by the comparator, handle the injection signal with a variable amplitude in the range of $3 - 300mV$, configure the shift registers of the pixels, read their output signals and compute the η_{hit} curve for every pixel.

The DAQ system shown in Figure 3.22, whose architecture is shown in Figure 3.23, is composed of a motherboard (responsible to provide all the voltage and current biases to the prototype chip), a power supply unit, a Data Timing generator and a PC. The motherboard also hosts the prototype chip, wire bonded on a carrier board, and an Arduino Nano 33 IoT. The Arduino board is needed to control the configuration bits required by every pixel and to read the outputs of the prototype chip. The Tektronix DTG 5334 Data Timing Generator, connected through the GPIB-USB-HS interface to the PC, is used to generate the injection signal and to feed the comparators with the 40 MHz clock, synchronous with the injection signal. A Python-based software package [118] has been developed as part of this thesis work specifically to manage data readout, configure the prototype chip, and send the required settings to the Data Timing Generator. A Graphical User Interface has been developed using the Tkinter Python framework to facilitate the data characterization process. The exchange of the readout and configuration data between the motherboard and the PC is made through the serial port of the Arduino board. The readout data received by the PC is analyzed by the DAQ Python-based software, giving information about the threshold, ENC and their distribution over the matrix. Finally, these information can be exported for deeper offline analysis.



(a) (b)

Figure 3.22: (a) Test setup showing the motherboard with the prototype chip, power supply, and oscilloscope; the oscilloscope displays the injected signal and CSA output. (b) Detail of the prototype chip wire bonded on the carrier board.

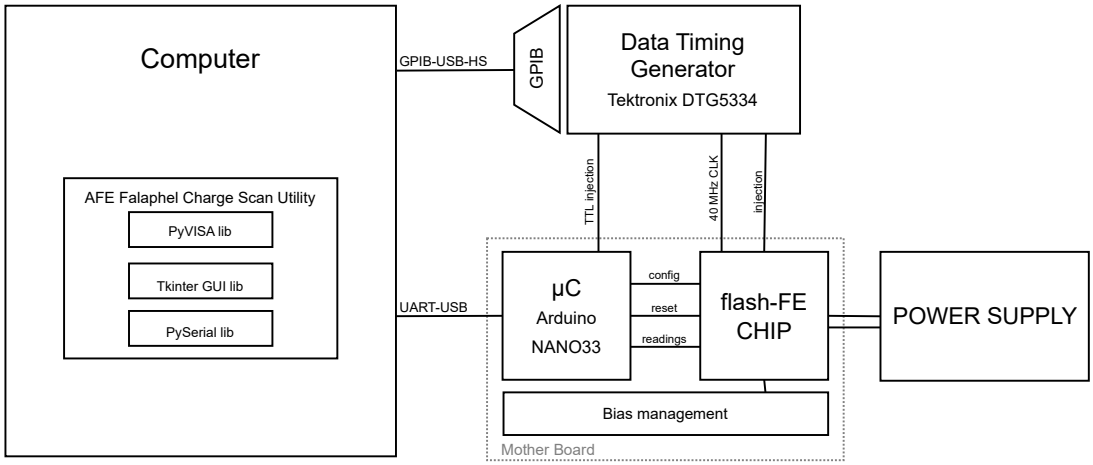


Figure 3.23: Architectural scheme of the developed Data Acquisition System.

Considering a typical testing flow, it is necessary to automate these operations:

1. configure the 10 bit shift register of every pixel with the desired settings generating the clock signal to slide the proper digital serial configuration signal. Figure 3.24 shows an example of the signals involved in the configuration of a pixel.

2. set the injection signal amplitude and the 40 MHz clock from the DTG. Considering that it is necessary to iterate the injections several times, the first is realized through a square wave which amplitude can span in the range of $3 - 300mV$. The latter is a 900mV amplitude square wave.

3. read the output signals from the double-hit detection stage and reset the double-hit detection stage (that is working as a latch) in order to be ready for the next injection event.

In order to keep everything consistent, the frequency of the reading and reset operations is set by the injection signal. The rising edge of this signal triggers the reset

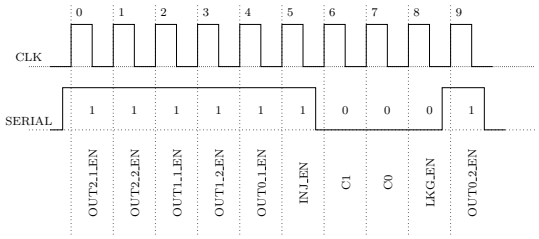


Figure 3.24: Example configuration signal pattern for a pixel, showing the serial bit stream that enables only the six output drivers and the injection setting, as defined in Table 3.2. In this example, bits 0–4 and bit 5 of the shift register are set to 1 (OUT2_1_EN, OUT2_2_EN, OUT1_1_EN, OUT1_2_EN, OUT0_1_EN, INJ_EN), while all other bits are set to 0.

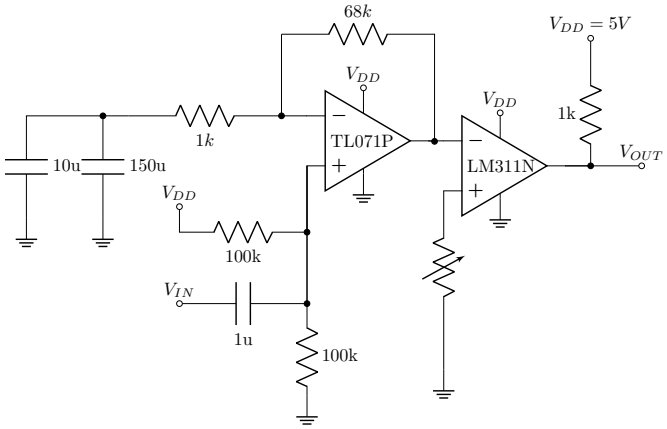
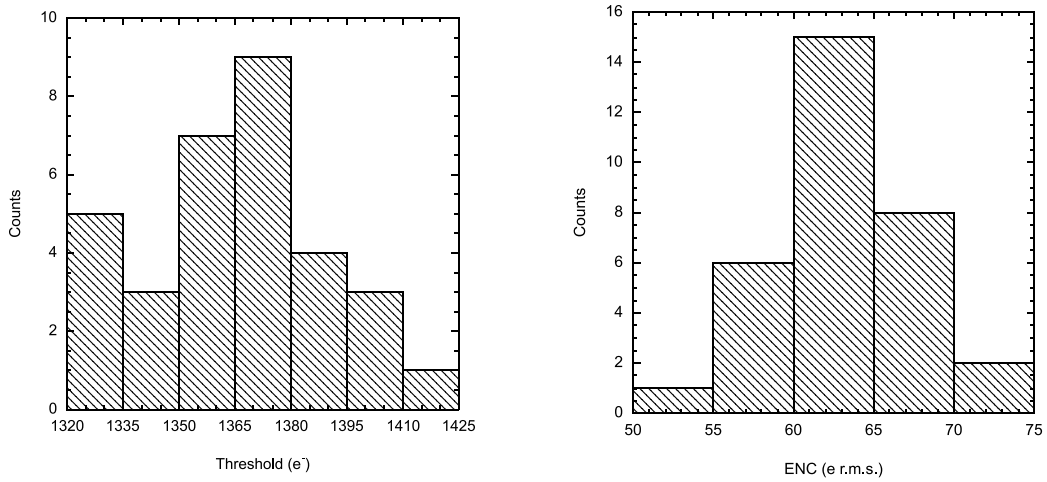


Figure 3.25: Schematic of the signal adapter from the DTG to the microcontroller. The circuit amplifies the injection signal and converts it to a TTL level suitable for the Arduino board. The trimmer is used to set the threshold for the comparator.

operations. The falling edge triggers the reading operations. Actually the DTG only offers two output channels that are used for the 40 MHz clock and the low voltage injection signal.

Since the Arduino microcontroller requires standard TTL (Transistor-Transistor Logic) levels—specifically, digital signals with voltage levels compatible with its 3.3V logic inputs—to reliably detect external interrupts, it is necessary to adapt the amplitude of the injection signal from the DTG. For this reason, the stage shown in Figure 3.25 has been designed and integrated on the mother board PCB. The circuit is composed of a non-inverting amplifier that increases the amplitude of the injection signal from the DTG, followed by a comparator (LM311N) whose output generates a clean digital (TTL-level) signal. The comparator threshold is set by a trimmer connected to its positive input and should be adjusted to a value higher than half of the Arduino power supply voltage, ensuring that the output toggles cleanly and produces a logic-level signal that the Arduino can interpret as a digital input.

At this stage, the system can be configured to execute a chip scan to calculate the Equivalent Noise Charge and the threshold dispersion that distinguishes this front-end circuit.



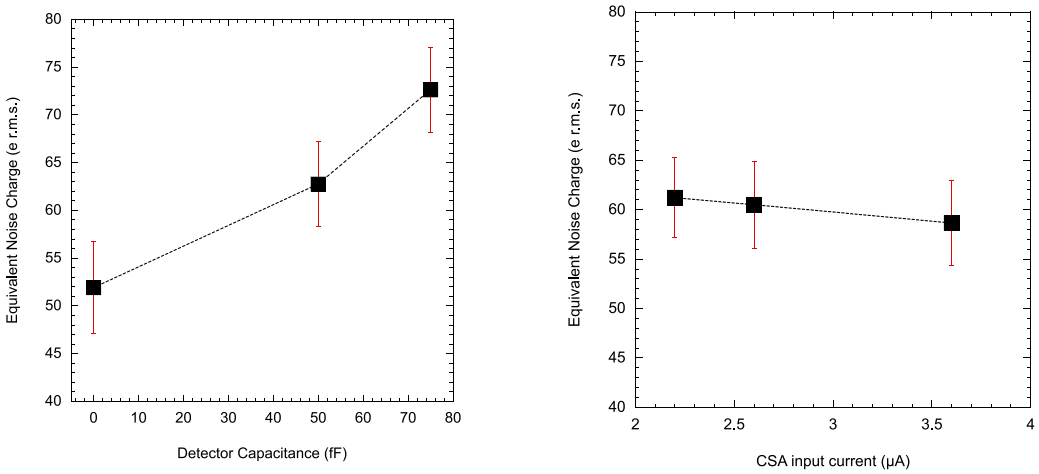
(a) (b)

Figure 3.26: (a) Threshold distribution for the 4×8 matrix integrated in the prototype chip. (b) Equivalent Noise Charge distribution for the 4×8 matrix integrated in the prototype chip.

3.7 Prototype chip characterization

The prototype chip has been characterized at room temperature (27 °C) mainly from the standpoint of noise and threshold dispersion performance. Figure 3.26a shows the measured threshold distribution for the 32 readout channels integrated in the matrix. Data have been obtained with a comparator clock frequency of 10 MHz. Although the front-end is capable of operating at higher frequencies, the clock signals on the test board used for chip characterization suffer from degradation due to factors such as increased jitter (measured up to 350 ps RMS), signal attenuation, and limited bandwidth of the PCB traces and connectors. These issues can lead to timing uncertainties and reduced signal integrity, which negatively impact the reliable operation and measurement accuracy of the front-end at higher clock frequencies. A mean threshold close to 1365 electrons has been measured. The standard deviation, referred to as threshold dispersion, is 24 electrons r.m.s., which is in fairly good agreement with the simulated value. Since the measured dispersion is already very small, additional in-pixel tuning circuitry is not necessary, simplifying the pixel design. As far as noise performance is concerned, Figure 3.26b shows the Equivalent Noise Charge distribution measured for the 4×8 matrix. A mean ENC close to 63 electrons r.m.s. has been measured across all 32 channels in the matrix, with a rather small standard deviation of approximately 4 electrons. The ENC distribution has been obtained by configuring a 50 fF detector-emulating capacitor at the CSA input of every pixel in the matrix, ensuring that this configuration was applied uniformly to all pixels during the measurement.

On the other hand, Figure 3.27a shows the behavior of the mean Equivalent Noise Charge as a function of the detector-emulating capacitance, where the red error bars refer to the noise standard deviation as obtained for the 32 pixels in the matrix. The effect of the preamplifier bias current on the noise performance is shown in Figure 3.27b, which reports ENC data for bias currents of 2.2 µA, 2.6 µA, and 3.6 µA, with the corresponding measured ENC values being approximately 62, 61, and 60 electrons r.m.s., respectively. The small change in noise as the preamplifier bias current increases can be explained by



(a) (b)

Figure 3.27: (a) Equivalent Noise Charge measured as a function of the detector emulating capacitance. (b) Equivalent Noise Charge as a function of the CSA bias current.

two competing effects. On one hand, increasing the bias current raises the transconductance of the input transistor, which typically reduces noise. On the other hand, a higher bias current also increases the bandwidth of the CSA, which can introduce more noise. As a result, these effects tend to balance each other, leading to only a slight reduction in noise as the bias current increases.

It is important to note that the CSA was tested in two distinct operating modes: one optimized for flash analog-to-digital conversion (with slow discharge of the feedback capacitor C_F), and another optimized for time-over-threshold (ToT) conversion (with fast discharge of C_F). The plots in Figure 3.28 illustrate the temporal behavior of the front-end in ToT mode, where a fast discharge is used. This distinction is crucial to avoid confusion, as the ToT mode produces a much shorter output pulse compared to the flash mode. The main analog performance parameters of the CSA, including the output signal amplitude, peaking time, discharge slope, and time-over-threshold, are measured by applying a controlled voltage step signal across the injection capacitor using a waveform generator (Tektronix AFG31000 series). In this experimental setup, a known voltage step is applied to the input node via a injection capacitor, nominally a 5 fF MoM capacitance. The preamplifier output signal in response to an input charge of 3200 e^- is shown in Figure 3.28a, for a feedback bias voltage V_{FF} (which sets the operating point of the feedback transistor in the CSA and, in turn, its baseline recovery time, see Section 3.1 for details) ranging from 580 mV to 620 mV and a detector-emulating capacitance of 50 fF. The Time-over-Threshold (ToT) is defined as the time interval during which the signal at the CSA output remains above the discriminator threshold; it can be approximated, for very low thresholds, as $t_{peak} + t_{falling}$, where t_{peak} is the time taken for the CSA output to reach its maximum value after charge injection, and $t_{falling}$ is the time required for the signal to return from its peak back down to the baseline level. In practice, ToT is measured by applying a known charge to the input and recording the duration for which the output stays above the threshold, providing a direct indication of the input charge and the CSA dynamic response [119]. The value of the current, I_{FF}, discharging the CSA feedback capacitance can be estimated from the measured return-to-baseline slope of the

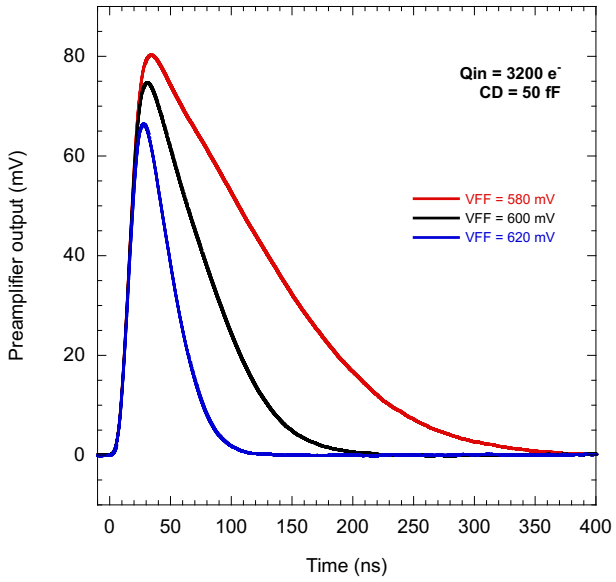


Figure 3.28: Measured output signal from the charge sensitive amplifier for different feedback bias voltages V_{FF}, with a detector-emulating capacitance of 50 fF at 27°C.

CSA output signal using the relationship $I_{FF} = -C_F \cdot \frac{dV_{OUT}}{dt}$, as described in Equation 3.10. The Time-over-Threshold can be easily computed by means of the following:

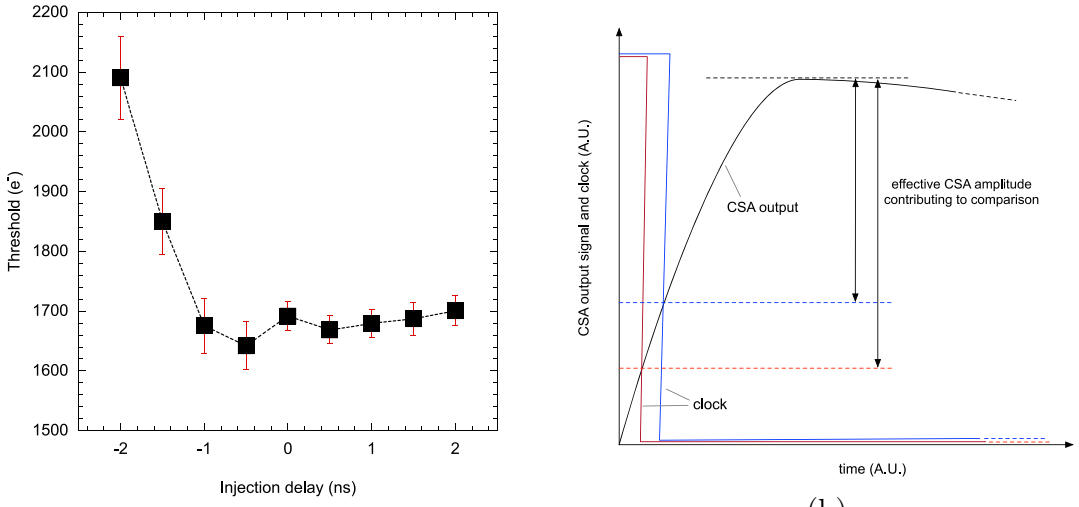
$$\text{ToT} = t_{peak} + t_{falling} = (\alpha + \beta Q_{\text{in}}) + \frac{Q_{\text{in}} - Q_{\text{th}}}{I_{\text{FF}}} \tag{3.19}$$

with α (in nanoseconds, typically ranging from 10 to 100 ns) and β (in nanoseconds per electron, typically ranging from 0.001 to 0.01 ns/e$^-$) as fitting parameters, Q_{in} the input charge, Q_{th} the threshold charge. Here, α represents the characteristic peaking time of the CSA output signal, while β quantifies the additional peaking time per unit of injected charge, reflecting the dependence of the signal rise time on the input charge.

According to simulation data discussed in section 3.4, threshold stability was investigated by measuring how the effective threshold changes when there is a delay between the CSA output signal and the threshold signal applied to the comparator. Ideally, the CSA output and the threshold signal should arrive at the comparator simultaneously, synchronized with the falling edge of the clock. In practice, small delays can occur due to clock skew or uncertainties in the timing of charge delivery from the sensor.

In particular, Figure 3.29a shows the measured threshold as a function of injection delay, defined as the time difference between the charge injection at the CSA input and the application of the threshold step at the comparator input. For positive delays (charge arrives after the threshold), the variation in the effective threshold required for detection is small—less than 20 electrons for delays up to 2 ns. For negative delays (charge arrives before the threshold), the effective threshold required for detection increases significantly.

This behavior is due to the finite rise time of the CSA output signal. The comparator samples the CSA output at the instant the threshold is applied; if the CSA signal is still rising at that moment, its value is lower than its peak amplitude. As a result, a higher effective threshold is needed to trigger the comparator, since the sampled CSA signal is not yet at its maximum. Figure 3.29b qualitatively illustrates this effect: the comparator responds to the difference between the CSA signal level at the moment the threshold



(a) (b)

Figure 3.29: (a) Effective threshold as a function of the delay between charge injection and threshold application, measured for a peripheral pixel with a 50 fF detector-emulating capacitance, CSA bias current of 2.5 μA, and temperature of 27°C. (b) Qualitative preamplifier output response with two example clock signals showing how the timing affects the effective CSA signal amplitude used for comparison with the threshold.

is applied and the threshold itself. This measurement is in good agreement with the simulation results shown in Figure 3.11, confirming the expected behavior and validating the design approach.

Figure 3.30-left shows the measured CSA output of a peripheral pixel in response to input signals ranging from about 600 to 13,000 electrons, with a detector-emulating capacitance of 50 fF. The output signal features a slow return-to-baseline (about 5 μs for an input signal of 6,000 electrons), which is required for proper operation of the comparator stage. The CSA peak amplitude is linear with the injected charge up to approximately 7,000 electrons; for input signals above this value, a noticeable deviation from linearity occurs, and saturation effects become significant.

Figure 3.30-right shows the measured output of the double-hit detection stage in response to two sequential charge injections separated by 25 ns, corresponding to the bunch crossing period. This demonstrates the zero dead-time capability of the front-end channel, as both events are successfully detected in consecutive bunch crossings without loss.

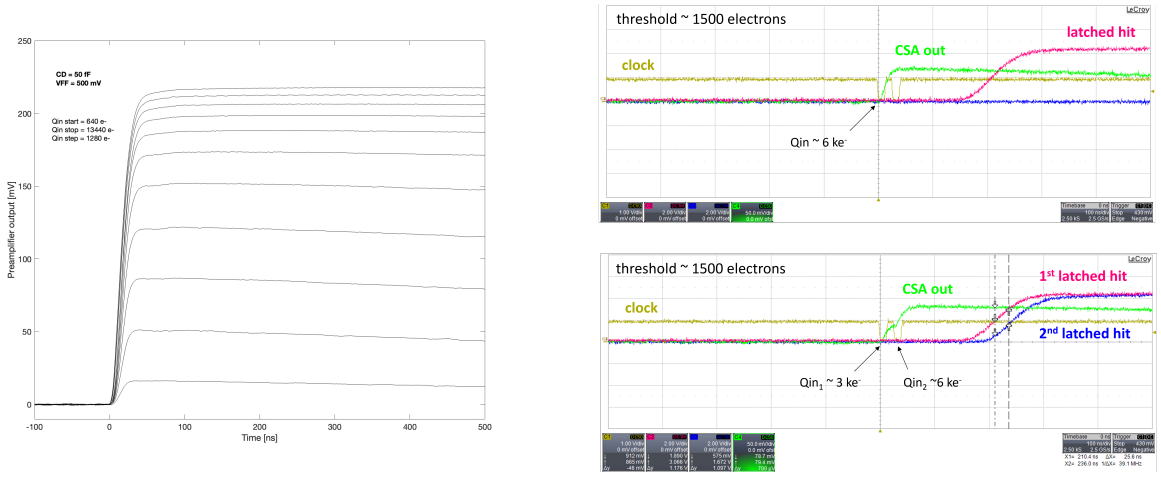


Figure 3.30: (Left) Measured preamplifier response to input signals ranging from 640 to 13,440 electrons, injected via a calibrated voltage step across the injection capacitor with a 50 fF detector-emulating capacitor enabled. (Right) Measured output of the double-hit detection stage in response to two sequential charge injections spaced by 25 ns, demonstrating zero dead-time operation.

Chapter 4

Time-over-Threshold front-ends

This chapter discusses the development of two Time-over-Threshold (ToT) front-end architectures, one tailored for High Energy Physics (HEP) applications and the other for X-ray imaging. Both architectures are designed to implement the ToT technique, which is crucial for accurately measuring the energy of incoming signals by analyzing the time duration for which the signal exceeds a predefined threshold. However, they are optimized for different operational requirements and applications, and exploit different circuit solutions. They have been developed in the framework of the *Falaphel* and *PiHEX* projects, and are based on the same technological platform, a 28 nm CMOS process.

4.1 High Energy Physics architecture

The architecture described in this section is designed for High Energy Physics applications, such as the Future Circular Collider (FCC) and the Large Hadron Collider (LHC) experiments, where accurate energy measurement of detected particles is essential and robust operation in harsh radiation environments is required.

4.1.1 Front-end channel description

The diagram of the HEP architecture, shown in Figure 4.1, targets the same extreme conditions as the flash ADC front-end described in the previous chapter. This architecture was developed for operation in harsh radiation environments, such as those at the hadronic Future Circular Collider (FCC-hh). It may also be relevant for possible upgrades at the CMS and ATLAS experiments in the post phase-II era at the LHC. The front-end channel described in the figure, and detailed in the first part of this chapter, exploits the ToT technique for the digitization of the signal delivered by the sensor. It includes a compact Charge Sensitive Amplifier, DC coupled to a differential comparator whose output drives both the ToT and Time-of-Arrival counters. A 5-bit digital-to-analog converter (DAC) is integrated in each cell for local threshold tuning.

Figure 4.2 presents the complete schematic of the front-end channel, explicitly showing the Charge Sensitive Amplifier, the pre-comparator stage (whose detail are crucial for understanding the threshold tuning system discussed in the following sections), and the comparator itself. The charge sensitive amplifier, similarly to the flash-ADC based version, features two independent feedback loops. The first feedback loop integrates the transistor M_F with the capacitor C_F, and is responsible for processing the signal, integrating the charge delivered by the sensor into C_F and subsequently discharging it. The second loop,

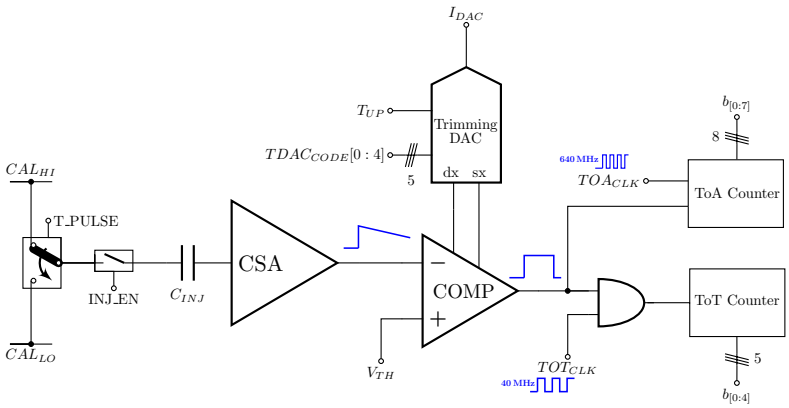


Figure 4.1: Schematic diagram of the front-end channel for HEP environments based on the ToT technique. The diagram shows an high level of abstraction in order to highlight the main blocks of the front-end channel, including the Charge Sensitive Amplifier, the comparator and the trimming DAC circuit itself.

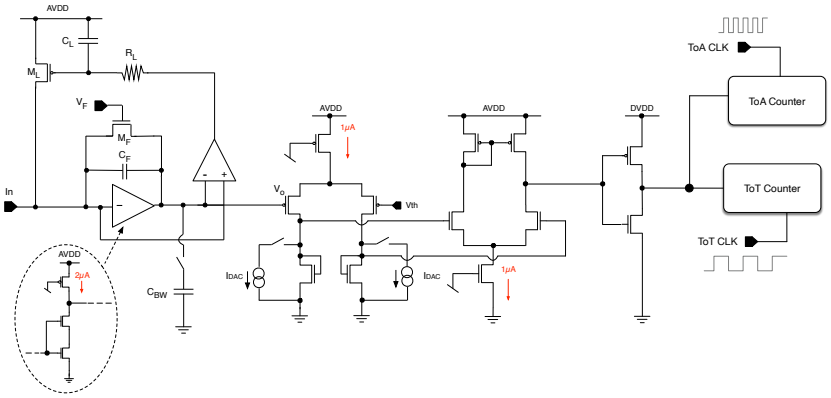


Figure 4.2: Schematic diagram of the front-end channel. The Charge Sensitive Amplifier is DC coupled to a pre-comparator stage, used for single-ended to differential signal conversion, followed by the comparator.

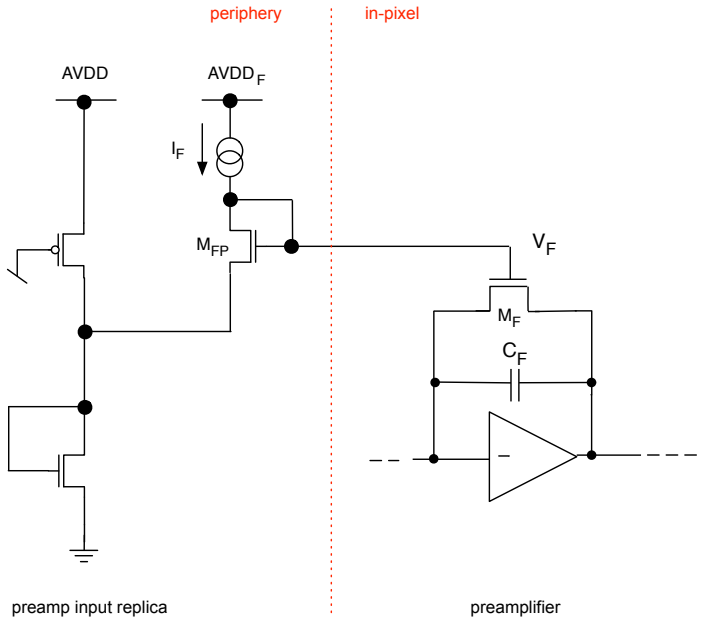


Figure 4.3: Schematic diagram of the circuit generating the bias voltage V_F for the CSA feedback transistor M_F which is responsible for the feedback capacitance discharge.

which includes a low-power (around 0.2 μW) amplifier and the PMOS transistor M_L, provides the front-end channel with a compensation mechanism for the detector leakage current. The feedback operational amplifier locks the DC level at the CSA output to the gate-to-source voltage of the preamplifier input transistor, even in the presence of leakage current, by adjusting the potential at the gate of M_L. The C_L capacitor and the R_L resistor, implemented by means of a NMOS transistor with gate and source terminals tied together (a technique to realize compact, high-value resistances), introduce a very low frequency pole at around 1 Hz in the feedback loop, so that the compensation circuit reacts to DC leakage currents only. The CSA gain stage is based on the so-called self-cascode (also known as composite cascode) configuration, which consists of two transistors of the same type connected in series to improve gain and output resistance compared to a straightforward common source stage, while keeping the input capacitance low [89]. From circuit simulations performed in the typical process corner at room temperature, the DC open-loop gain of such a stage was found to be close to 50 dB. For the self-cascode architecture, shown in the in-set of Figure 4.2, and considering M_1 the input device, M_2 the cascoded transistor and M_3 the active load, the input-referred noise spectral density is given by the following expression:

$$\frac{\overline{de_{rc}^2}}{df} \approx \frac{4kT\tau}{g_{m1}} \left(1 + \left(\frac{g_{ds1}}{g_{m1}} \right)^2 + \frac{g_{m3}}{g_{m1}} \right) \tag{4.1}$$

where g_{m1} is the transconductance of the input transistor, g_{m3} is the transconductance of the active load transistor, and g_{ds1} is the output conductance of the input transistor. The noise contribution of the cascoded transistor M_2 is proportional to $\left(\frac{g_{ds1}}{g_{m1}}\right)^2$. This architecture is very compact and, compared to a standard cascode circuit, does not require any additional bias line, which is particularly advantageous in a dense pixel matrix where minimizing routing complexity and area overhead is critical. As a matter of fact, such an

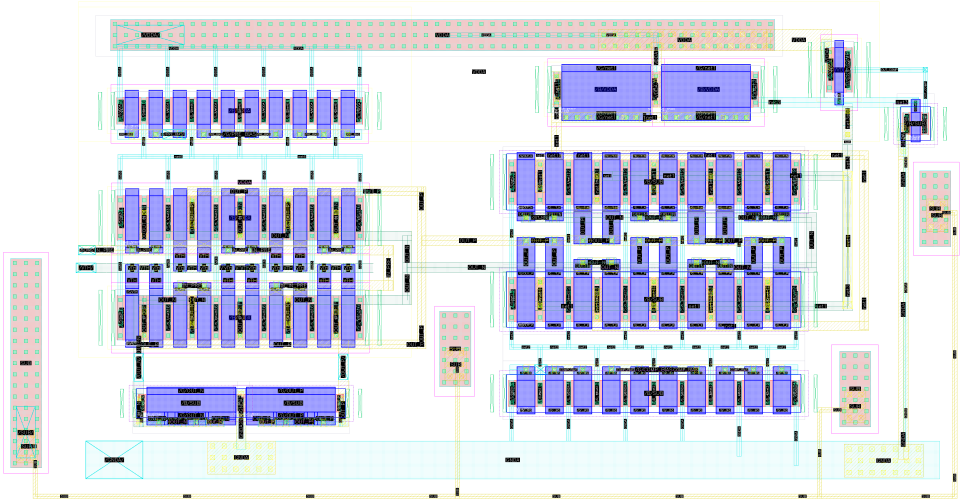


Figure 4.4: Layout picture of the comparator block. The layout is designed to be compact and suitable for integration in a pixel matrix structure. The pre-comparator stage is implemented with a differential pair of PMOS transistors, followed by a differential pair of NMOS transistors, and an inverter for the final output stage.

architecture has been chosen with the aim of minimizing the area occupation of the gain stage, saving up a significant amount of the area with respect to the regulated cascode [89] configuration implemented in the flash-ADC front-end.

By programming a CMOS switch, a bandwidth-limiting capacitor, denoted as C_{BW} (with BW indicating "Bandwidth"), is connected to the preamplifier output; C_{BW} is implemented as a Metal-oxide-Metal (MoM) capacitor with a value of 20 fF. When C_{BW} is not connected, the bandwidth is around 3 MHz; when connected, it can be reduced down to 1 MHz. This is useful to limit the noise contribution of the CSA, which is the main source of noise in the front-end channel.

The current discharging the CSA feedback capacitor is provided by the transistor M_F, whose gate voltage is set to V_F. Instead of setting a direct voltage to the gate of the transistor, a solution, shown in Figure 4.3, has been proposed to make the architecture robust against process and temperature variations. In view of integrating the front-end channel in a pixel matrix structure, a replica of the CSA core amplifier is implemented in the matrix periphery, in such a way to track the gate-to-source voltage of the preamplifier input transistor.

A 1:1 current mirror, using the transistors M_{FP} and M_F, ultimately provides the current I_F for the discharge of C_F capacitor. Such a discharge is mostly linear for large input signals, which pushes the M_F transistor into saturation region; in this regime, M_F behaves as a current source, resulting in a nearly constant discharge current and thus a linear voltage decrease across C_F. This architecture may actually be exploited for compensating for IR drops across the matrix as well. Assuming that the analog power is distributed along the matrix columns, the described structure can possibly be distributed along columns (1 every n pixels, not to impair the overall power consumption of the front-end) and be connected, except for $AVDD_F$, to the local $AVDD$ and $AGND$ power supplies, in order to track voltage changes along the column. A dedicated bias line, $AVDD_F$, provides the supply for the current mirror. Since the current I_F is of the order

of tens of nanoamps, a negligible voltage drop is expected on the $AVDD_F$ line, hence a uniform discharge current can be mirrored into the pixels irrespective of their position along the matrix column.

4.1.2 The comparator stage

The threshold discriminator consists of two stages: the first stage, which is DC coupled to the preamplifier, converts the single-ended signal from the CSA output to a differential signal, and the second stage performs the actual comparison with a global threshold, V_{th}. The first stage is implemented as a differential pair with PMOS input transistors and a diode-connected NMOS load (see Figure 4.2 for the circuit schematic). The differential signal at the output of this stage is provided to the second stage, implemented by means of a straightforward differential pair with NMOS input and PMOS active load. The use of differential signals is beneficial to reduce common mode noise, improve signal integrity, and enhance power supply rejection. This is particularly important in HEP experiments, where the radiation environment and power supply fluctuations can introduce significant noise and interference. An additional gain stage, implemented as a standard CMOS inverter, is used to amplify and sharpen the output signal, providing a consolidated digital signal at the discriminator output.

Each stage of the comparator consumes 1 µA, therefore, the total current consumption is 2 µA (preamplifier) + 0.2 µA (feedback amplifier) + 2× 1 µA (comparator stages) = 4.2 µA. This results in a total power consumption around 3.8 µW.

Figure 4.4 shows the layout of the comparator block, which is designed to be compact and suitable for integration in a pixel matrix structure, but also keeping the distances between the transistors as short as possible to minimize parasitic capacitances and improve speed. Even if a threshold tuning system is implemented, the comparator layout is designed to minimize the threshold dispersion, which is a key requirement for the front-end channel. The design approach of this block is to minimize the mismatch between the two branches of the differential pair, which is crucial for achieving a low threshold dispersion. In order to achieve this, the PMOS and NMOS transistors are placed in a common centroid configuration, ensuring that the layout symmetry is maintained.

4.1.3 Threshold tuning system

A 5-bit, current digital-to-analog converter with an additional sign bit is implemented at the pre-comparator level for fine threshold tuning. The sign bit determines the direction in which the tuning current is steered. Depending on its value, the current is directed to either the left or right branch of the pre-comparator differential pair, thereby allowing the threshold to be either increased or decreased. This mechanism enables precise adjustment of the comparator trigger threshold by digitally controlling both the magnitude and direction of the tuning current. Specifically, a binary-weighted DAC is designed in such a way to provide a maximum current I_{DAC} (the actual current delivered to the pre-comparator load is a fraction of I_{DAC}) determined by the digital code applied to the DAC. This current is sunk in parallel with the pre-comparator load, in one of the two branches of the pre-comparator, depending on the sign bit. Figure 4.2 includes the pre-comparator detail which highlights the presence of two equivalent current generators, each capable of delivering a digitally-controlled fraction of I_{DAC}, in parallel to the precomparator active load.

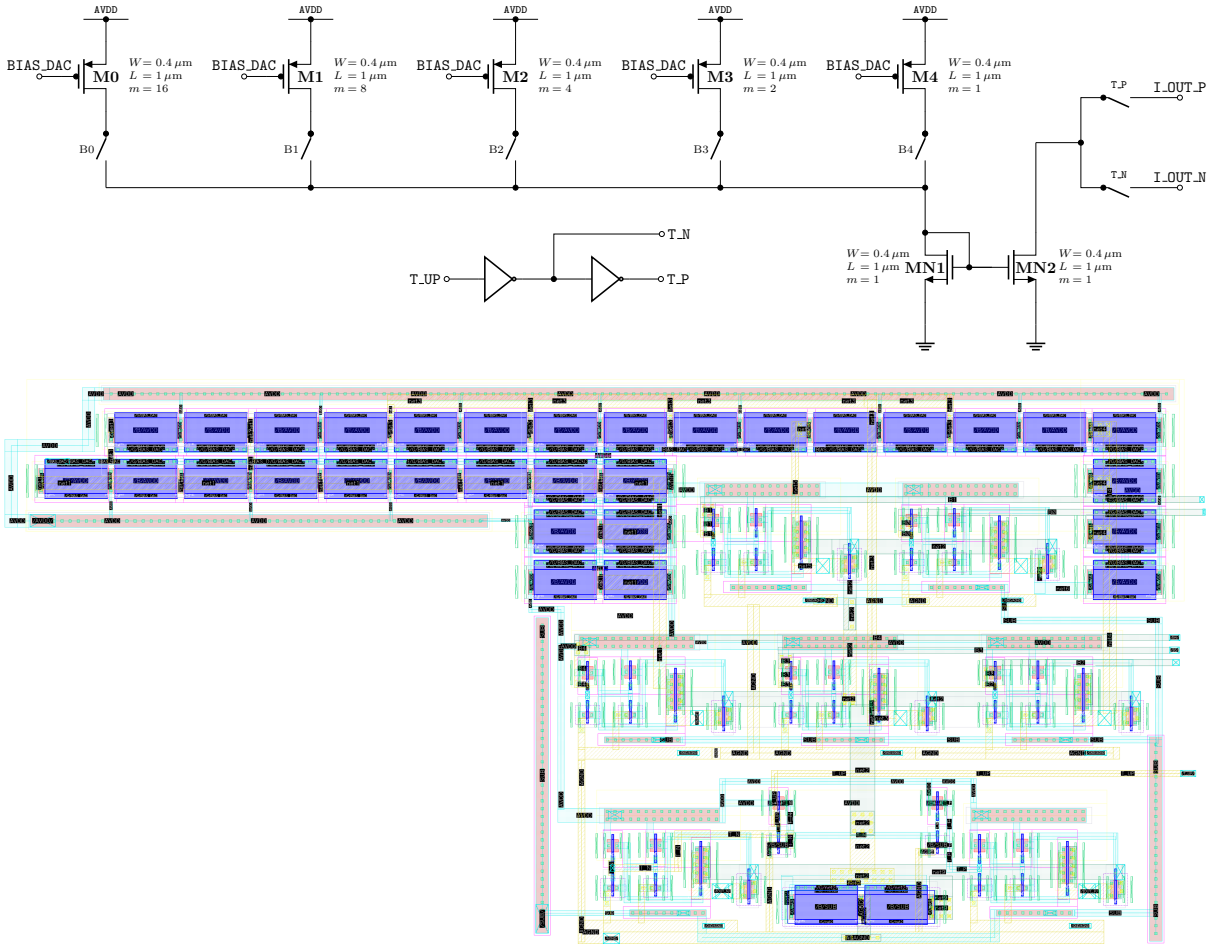


Figure 4.5: Threshold tuning Digital-to-Analog Converter (DAC): (top) schematic diagram showing the binary-weighted PMOS mirrors connected to the pre-comparator load, with control and sign bits for fine threshold adjustment; (bottom) layout view highlighting the compact implementation and routing of the control and current lines. The design choices have been made to ensure best fit with the overall chip architecture.

Figure 4.5 shows the implementation of the tuning DAC. It consists of five PMOS transistors (M0–M4), which mirror the current I_{DAC} coming from a current mirror located in the chip periphery. The set of mirrors is connected via switches to an additional unitary current mirror, which provides the tuning current to the pre-comparator. The transistor sizes are chosen so that each transistor contributes proportionally to the total I_{DAC} current, ensuring fine adjustment of the threshold level. All transistors have the same size, $W = 0.4\,\mu m$ and $L = 1\,\mu m$, but increasing multiplicity. The multiplicities follow a power-of-two progression, starting from the smallest with multiplicity 1 up to the largest with multiplicity 16. Each switch is controlled by a bit of the tuning bus, which selects which and how many transistors to connect to the load. Thus, five configuration bits, denoted as B[0:4], are available with B[0] controlling the smallest (unit) transistor and B[4] controlling the largest one (with multiplicity 16). These bits collectively form a 5-bit binary word, where the digital value represented by the word determines the total current mirrored to the pre-comparator load, and hence sets the DAC output. There is finally a digital control signal, the sign bit `T_UP` (where "T_UP" stands for "Threshold UP"). This bit selects whether the tuning current is connected to the left (positive, IOUT_P) or right (negative, IOUT_N) branch of the pre-comparator, thus digitally selecting the direction of the tuning. This digital control enables precise and programmable adjustment of the comparator threshold by selecting the appropriate combination of transistors.

Threshold calibration algorithm and simulation

The threshold tuning system is crucial for ensuring that the comparator operates uniformly across the entire pixel matrix, compensating for variations in process parameters and temperature. In order to achieve this, a calibration algorithm is needed to automatically adjust the comparator trigger threshold.

The tuning system simulation was performed using the Cadence Virtuoso Analog Design Environment (ADE-XL) and the Ocean scripting tool based on SKILL language. An Ocean script has been developed to allow Monte Carlo simulations and analysis of the comparator threshold dispersion, and is easily integrated into an automated simulation flow for automatic threshold calibration. The code snippet in Listing 4.1 shows the Ocean script written in the SKILL language. This script is used to perform the automatic calibration of the threshold across process variations modeled by Monte Carlo simulation. The script is designed to be run within a Cadence ADE-XL environment and leverages Ocean APIs to programmatically manipulate simulation parameters. The calibration aims to determine, for each pixel/run in the Monte Carlo simulation ,the optimal value of the digital code `TDAC`, that is the 5-bit code that enables the B[0:4] switches, which sets the comparator threshold reducing the dispersion introduced by process variations.

At the beginning, the script inherits the current simulation environment with the `ocnxlLoadCurrentEnvironment` command. It then sets up a `dc` simulation to analyze the `VTH` parameter and save the operating point. The `ocnxlSetCalibration` function enables the calibration context for a single iteration.

The procedure continues with an initial simulation where the `TDAC` value is set to zero. This means that no correction is applied to the precomparator yet. If the comparator output switches before the expected level, i.e., if the threshold is lower than the reference, a voltage offset `T_UP_voltage` is applied to compensate, thus signaling an under-threshold case.

At this point, the script starts an iterative procedure similar to a five-step binary search, aiming to optimize the `TDAC` code value. At each iteration, the `TDAC` value is

updated and the simulation is rerun. The difference between the observed switching point, obtained via the `cross(...)` function, and a reference value of 379 mV is calculated. This reference value corresponds to the DC baseline at the preamplifier output, representing the comparator reference threshold and it is obtained from a previous dc simulation.

This difference is used to determine whether the `TDAC` code should be increased or decreased, depending on whether the simulation result is positive or negative. If the result is positive, the comparator threshold is too high and the `TDAC` code has to be decremented; conversely, if the result is negative, the `TDAC` code is incremented. The process continues until the `TDAC` code converges to the optimal value that minimizes the absolute error between the observed switching point and the reference value. The optimal `TDAC` value is then saved as `TDAC_calibrated`, and the `T_UP_voltage` value is updated based on the simulation result. The script ends by updating the simulation point parameters with the optimized values of `TDAC_calibrated` and `TUP_calibrated`, making them available as outputs in ADE-XL.

The script is run with Monte Carlo simulation settings with 200 iterations, so as to evaluate the comparator threshold dispersion in the presence of process variations, assuming a matrix composed of 200 pixels. The algorithm is executed for each pixel, allowing the calibration of the threshold across the entire matrix. The calibration result returns the optimal value of the `TDAC` code for each pixel, which minimizes the comparator threshold dispersion, the value of `T_UP_voltage` that compensates the comparator behavior in case of under-threshold, and the value of `CalResult` representing the calibration result. The distribution of thresholds obtained from the calibration, as shown in Figure 4.10b, is very narrow and allows achieving a comparator threshold dispersion below 0.4 mV r.m.s., corresponding to about 16 e^- r.m.s. at the front-end input, thus ensuring excellent threshold uniformity across the entire matrix.

4.1.4 Injection system

During the testing phase of the flash-ADC front-end version, emulating the presence of a real silicon detector proved challenging. In that case, a specific configuration for the injection system was implemented by combining settings on the motherboard with adjustments using laboratory instrumentation. Different issues had to be overcome. These included the need for precise timing and synchronization between the injection signals and the readout system, understanding the actual waveform that the preamplifier input would integrate, and accurately estimating the amplitude of the injected signal. For these reasons in this second design, every pixel cell is equipped with an injection system which allows the injection of a known charge into the CSA input. This is useful for testing the front-end channel and for calibrating the comparator trigger threshold, as it allows the injection of a known and reproducible charge, enabling precise adjustment and verification of the comparator's response to defined input signals. The purpose of this block is to generate a controlled current pulse using a square wave, injected through an injection capacitor, in this case $C_{INJ} \approx 7$ fF, at the input of the analog channel , to simulate a charge collection event (i.e., a particle detected by the sensor).

```
;; Montecarlo Calibration Example
;; Inherit test setup from the current point
   ocnxlLoadCurrentEnvironment( ?noAnalysis t)

;; Apply changes if any e.g set a different analysis for calibration run
   analysis('dc ?saveOppoint t ?param "VTH" ?start "300m" ?stop "450m" ?step "1m" )

;; The following command sets the calibration run. It will iherit main
;; montecarlo options for single iteration run.
   ocnxlSetCalibration()

   desVar( "T_UP_voltage" 0 )
   tupResult = 0
   desVar( "TDAC" 0 )
   ocnxlRunCalibration()
   SimResult=cross(VS("/OUT_COMP") 0.6 1 "falling" nil nil nil ) - 379m

   if( SimResult > 0 then
      desVar( "T_UP_voltage" 900m )
      tupResult=900m
   )

   n=16
   TDAC_codes = vector(0 0 0 0 0 0)
   sim_out = vector(0 0 0 0 0 1000000.00)
   for( i 0 4
      desVar( "TDAC" n )
      ocnxlRunCalibration()
      SimResult=cross(VS("/OUT_COMP") 0.6 1 "falling" nil nil nil ) - 379m
      sim_out[i] = abs(SimResult)
      TDAC_codes[i] = n
      printf("TDAC %d \n" n)
      printf("TUP %L \n" tupResult)
      if( tupResult==0 then
            if( SimResult >= 0 then
                     n = n - (2**(4-i))/2
            )
            if( SimResult < 0 then
                     n = n + (2**(4-i))/2
            )
      else
            if( SimResult < 0 then
                     n = n - (2**(4-i))/2
            )
            if( SimResult >= 0 then
                     n = n + (2**(4-i))/2
            )
   )

   if(n<2
      then
      desVar( "TDAC" 0 )
      ocnxlRunCalibration()
      SimResult=cross(VS("/OUT_COMP") 0.6 1 "falling" nil nil nil ) - 379m

      sim_out[5] = abs(SimResult)
      TDAC_codes[5] = 0
   )

   tmp=1000000.00
   for(i 0 5
      if( sim_out[i]<tmp
         then
         tmp=sim_out[i]
         TDAClocal=TDAC_codes[i]
      )
   )
   CalResult = TDAClocal

;; Add this value as ADE XL output so that it can be viewed in outputs window.
;; An output name Calibrated_ParamName will be added for each point.
  ocnxlAddOrUpdateOutput("TDAC_calibrated" CalResult)
  ocnxlAddOrUpdateOutput("TUP_calibrated" tupResult)

;; Update the main simulation environment with the calibrated result.
   ocnxlUpdatePointVariable("TDAC" sprintf( nil "%L" CalResult))
   ocnxlUpdatePointVariable("T_UP_voltage" sprintf( nil "%L" tupResult))
```

Listing 4.1: Ocean script for automatic calibration simulation of the comparator trigger threshold using Monte Carlo simulations. This script aims to simulate and find the level of correction of the Trimming DAC.

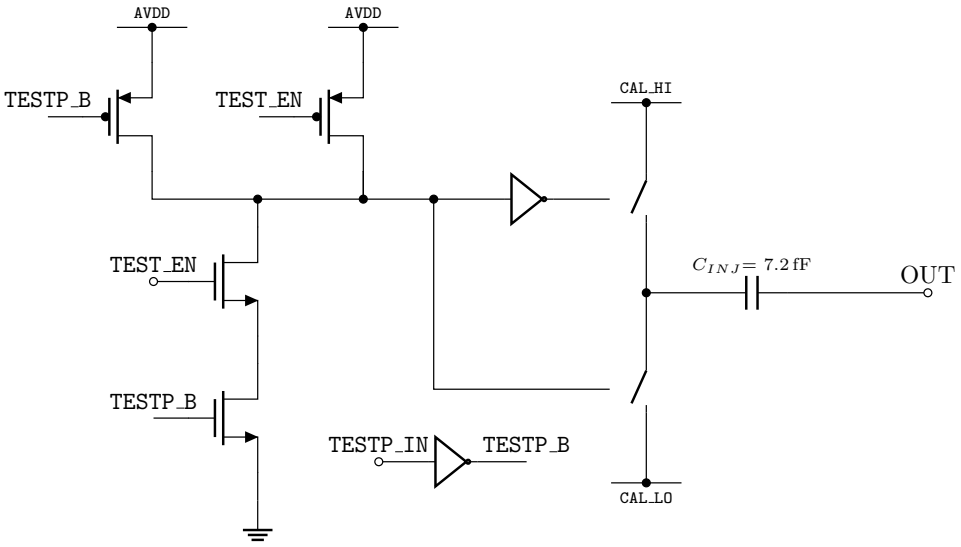


Figure 4.6: Schematic diagram of the injection system. The diagram shows the switching network that selects between two voltage levels (`CAL_HI` and `CAL_LO`) to inject a known charge into the CSA input through the injection capacitor C_{INJ}. The `TEST_P` and `TEST_EN` signals control the switching transistors, allowing for periodic charge injection.

The switched node is connected to one plate of the injection capacitor C_{INJ}. The other plate of the capacitor is connected to the front-end input, which is virtual ground. When the `TESTP_IN` signal switches, it generates a voltage edge (positive or negative) on the injection capacitor. This edge generates a current pulse according to $I = C_{INJ}\frac{dV}{dt}$, where C_{INJ} is the injection capacitance and dV/dt is the time derivative of the voltage across the capacitor. The current pulse has an area equal to the transferred charge, that is,

$$Q_{in} = \int I\,dt = C_{INJ}\Delta V \tag{4.2}$$

where $\Delta V = V_{CAL\_HI} - V_{CAL\_LO}$ is the voltage difference between the two levels generated by the switching.

To estimate the range of the injected charge, the relevant parameters are the injection capacitance $C_{\mathrm{INJ}} = 7$ fF and the maximum voltage step ΔV, which is limited by the chip supply voltage (0.9 V). The actual voltage swing may be slightly lower due to non-idealities such as switch resistance, parasitic capacitances, and charge injection effects. The elementary charge is $q = 1.602 \times 10^{-19}$ C. The maximum injected charge is given by $Q = C_{\mathrm{INJ}} \cdot \Delta V = 7 \times 10^{-15}$ F $\cdot$ 0.9 V $= 6.3 \times 10^{-15}$ C (6.3 fC). The corresponding number of electrons is $N_e = Q/q = 6.3 \times 10^{-15}$ C$/1.602 \times 10^{-19}$ C/e$^-$ $\approx 39337\ e^-$, or approximately 3.9×10^4 electrons. This value represents the ideal maximum; in practice, parasitic effects and process variations may reduce the effective injected charge.

It would be possible to extend the circuit for multiple or dual-level injections, for example by adding a second selectable capacitor to vary the charge range or more sophisticated digital controls to generate test sequences. During the design phase, it was decided to keep the circuit simple and compact, so that it could be easily fabricated and tested.

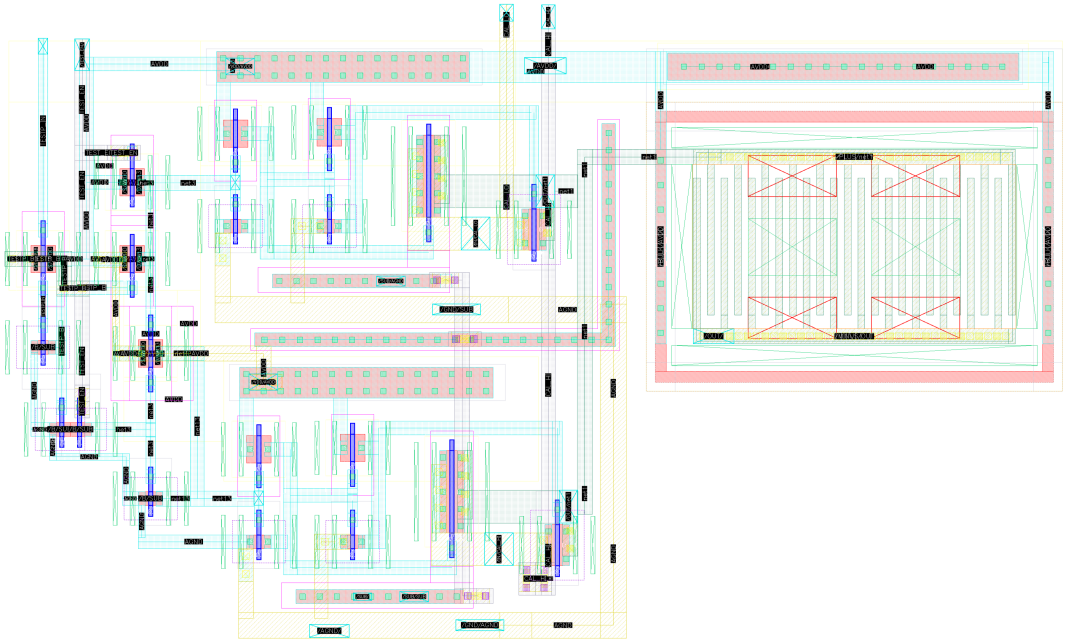


Figure 4.7: Layout picture of the injection system. The layout is designed to be compact and suitable for integration in a pixel matrix structure.

Figure 4.7 shows the layout of the injection system, highlighting the injection capacitor and the switching network used to select between the `CAL_HI` and `CAL_LO` voltage levels. The positioning of the elements is adapted to the available area and the routing constraints of the pixel cell, ensuring that the injection capacitor is placed close to the CSA input to minimize parasitic capacitances and improve signal integrity.

4.1.5 Bias management with the peripheral block

As with previous versions of the front-end, pixel bias management is crucial. For this purpose a peripheral block is integrated in the chip. It provides the necessary bias currents to the various components of the pixel matrix, including the charge sensitive amplifier, comparator, and feedback amplifier, thereby ensuring proper operation and performance. The same approach adopted for the flash-ADC version has been retained. As a matter of fact, the peripheral block includes a set of current mirrors with proper multiplication factors, described later on this section, to generate the required bias levels.

The implemented approach leverages the connection of the current mirror loads to chip pads, which are then connected to external fixed resistors in series with a trimmer; the trimmer is manually adjusted during calibration to finely tune the bias current, which is essential for optimizing the performance of the front-end channels.

The peripheral block provides the following bias levels:

- `PMOS_BIAS`= 20 µA. After a scaling factor of 10:1 in the current mirrors, 2 µA is supplied to the active load of the self-cascode preamplifier (see Figure 4.2), ensuring the correct bias level for optimal preamplifier performance.

- `AMP_BIAS`= 2 µA. With a mirror factor of 10:1, a 0.2 µA current is provided to the tail of the differential stage of the slow feedback operational amplifier.

- `PRE_BIAS`= 15 µA. With a mirror factor of 10:1, a current of 1.5 µA is provided to the tail of the differential stage of the precomparator (the first comparator stage, as shown in Figure 4.2).
- `BIAS_DAC`= 3 µA. After a 160:1 scaling factor, a 0.018 75 µA current is provided to the DAC. This current corresponds to the minimum value set by the smallest DAC bit (multiplicity of 1). Before operation, the matrix must be calibrated to determine the optimal `BIAS_DAC` current, ensuring that the DAC provides sufficient dynamic range for effective threshold correction across all pixels.
- `COMP_BIAS`= 10 µA. With a mirror factor of 10:1, a current of 1 µA is provided to the tail of the second stage of the comparator (see Figure 4.2), ensuring the correct bias level for the second comparator stage.
- `VGG`= 0.5 µA. The pad named `VGG` provides the bias current (mirror factor 10:1) that controls the value of I_F in Figure 4.3, corresponding to the discharge current for the CSA feedback capacitor. At the periphery, a current of 0.5 µA is generated; after the scaling factor, this provides 0.05 µA to the replica of the CSA core amplifier. This bias is crucial for setting the correct discharge current for the feedback capacitor of the CSA, which in turn affects the fall time of the CSA output signal.

As one can note, in this version the discharge of the feedback capacitance is managed through a current mirror control, whereas in previous versions of the front-end—the flash-ADC architecture described in Chapter 3—the discharge was implemented using a direct voltage control at the gate of the feedback transistor. This approach is more robust against process and temperature variations, as the current mirror can track these variations and adjust the discharge current accordingly.

4.1.6 Simulation results

The main simulation results for the front-end, with a focus on noise and threshold dispersion performance, time-walk and ToT characteristics are reported below. The analog performance parameters have been evaluated. For the CSA, these parameters were measured with the bandwidth (BW) limitation introduced by the capacitor C_{BW} connected to the preamplifier output, as discussed in the previous section.

The main outputs of the front-end are visible in Figure 4.8a which shows the CSA response (black waveform) together with the differential pre-comparator (red and blue curves) and comparator (dotted green line) outputs, in response to an input signal of 2000 electrons, for the bandwidth-limited configuration of the front-end operated with a threshold of 800 electrons.

The ToT as a function of the input charge is shown in Figure 4.8b, as a result of a four corner simulations (i.e., simulations performed at the main process corners: typical-typical, slow-slow, fast-fast, and fast-slow, to account for manufacturing variations). For both CSA versions (with and without bandwidth limitation), the ToT (ToT) characteristics exhibit an integral non-linearity close to 2 % over an input charge range up to 15 000 e^-.

Figure 4.9a shows simulation results for the Equivalent Noise Charge (ENC) as a function of the detector capacitance, comparing both limited (solid markers) and regular (blank markers) bandwidth configurations, and including results for two different temperature conditions. Spectre simulations were performed on the extracted view (post-layout)

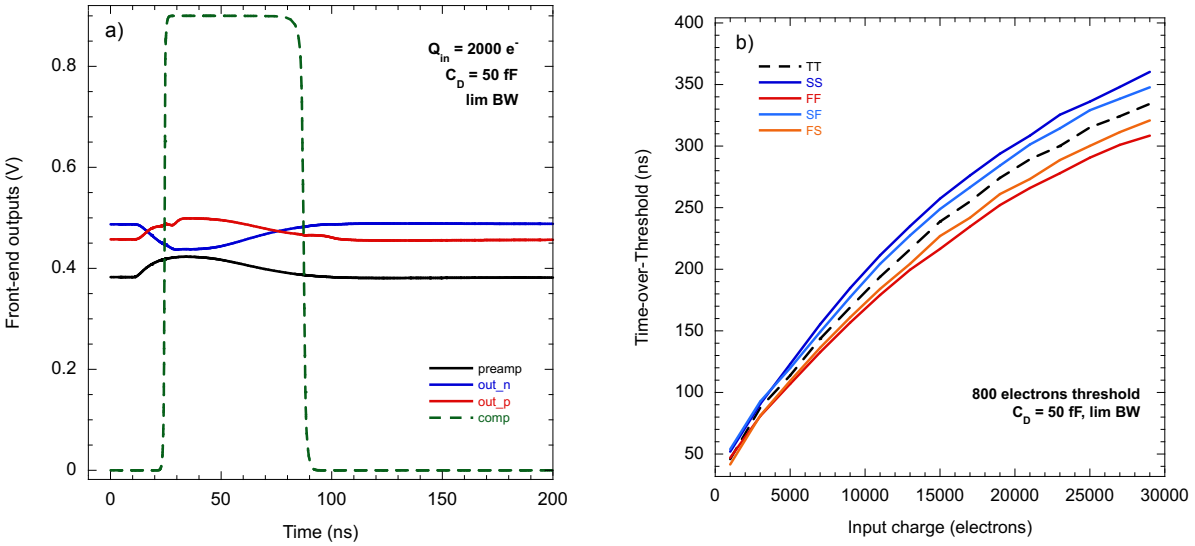
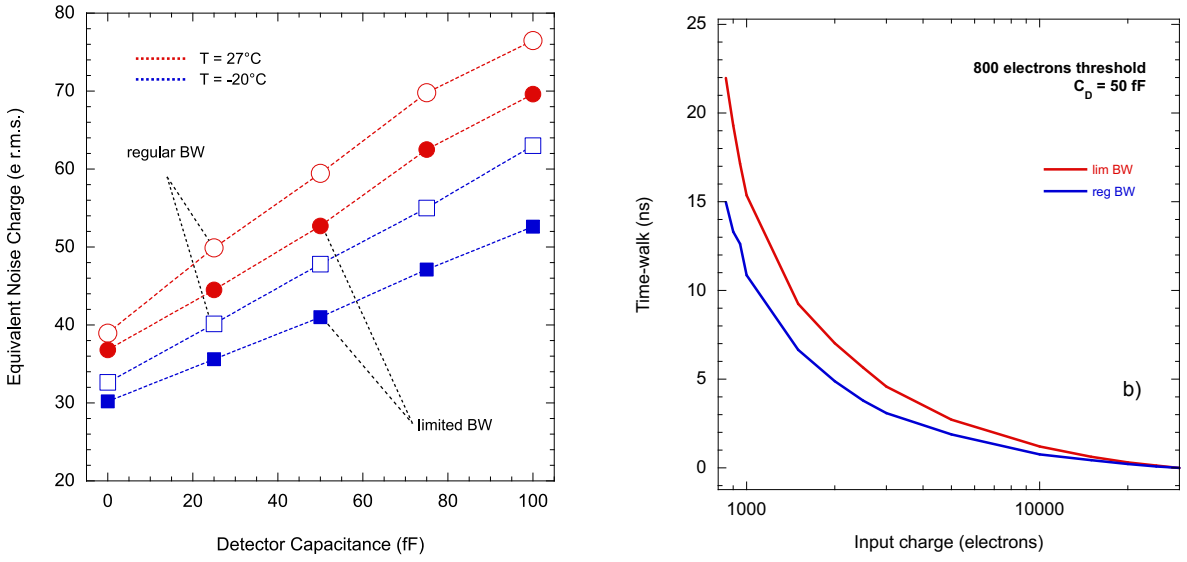


Figure 4.8: (a) Front-end output signals: CSA response (black), differential pre-comparator (red and blue), and comparator (dotted green) for an input signal of 2000 electrons and a threshold of 800 electrons. (b) ToT as a function of the input charge, showing the ToT characteristics for both CSA versions: the regular bandwidth and the bandwidth-limited configuration.

of the front-end channel, in the typical process corner for both room temperature and −20 °C. In the figure, the red curves correspond to room temperature, while the blue curves correspond to −20 °C. An ENC close to 67 electrons r.m.s. was obtained for the regular bandwidth (BW) configuration of the CSA at room temperature, for a detector capacitance of 50 fF; a noise reduction of around 15 % was observed when limiting the bandwidth of the preamplifier. For −20 °C, which is the expected operating temperature for the pixel readout chips in the High Luminosity upgrades of CMS and ATLAS, the ENC is close to 48 e^- r.m.s., for the regular bandwidth version of the CSA connected to a 50 fF detector capacitance. The ENC was found to be well below 100 e^- r.m.s. for both configurations of the CSA, for the maximum simulated value of the detector capacitance, namely 100 fF.

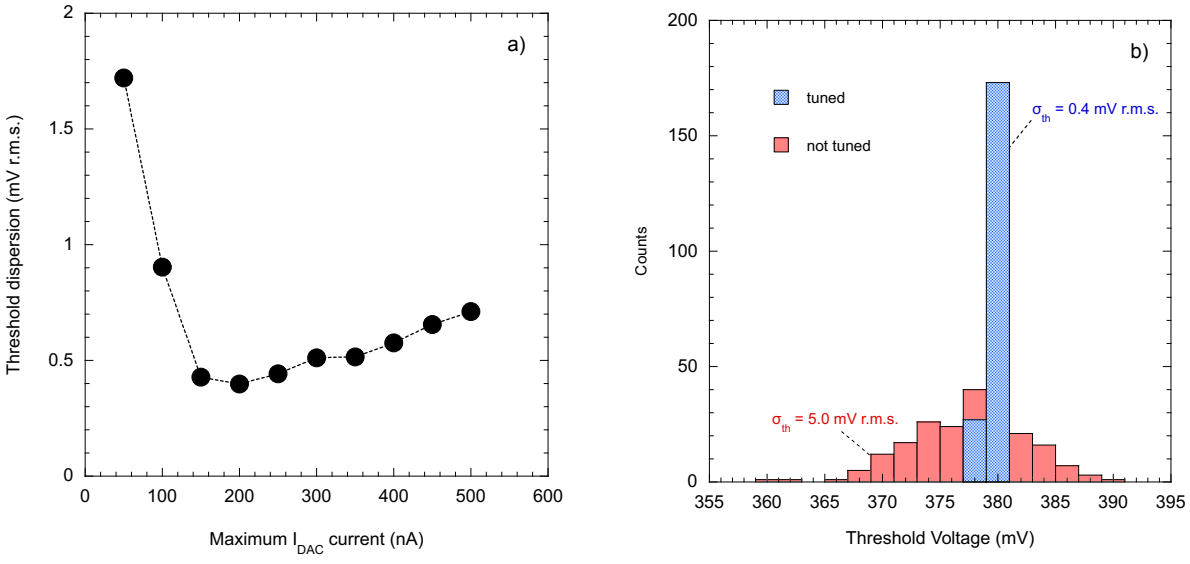
While, on one hand, the bandwidth limitation is beneficial from the noise standpoint, on the other hand it slows down the preamplifier response, resulting in an increased time-walk of the front-end channel. This is shown in Figure 4.9b, where the simulated time-walk is plotted as a function of the input charge for the two configurations of the CSA. Time-walk data is also reported in Table 4.1. Simulations have been performed with a nominal threshold of 800 e^- with a detector capacitance of 50 fF and for different overdrives, defined as the difference between the input charge and the threshold. As expected the time-walk is larger when the preamplifier bandwidth is limited. Nonetheless, even with limited preamplifier bandwidth, the time-walk is found to be smaller than 25 ns (the bunch crossing period at LHC) for a marginal overdrive of 50 e^-.

Threshold dispersion properties of the front-end channel have been investigated by running a set of Monte Carlo simulations, automated through an Ocean script (see Listing 4.1) specifically developed to calibrate and fine-tune the pixel threshold. Figure 4.10a shows the threshold dispersion, as obtained after the tuning, as a function of the maximum



(a) (b)

Figure 4.9: (a) Equivalent noise charge (ENC) as a function of the detector capacitance. (b) Time-walk as a function of the input charge for the two CSA configurations. [120]



(a) (b)

Figure 4.10: (a) Threshold dispersion as a function of the maximum I_{DAC} current delivered by the threshold tuning DAC. (b) Threshold distributions before and after the fine-tuning of the comparator threshold.

Overdrive (e^-)	Limited BW (ns)	Regular BW (ns)
50	21.9	14.9
100	19.3	13.3
150	17.1	12.6
200	15.3	10.8

Table 4.1: Simulated time-walk for an 800-electron threshold.

current delivered by the in-pixel tuning DAC. It is possible to notice that the dispersion, here evaluated at the comparator input (in mV r.m.s.), features a minimum for a maximum I_{DAC} close to 200 nA. Smaller DAC currents lead to an insufficient tuning DAC dynamic range, resulting in a larger threshold dispersion. Similarly, if I_{DAC} is set too large, the resulting dynamic range becomes excessive compared to the un-tuned threshold dispersion, which increases the LSB of the DAC and reduces the tuning resolution. The optimum threshold dispersion is found to be around 0.4 mV r.m.s. and can be converted to the equivalent noise charge (ENC) at the front-end input using the following formula:

$$\mathrm{ENC} = \frac{\sigma_{\mathrm{th}}}{S_Q}$$

where σ_{th} is the threshold dispersion and S_Q is the charge sensitivity of the channel (around 25 mV/ke from circuit simulations).

Figure 4.10b shows the threshold distribution before and after the fine-tuning of the threshold, performed with the optimum value of I_{DAC}. The ratio between the un-tuned and tuned threshold dispersion was found to be close to 12. This results, combined with the promising noise performance, guarantees operation of the front-end down to threshold of 1000 e^-.

4.1.7 The prototype chip

At the time of writing the chip has been designed, fabricated, delivered and is currently undergoing final developments for the data acquisition system that will be used for the characterization of the front-end channel. Testing campaigns under radiation are planned to validate the TID radiation hardness of the front-end channel. The chip is expected to be tested in the final months of 2025 and the first months of 2026. Because these details still have to be managed, the detailed test methodology and experimental results are outside the scope of this thesis and will be presented in future publications. The architectural design of the chip follows the same approach as the one described by the RD53 collaboration, as depicted in the Section 1.3.1. This approach implements a matrix of pixel cells, where each group of four pixel cells forms an analog island surrounded by digital electronics. This structure enables efficient integration of analog and digital circuitry within a dense pixel matrix.

A layout detail of the front-end channel, highlighting the analog island composed of four pixel cells, is shown in Figure 4.11. Each island is then connected to the other islands through a network of analog and digital lines. The analog lines are used to distribute the power supply and bias references, while the digital lines handle control signals and collect data from the pixel cells.

The developed chip integrates a matrix of 32×8 pixel cells, with each pixel measuring 100 µm by 25 µm, resulting in a total chip area of approximately 1500×1700 µm^2. Within

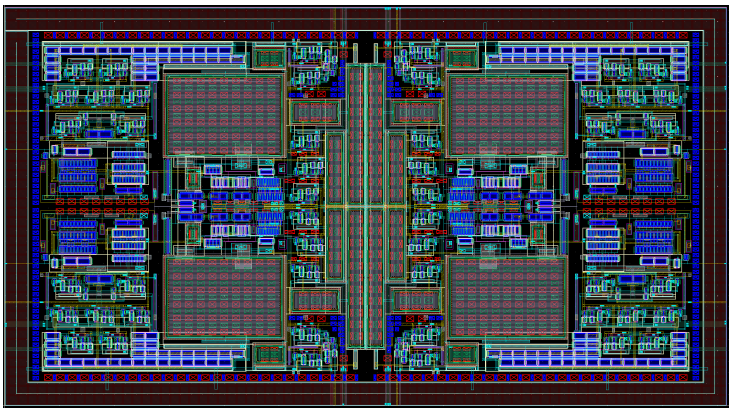


Figure 4.11: Layout detail of the front-end channel for the ToT architecture. The layout is designed to be compact and suitable for integration in a pixel matrix structure.

each pixel, the front-end channel described in the following sections is implemented. In addition to the analog front-end, the design incorporates digital electronics for pixel configuration and data readout, developed in collaboration with the Electronics Laboratory of the INFN Milan section. Bias distribution across the matrix is managed by a network of analog lines and peripheral current mirrors.

The digital electronics provides several key functionalities, including the configuration of the front-end channel, acquisition, readout of pixel data, and external communication. When a hit is detected by the pixel, the comparator triggers and its output is made available on the `HIT_OUT` signal, which is routed to a digital structure. The ToT (ToT) measurement is performed using a 40 MHz clock, while the Time-of-Arrival (TOA) is measured with a 640 MHz clock. Both clocks need to be provided externally and passed through the pads of the chip. Specifically, the ToT counter starts on the rising edge of the `HIT_OUT` signal and stops on its falling edge, whereas the TOA counter starts on the rising edge of the `INJ_PULSE` signal, which is a signal provided to emulate the injection pulse given by a particle crossing the detector, and stops on the rising edge of `HIT_OUT`. The TOA value is stored in an 8-bit counter whereas the ToT value is stored in a 5-bit counter; thus, the output data format consists of 8 bits for TOA and 5 bits for ToT, directly reflecting the width of these counters. To ensure correct synchronization, the TOA counting must remain synchronous with the 40 MHz clock. This requires all flip-flops operating at this frequency to exhibit very low skew. Such a synchronization is crucial for accurate time measurements.

The behavior for short `HIT_OUT` pulses can be summarized as follows: (i) if a `HIT_OUT` pulse is shorter than 25 ns (the period of the 40 MHz clock), the ToT counter may not register a count, resulting in a ToT value of zero. (ii) The ToA counter, running at a much higher frequency (640 MHz), can still capture the precise arrival time of the pulse. (iii) For example, if a `HIT_OUT` pulse lasts only 10 ns, the ToT counter will output zero, while the ToA counter will provide a value greater than one, indicating that a short pulse was detected. This logic allows the system to distinguish between very short pulses and the absence of a signal: if both the ToT and TOA counters output zero, it indicates no signal was detected, whereas if the ToT value is zero but the ToA value is greater than zero, it indicates a very short pulse was detected; this ensures accurate event timing even for signals shorter than the ToT clock period.

In a similar way as done with the zero-deadtime version (described in Chapter 3),

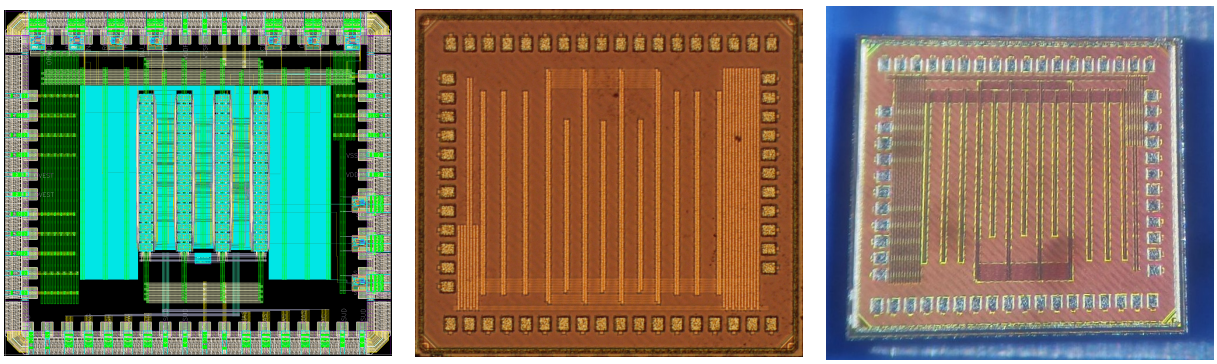
Table 4.2: List of the implemented SPI registers. The table includes the register name, whether it is global or local, its type (read/write), the number of bits, the default value, and any additional useful notes.

Register name	Global/Local	Type	# bits	Default	Note
INJ_PERIOD	global	R/W	8	0xFF	10 μs $\times$ (INJ_PERIOD+1)
INJ_BYPASS	global	R/W	1	1	1: external, 0: internal
INJ_START	global	R/W	1	1	1: to start internal pulses generation
INJ_BURST	global	R/W	8	0x0F	number of pulses
INJ_DUTY	global	R/W	4		650 ns $\times$ (INJ_DUTY+1)
OUT_EN	local	R/W	1	0b001	pixel config bit0
T_UP	local	R/W	1	0b001	pixel config bit1
CAP_CSA_LOAD	local	R/W	1	0b001	pixel config bit2
CAP_50	local	R/W	1	0b001	pixel config bit3
TEST_EN	local	R/W	1	0b001	pixel config bit4
B4-B0	local	R/W	5	0b10000	pixel config bits 9–5 (pixel threshold)
CAP_25	local	R/W	1	0b001	pixel config bit10
TOT	global	R	12		"000000" & valid ToT (1 bit) & ToT value (5 bits)
TOA	global	R	12		"000" & valid ToA (1 bit) & ToA value (8 bits)

additional configurable capacitances are present at the input of the preamplifier. The configuration bits CAP_25 and CAP_50 allow the user to enable or disable an additional input capacitance at the preamplifier input node, emulating increased detector capacitance after irradiation or different sensor types.

Additionally, the chip integrates an SPI controller for configuration and communication. This controller allows for the programming of various registers, including those for ToT and ToA counters, as well as pixel configuration registers. The SPI controller is designed to operate at a maximum frequency of 10 MHz and supports both global and local registers. Table 4.2 lists the SPI registers available in the chip, detailing their names, types, default values, and notes on their functionality.

The full chip diagram, alongside microscope images, is shown in Figure 4.12. Figure 4.13 shows the layout details of the single front-end channel, together with the auxiliary circuitry necessary for configuring the channel input, including the injection capacitance and emulated detector capacitances. The charge sensitive amplifier with its feedback networks, denoted by the large central capacitance, is visible in the center of the im-



(a) (b) (c)

Figure 4.12: (a) Complete layout of the ToT chip, showing the pixel matrix and periphery circuitry. (b) High-resolution optical microscope image of the chip fabricated in 28 nm CMOS technology. (c) Lower magnification optical microscope image showing the entire chip.

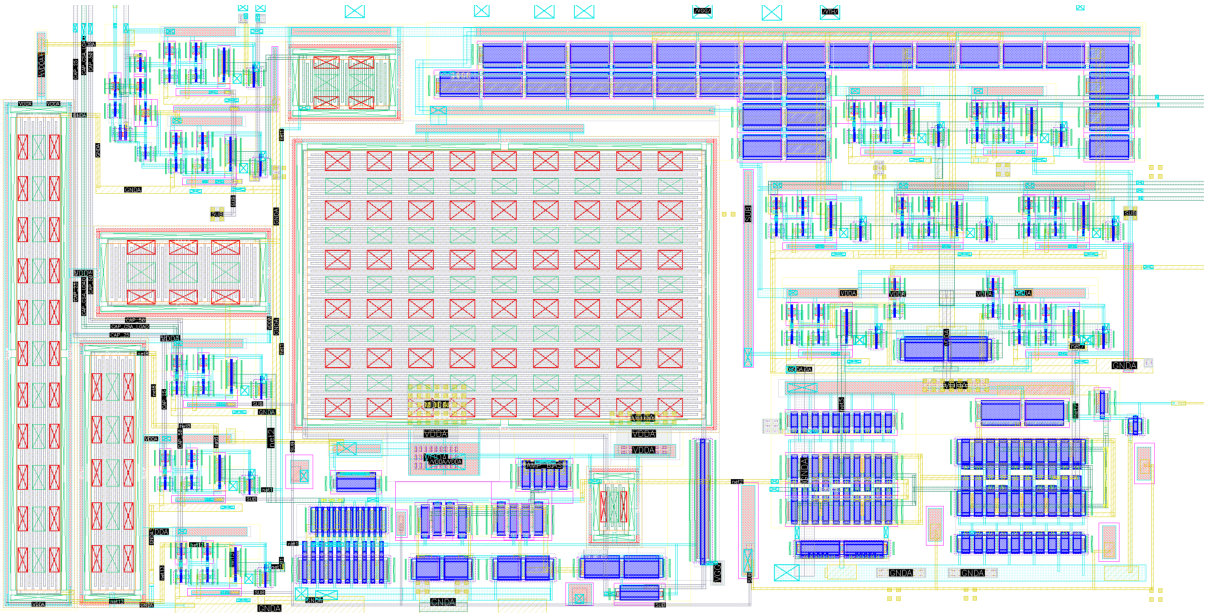


Figure 4.13: Layout detail of the front-end channel for the ToT architecture. The layout is designed to be compact and suitable for integration in a pixel matrix structure.

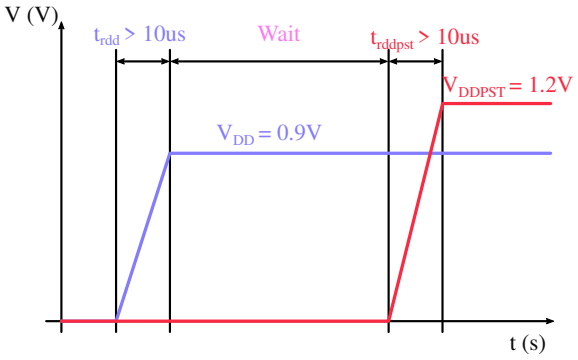


Figure 4.14: Recommended power-up sequence for the ToT chip. The sequence ensures that the bias circuitry reaches its steady state before powering up the IO ring, preventing damage to the transistors. The sequence is crucial for the proper operation of the chip, especially in high radiation environments [121].

age. Finally, on the right side of the image, the pre-comparator and comparator stages are implemented using a common centroid structure, a layout technique that arranges transistors symmetrically to minimize mismatch and improve performance, which is especially important for precise analog circuit operation. Above them is visible the 5-bit trimming DAC, composed of switches and current mirrors. The three pictures side by side in Figure 4.12 show: (a) the complete layout of the chip, (b) the high-resolution optical microscope image of the chip fabricated in 28 nm CMOS technology, and (c) a lower magnification optical microscope image showing the entire chip.

It is possible to see the pixel matrix and the periphery circuitry, including the analog island and the digital electronics, both in the layout image, and also on silicon. The pad ring is clearly visible in all images, providing the necessary connections for the wire bonding process. Its structure includes a single-row staggered radiation-hard IO ring, based on the CERN Library and operating at 1.2 V, to ensure robust operation in harsh environments. The pad map is visible in Figure 4.15, showing the distribution of the bonding pads around the chip. The details of every pad and the related functionality are listed in Table 4.3. It is clear that analog bias and power pads are responsible of the front-end channel operation, while digital pads are mainly used for clocking and to manage the SPI registers. In the table are also listed the power pads named `VDDPST` and `VSSPST`, which are used to power the IO ring, and the pads named `VDDA` and `VSSA`, which are used to power the analog macro. As shown in Figure 4.14, according to the pad documentation, these pads must follow a proper power-up sequence to ensure no damage occurs to the transistors. The driver is implemented with thin-oxide transistors whose maximum operating voltage is 0.99 V (powered by VDD). Since the output stage is composed of an H-bridge with a maximum operating voltage of 1.32 V, an adequate power sequence is required to guarantee that the bias circuitry (supplied by VDD) reaches its steady state before VDDPST is powered up. The power-up sequence must follow the order: (i) power up VDD with a rising time larger than 10 μs; (ii) wait some microseconds to reach the steady state of the bias circuitry; (iii) power up VDDPST with a rise time larger than 10 μs. These settings ensure the proper timing and sequencing of the power supplies of every single channel.

For the testing of this chip, considering that it is not going to be used in an experiment

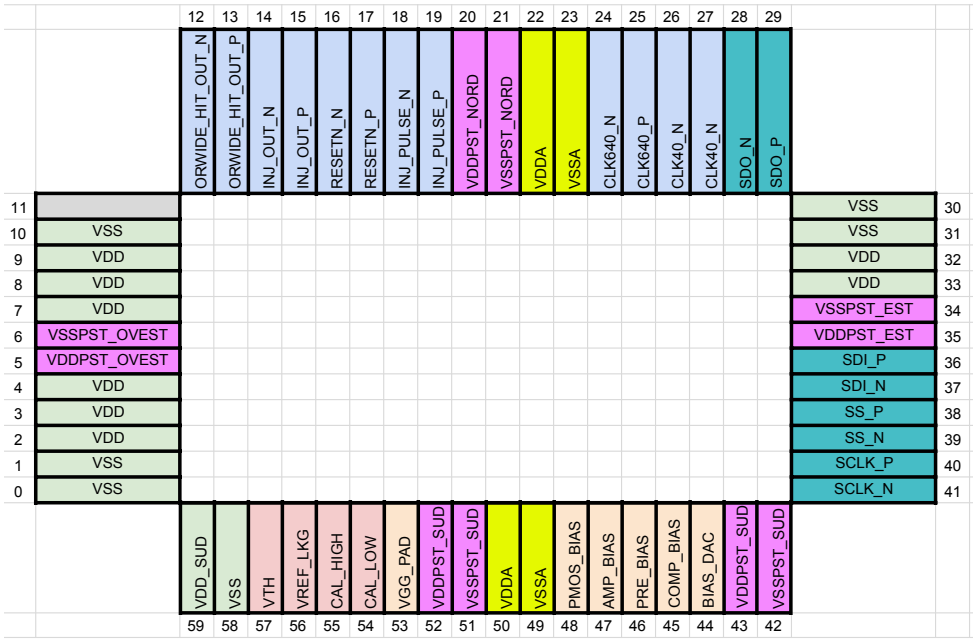


Figure 4.15: Pad ring layout for the ToT chip, showing the arrangement of the bonding pads for wire connections. The pad ring is designed to facilitate the connection of the chip to external circuitry, ensuring proper signal transmission and power distribution.

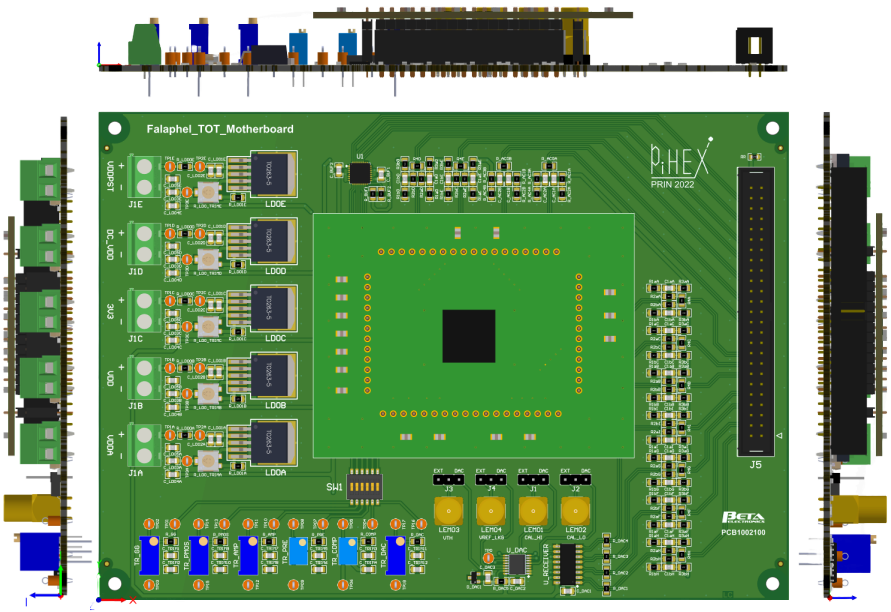


Figure 4.16: 3D rendering of the PCB assembly: the daughter board with the wire-bonded chip is mounted on the motherboard, which provides power, biasing, and signal interfacing to the FPGA.

or a complex embedded system, the power up sequence is going to be managed through the power supply instrumentationavailable in the test setup. The power supply channel will be configured with a slew rate of $50\,000\,\mathrm{V\,s^{-1}}$; for example, for a voltage step of 0.5 V, this corresponds to a rise time of $10\,\mu$s, thus ensuring that the voltage rise time for the required step is greater than $10\,\mu$s.

Table 4.3: List of the implemented IOs. The table includes the IO name, type, number of pads, and notes.

IO name	**Type**	**# pad**	**Note**
BIAS_DAC	Analog	1	Threshold tuning DAC bias
AMP_BIAS	Analog	1	Preamp feedback opamp current bias
VREF_LKG	Analog	1	Bias for leakage compensation feedback
PRE_BIAS	Analog	1	Pre comparator current bias
VTH	Analog	1	Global voltage threshold
COMP_BIAS	Analog	1	Comparator current bias
PMOS_BIAS	Analog		Preamp current bias
VGG_PAD	Analog	1	Preamp feedback discharge current bias
CAL_HIGH	Analog	1	DC calibration level high
CAL_LOW	Analog	1	DC calibration level low
VDDPST	Ring Power	4	VDD for the IO ring
VSSPST	Ring Power	4	VSS for the IO ring
VDDA	Analog Power	4	VDD for the analog Macro
VSSA	Analog Ground	4	VSS for the analog Macro
VDD	Digital Power	4	VDD for digital
VSS	Digital Ground	4	VSS for digital and for substrate (?)
INJ_PULSE	LVCMOS12	1	Start signal to the injection
SPI	LVCMOS12	4	
RESETN	LVCMOS12	1	Global active-low reset
CLK40	SLVS	2	Clock @ 40 MHz for the ToT count
CLK640	SLVS	2	Clock @ 640 MHz for the ToA count
ORWIDE_HIT_OUT	SLVS	2	Or-wide of all HIT_OUT pixels
INJ_OUT	SLVS	2	Internal injector signal sent out

Based on the pad ring layout and the available IOs, the printed circuit boards (PCBs) required for wire-bonding the chip and for system integration have been designed. Figure 4.16 presents a 3D rendering of the boards, both designed as part of the duties for this thesis, illustrating the placement of the chip and the main connectors. On the left side is visible the five groups of LDO structures that manage the power supply for the analog and digital domains. On the bottom side, blue trimmers and resistors are configured to tune the peripheral bias blocks of the chip. Then there are the four LEMO connectors

together with the DAC for the management of calibration and threshold voltages. On the top and right side, the adapting circuitry necessary for communication between the chip and the FPGA, as well as SLVS/LVDS signal interfacing, is present.

An FPGA is responsible for chip configuration, data processing, and communication with a software interface on a computer for data export and analysis. This setup enables data acquisition and characterization of the front-end channels. The firmware running on the FPGA is under development and will be tailored to the specific requirements of the ToT chip.

4.2 X-ray imaging architecture

In the context of the *PiHEX* project, a novel approach for X-ray imaging instrumentation is being developed. The necessity of new techniques for X-ray detection and imaging has become increasingly important due to the growing demand for high-resolution imaging in various scientific and medical applications. In this field, electronics is both the enabling factor and the limiting one. As a matter of fact, the performance of X-ray detectors is heavily influenced by the quality of the associated electronics, especially on the detector readout side. Overall, modern X-ray imaging systems must achieve both high dynamic range and high signal-to-noise ratio, especially for demanding applications such as medical imaging, Free Electron Lasers (FELs), or X-ray Photon Correlation Spectroscopy (XPCS). These applications require the detection of signals ranging from single photons to thousands of simultaneous photons within each pixel.

Facing these requirements, approaching them with a single fixed-gain amplifier cannot cover the required dynamic range. Therefore, the front-end should incorporate a system to implement an automatic gain switching mechanism, dynamically adjusting sensitivity according to the signal intensity.

State of the art front-ends such as DSSC, AGIPD, or JUNGFRAU, have demonstrated the effectiveness of advanced readout techniques in achieving high performance in X-ray imaging applications. These systems typically employ advanced signal processing algorithms and hardware architectures to optimize the detection and readout of X-ray signals.

The work developed during this thesis aims to enhance the performance of X-ray imaging systems by designing an analog front-end for silicon pixel detectors that implements a ToT method featuring a bi-linear input-output characteristic. In this architecture, local counters for each pixel measure the time duration for which the signal exceeds a set threshold, ensuring that only the relevant pixel is processed.

An adaptive gain switching mechanism is implemented to automatically select the appropriate gain setting based on the input signal level. This ensures both high sensitivity and a wide dynamic range, reducing the risk of saturation at high photon fluxes. Two operative regions are foreseen: a high-gain mode for weak signals (from 1 to 100 photons) and a low-gain mode for large signals (from 100 to around 4×10^3 photons).

This architecture implements the ToT technique by using an adjustable CSA feedback current whose value depends on the preamplifier signal amplitude itself (hence, on the amount of the charge delivered by the sensor).

The detector is assumed to be a silicon pixel, generating a charge proportional to the energy of each incoming photon. The design took into account a typical parasitic input capacitance of 100 fF for each pixel.

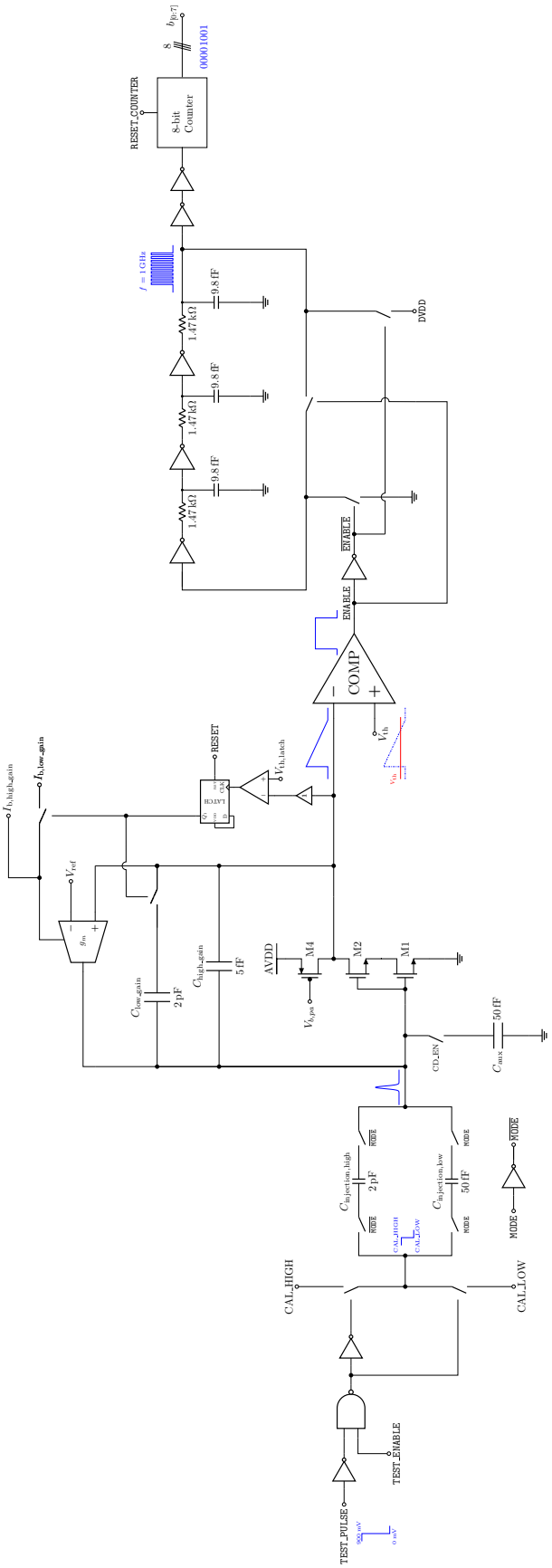


Figure 4.17: Full schematich architecture of the ToT channel for X-ray imaging applications. The architecture is based on a CSA, a comparator, an oscillator and a counter. The output of the counter is the ToT measurement.

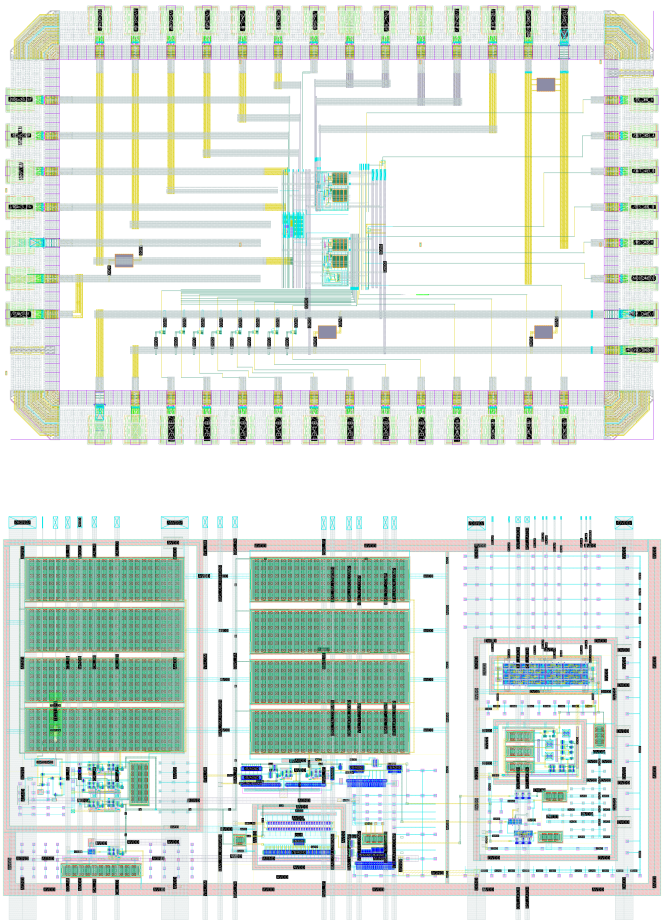


Figure 4.18: (Top) Layout of the full chip version for the bilinear ToT channel, with a size of 1440 µm × 960 µm. (Bottom) Layout of the analog front-end, with an area of around 110 µm × 60 µm.

During simulations, the target experiments considered for this channel architecture are the ones that work with photons in the range of 9 keV, with a defined bunch train structure, such as the European XFEL, FERMI, or LCLS-II. In typical FEL experiments, such as those at the European XFEL, the time interval between two consecutive bunch trains is actually quite large (on the order of 100 ms). Instead, the relevant timing reference for the integration window is set by the repetition rate of the X-ray pulses within a bunch train, which is typically around 4 MHz–5 MHz. Therefore, a maximum signal-processing time of 250 ns is chosen to match the pulse repetition rate, ensuring that the front-end can process each X-ray event within the available time window. The timeframe operation can be adjusted by modifying analog parameters in the design, such as the discharge current for the preamplifier feedback capacitances.

The designed front-end channel, integrated in a 1.4 mm × 1 mm prototype chip submitted in June 2025, aims to demonstrate the feasibility of the bilinear ToT method in a 28 nm CMOS process. That is why the proof-of-concept chip submitted for fabrication includes only two versions of the same channel. One version exposes the output of the preamplifier, with its signal driven by buffers connected to the chip PADs. The other version allows the study of the entire channel.

The schematic of the full channel of this silicon pixel detector front-end is shown in Figure 4.17. It can be divided into three main blocks: (i) the injection system that aims to emulate the presence of a real silicon detector, which enables calibration and characterization of the front-end; (ii) the analog front-end composed of a charge sensitive amplifier with an automatic gain switching system and a comparator; (iii) the mixed-signal section, which is responsible for ToT counting. The output of this channel is an 8-bit digital word representing the ToT measurement.

The layout of the full chip is shown in Figure 4.18-top. In the center of the area, the two versions of the channel are placed, with the bias management circuitry. In the bottom part of the layout digital buffers have been integrated to drive the output signals to the chip PADs. The total area of the chip is 1440 µm × 960 µm, while the front-area area is about 110 µm × 60 µm. Figure 4.18-bottom shows the layout of the analog front-end, composed of the three main section described above. On the left side is the injection system, in the center the CSA with the comparator, and on the right side the digital section with the ring oscillator and counter. The approach used for isolation between the analog and digital sections is based on the use of guard rings and deep n-wells. In particular the digital section is placed in a deep n-well, which is then surrounded by a guard ring connected to the positive supply voltage. Instead the analog section is surrounded by a guard ring connected to ground, on the substrate of the chip. The choice to isolate the digital section in a deep n-well is driven by the need to minimize the coupling of digital switching noise into the sensitive analog front-end. Digital circuits, especially those operating at high speeds such as the ring oscillator, can generate significant noise due to rapid switching of signals. Moreover, the counter can also contribute to this noise, caused by the flip-flops triggering and switching. This noise can couple into the substrate and affect the performance of nearby analog circuits.

In the following sections the three main blocks of the front-end channel are described in detail.

4.2.1 The injection system

As from the lesson learnt from the development of the zero-deadtime front-end version (Chapter 3), a solution similar to the one implemented in the HEP ToT version of the front-end, and described in the Section 4.1.4, has been implemented for the charge injection circuit. Differently from the HEP ToT version, this front-end channel needs to include a system to switch between two gain modes, high-gain and low-gain, to cover a wide dynamic range. Therefore a single injection capacitance is not sufficient, and a dual-capacitance injection system has been implemented.

Figure 4.19 shows the schematic representation of the injection system, which features two selectable injection capacitors to accommodate a wide range of input signals: a $C_{injection,low} \approx 50\,\text{fF}$ capacitor for high-gain mode and a $C_{injection,high} \approx 2\,\text{pF}$ capacitor for low-gain mode. The selection between these two capacitors is managed by a digital `MODE` signal. When `MODE` is high, the 50 fF capacitor is enabled and the 2 pF capacitor is disconnected; when `MODE` is low, the 2 pF capacitor is enabled and the 50 fF capacitor is disconnected. This switching is implemented through a network of switches controlled by the `MODE` signal and its complement, obtained through a simple inverter.

The injection is performed by applying a square wave (`TEST_PULSE`) to the selected injection capacitor, with the process enabled by the `TEST_ENABLE` signal. The voltage swing is defined by two DC reference levels, `CAL_HIGH` and `CAL_LOW`. When a transition

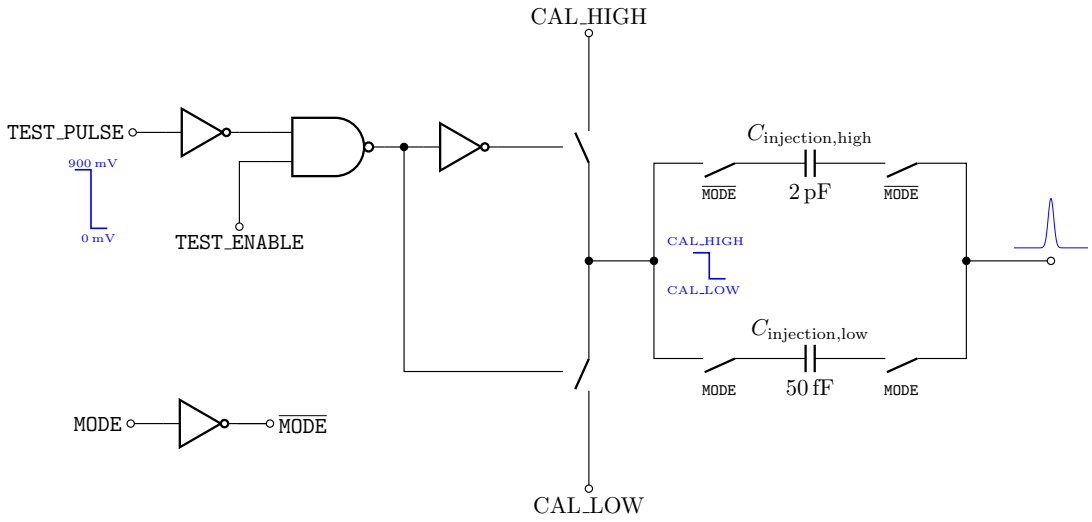


Figure 4.19: Schematic representation of the dual-capacitance injection system for the ToT channel. The system is designed to emulate the behavior of a real silicon detector, allowing for accurate calibration and characterization of the front-end.

occurs on TEST_PULSE, the selected injection capacitor transfers charge to the input of the analog front-end, generating a current pulse. The total injected charge is given by

$$Q_{in} = C_{INJ} \cdot (V_{CAL\_HIGH} - V_{CAL\_LOW}), \tag{4.3}$$

where C_{INJ} is either 50 fF or 2 pF, depending on the selected mode. This dual-capacitance approach allows precise emulation of a wide range of signal amplitudes for calibration and characterization of both gain modes in the front-end. To better understand the capabilities of the injection system, let us consider the range of charge that can be delivered in both gain modes. The total injected charge is determined by the selected injection capacitance and the voltage difference applied across it, as described by Equation 4.3. For this design, the minimum value for CAL_LOW is set to 0 V, while the maximum value for CAL_HIGH is 900 mV. This allows the injected charge to be swept from zero up to a maximum value, depending on the selected mode.

In high-gain mode, where the injection capacitance is $C_{INJ} = 50\,\text{fF}$, the maximum injected charge is $Q_{max} = 50\,\text{fF} \times 0.9\,\text{V} = 45\,\text{fC}$. To put this into perspective, a single 9 keV photon absorbed in silicon generates approximately 2500 electrons, corresponding to about 0.4 fC of charge. Therefore, the high-gain mode allows the injection of up to roughly 112 photons. This mode is thus well suited for calibrating and characterizing the front-end response to low signal levels, as expected in single-photon or few-photon detection scenarios.

By switching to low-gain mode, the injection capacitance increases to $C_{INJ} = 2\,\text{pF}$, resulting in a much larger maximum injected charge of $Q_{max} = 2\,\text{pF} \times 0.9\,\text{V} = 1.8\,\text{pC}$. Using the same conversion, this corresponds to approximately 4494 photons. This extended range enables the front-end to be tested and calibrated under conditions simulating high photon flux, as encountered in demanding X-ray imaging applications. A finer understanding can be obtained by considering the charge injected per millivolt of voltage swing. In high-gain mode, each mV step corresponds to 0.05 fC, or approximately 0.125 photons at 9 keV. In low-gain mode, each millivolt injects 2 fC, equivalent to roughly 5

photons. These values are useful for estimating the calibration granularity of the system, particularly when the voltage step levels are defined by a digital-to-analog converter (DAC).

It is important to note that these calculations are based on ideal component values. In practice, factors such as the tolerance of the injection capacitors, charge injection and feedthrough from the switches, and the actual voltage swing across the capacitor (which may be affected by driver strength and switch on-resistance) will introduce some variation. If the resolution of the DACs generating `CAL_HIGH` and `CAL_LOW` is known, it is possible to further refine these estimates and determine the minimum resolvable injected charge in terms of equivalent photons for each mode.

For what concerns the `TEST_PULSE` signal, it can be generated by a dedicated pulse generator circuit that produces a short voltage pulse with a defined amplitude and duration or by using the GPIO output from an FPGA or microcontroller. The frequency of this signal can be in the order of kHz. An important factor is that at every edge of the signal, the system injects a certain amount of charge, either negative or positive, depending on the polarity of the `TEST_PULSE` transition. Therefore, the pulse generator should be designed to produce a pulse with a low duty cycle, ensuring that the system has sufficient time to recover between injections. Alternatively, the frequency can be set low enough to allow for proper settling of the system.

4.2.2 The analog front-end

The analog front-end, namely the very first stage in the signal processing chain, responsible for amplification and processing before signal digitization, consists of the charge sensitive amplifier and the comparator stages. The schematic representation of the preamplifier is shown in Figure 4.20.

As shown, it features a single gain stage with a feedback network composed of two parts. The first part of the feedback includes a 5 fF capacitor in parallel to a transconductor amplifier responsible for providing the discharge current of the capacitor itself, which is set by the $I_{\mathrm{b,high\_gain}} \approx 300\,\mathrm{nA}$ current reference. The transconductor operates with a reference voltage of $V_{\mathrm{ref}} = 450\,\mathrm{mV}$, which sets the DC operating point at the output node of the gain stage. The second part consists of a source follower that buffers and decouples the output signal of the gain stage. This buffered signal is then fed to a comparator, which compares it to a $V_{\mathrm{th,latch}}$ threshold; when the threshold is crossed, the comparator triggers a latch that switches the feedback network, thereby changing the gain mode of the amplifier. In particular, if the latch fires, then the switches controlling the auxiliary feedback path (as shown in Figure 4.20) are closed, connecting an auxiliary 2 pF capacitor in parallel with the $C_{\mathrm{high\_gain}}$ capacitance. Additionally, a second current reference is added to the transconductor, increasing the current by $I_{\mathrm{b,low\_gain}} \approx 6.8\,\mu\mathrm{A}$, therefore increasing the discharge current of the CSA feedback capacitance.

When a signal exceeds the $V_{\mathrm{th,latch}}$ threshold, the system transitions to low-gain mode, allowing it to handle larger signals without saturation. This is made possible thanks to the charge redistribution between the two feedback capacitors and the increased discharge current, which together effectively reduce the gain of the amplifier.

The gain stage is implemented using the same self-cascode architecture described in the previous section for the ToT for HEP experiments. However, in this case, considering the gain necessary to integrate such large signals from the photon detectors, the design must account for the increased capacitance and current levels. The active load

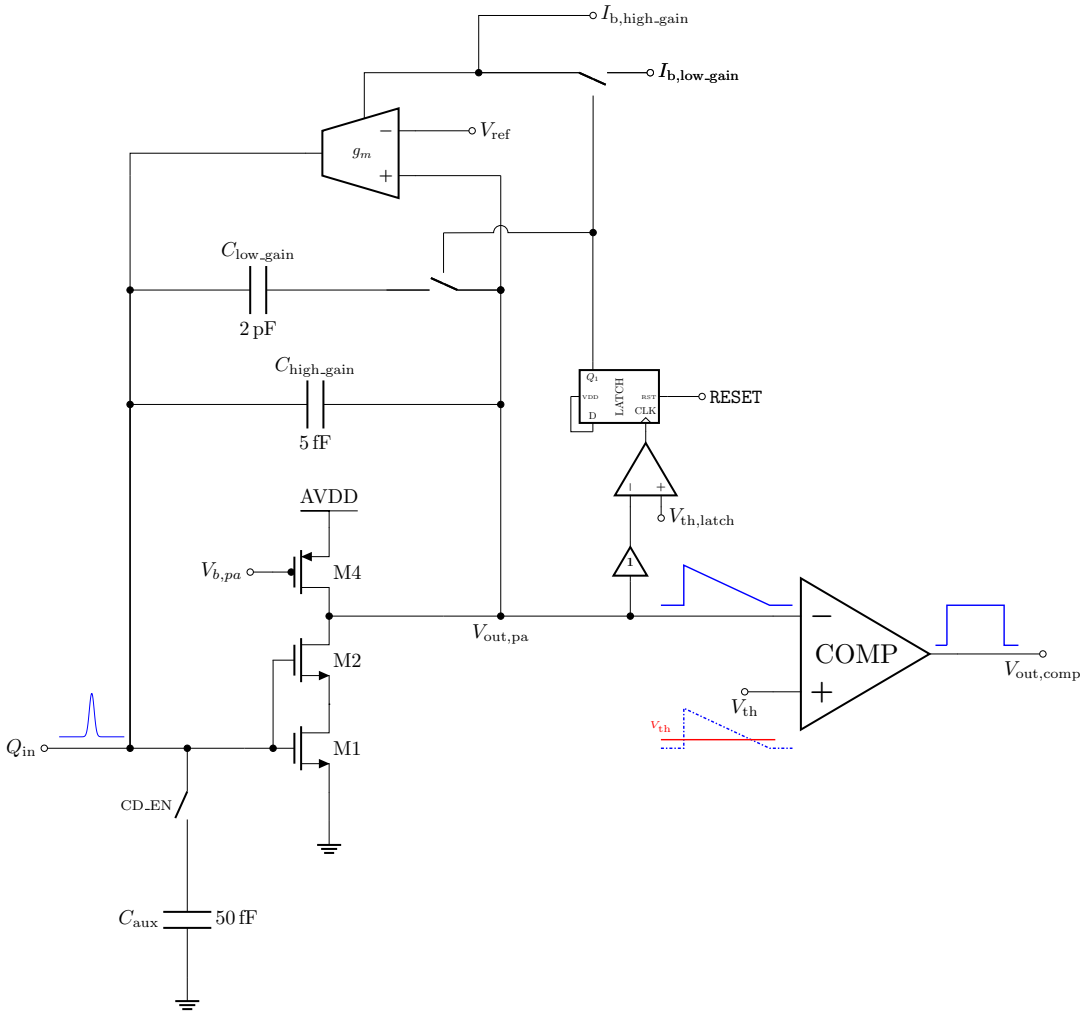


Figure 4.20: Schematic representation of the analog front-end for the ToT channel. The front-end includes a charge sensitive amplifier with automatic gain switching feedback and a comparator to process the input signal.

of the self cascode is biased in order to guarantee at least a current of 350 µA flowing through the input transistor. The bias current is selected as a design trade-off between noise performance, speed, and power consumption. Increasing the bias current enhances the transistor transconductance, thereby reducing the input-referred noise and improving the bandwidth, at the expense of higher static power dissipation. The input device, features a $W/L = 4.5\,\mu m/200\,nm$, with 36 fingers. The cascoded device M_2 has a $W/L = 6\,\mu m/50\,nm$, with 12 fingers. The active load device M_3 has a $W/L = 250\,nm/300\,nm$, with a multiplicity of 50. The use of multiple fingers primarily improves the matching and layout density of the device, while the input capacitance is determined by the total gate area.

Table 4.4 summarizes the open loop analysis of the gain stage across process, voltage, and temperature (PVT) corners. In the typical-typical (TT) corner, the gain bandwidth product is 34.5 GHz, the open loop gain is 28.9 dB. Figure 4.21 shows the open loop gain plots for all PVT corners.

Post-layout simulations show that in high-gain mode, the Signal to Noise Ratio (SNR) is about 10, with the gain stage input device being the main contributor to the noise.

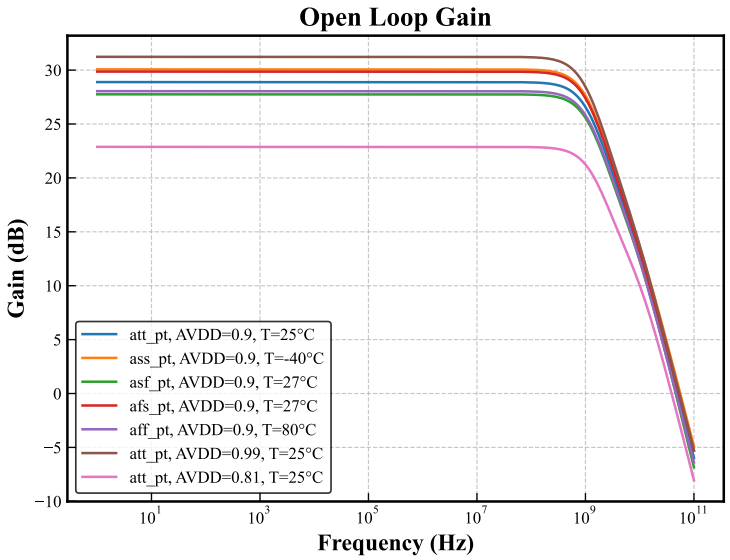


Figure 4.21: Open loop gain of the gain stage across process, voltage, and temperature (PVT) corners.

	Open Loop Gain (dB20)	Open Loop GBW
TT	28.9	34.5 GHz
SS	30.1	34.7 GHz
FS	27.8	34.5 GHz
SF	29.9	34.1 GHz
FF	28.1	34.3 GHz
TT_VDD+10%	31.2	32.9 GHz
TT_VDD-10%	22.9	34.4 GHz

Table 4.4: Gain stage simulation results across process, voltage, and temperature (PVT) corners.

The equivalent noise charge is approximately 242 electrons r.m.s. in the Typical-Typical corner. This result is compatible with the Poisson limit for which, in the case of a single 9 keV photon detection, the ENC should be below 250 electrons. Table 4.5 summarizes the noise performance metrics for the CSA in different corners, and the column dedicated to the ENC shows that this limit is met in all the simulated corners.

In low-gain mode the SNR improves to approximately 20. This improvement can be attributed to the fact that the input signal is much larger (hundreds of photons instead of a single one). In general, both the increased feedback capacitance and higher discharge current tend to increase the equivalent noise charge. However, since the signal amplitude grows much faster than the noise, the overall SNR is higher in low-gain mode. This trade-off is typical in front-end design for X-ray imaging: extending the dynamic range by lowering the gain and increasing the feedback capacintance allows the system to process large signals, but at the cost of higher noise. The design ensures that, even with increased ENC, the SNR remains sufficient for accurate measurement in the intended signal range. Table 4.6 summarizes the noise performance metrics for the CSA in different corners in low-gain mode. The ENC in this case is significantly higher, around 34.6k electrons r.m.s. in the Typical-Typical corner, which is expected due to the larger input signals being

processed in this mode.

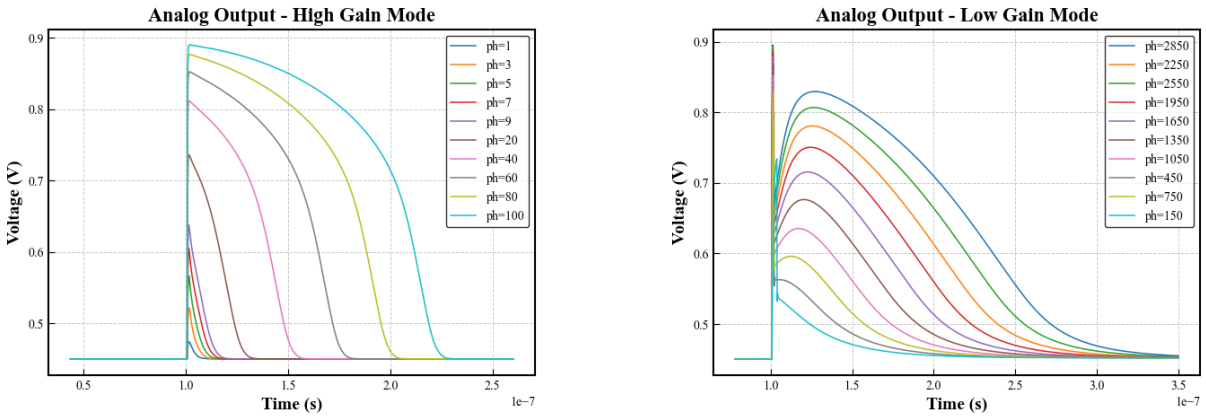
	SNR	ENC (e- r.m.s.)	Total Summarized Noise (mV)	Output Amplitude (mV)
TT	10.3	242.1	2.32	24.04
SS	11.6	214.9	2.28	26.64
FS	10.3	242.3	2.34	24.19
SF	10.2	244.7	2.32	23.76
FF	9.5	264.2	2.34	22.14
TT_VDD+10%	10.6	236.4	2.42	25.54
TT_VDD-10%	10.1	248.3	2.12	21.32

Table 4.5: Noise performance metrics for the High gain mode for the CSA in different corners. The simulations has been carried out considering a single photon input ($Q_{\text{in}} = 2500e^{-}$).

	SNR	ENC (e- r.m.s.)	Total Summarized Noise (mV)	Output Amplitude (mV)
TT	21.64	34.66k	1.43	30.99
SS	27.42	27.35k	2.15	58.98
FS	23.05	32.54k	1.38	31.97
SF	19.98	37.53k	1.35	27.08
FF	29.14	25.74k	1.05	30.55
TT_VDD+10%	24.42	30.71k	1.20	29.37
TT_VDD-10%	22.28	33.67k	1.55	34.42

Table 4.6: Noise performance metrics for the Low gain mode for the CSA in different corners. The simulations has been carried out considering a 100 photon input.

As one can see from Figure 4.22, the output signals in high-gain and low-gain modes exhibit different characteristics, allowing the system to adapt to varying input signal conditions. As mentioned, the signal is processed in high-gain mode by default. The feedback automatically detects, depending on the setting of $V_{\text{th,latch}}$, when the output signal exceeds a certain threshold, indicating that the input signal is too strong for the high-gain mode. At this point, the system switches to low-gain mode by enabling the additional feedback capacitor and increasing the discharge current. This transition helps to prevent saturation and maintain linearity in the response of the amplifier. The proper value of the current references must be chosen to ensure that the output signal returns to baseline in 250 ns, which is the window time frame chosen as requirement. Another important thing to take care of is that as soon as the changing in the gain mode occurs, the signal from the preamplifier can undershoot. Figure 4.22-b shows the output signals in low-gain mode. The curve in lightblue, referring to an input signal of 150 photons, shows a small undershoot just after a main, positive-going spike, near after 1 ns, at a voltage of about 530 mV. If the undershoot of the signal is too large, there is the risk that the signal crosses the voltage threshold of the ToT comparator, causing false triggering and erroneous ToT measurements. This effect can be mitigated by carefully selecting the discharge current values, as well as by optimizing the comparator threshold and bandwidth to avoid false triggers due to undershoots.



(a) (b)

Figure 4.22: Output signals from the charge sensitive preamplifier in high-gain (a) and low-gain (b) modes, illustrating the channel's response to weak and strong input signals as discussed in the preceding section.

The comparator stage is shown in Figure 4.23. It is designed to be minimal and efficient, composed of a simple differential pair with active load followed by a cascade of three inverters to consolidate the output levels. The same architecture has been implemented for both the comparator that discriminate between high-gain and low-gain modes and the comparator that drives the ToT counting system.

The whole analog section, including the CSA, the comparator, and the associated biasing circuitry, requires a total power consumption of approximately 1.2 mW per pixel from a 0.9 V supply voltage. This power budget is acceptable for pixel-level integration in high-density arrays, specifically for the intended application in X-ray imaging systems. In fact, in such systems, the machine structure is typically designed to accommodate the power dissipation of the front-end electronics, ensuring that thermal management and overall system performance are not compromised. The pixel matrix is expected to operate within a controlled environment, where cooling solutions, such as liquid cooling systems, thermoelectric modules, or forced air convection, can be implemented to manage the heat generated by the electronics, as commonly adopted in similar high-density pixel array systems.

4.2.3 The mixed-signal section

This last block is responsible for the ToT counting and digital output generation. It measures the time duration for which the signal from the comparator remains above a defined threshold, which is indicative of the input signal's amplitude. The implemented approach uses a ring oscillator to generate a 1 GHz clock signal, which is fed to an 8-bit counter while the comparator output remains high. The schematic diagram in Figure 4.24 illustrates the main blocks of the ToT counting system, including the ring oscillator that generates the clock signal and the 8-bit counter that records the duration of the comparator output pulse.

The chosen frequency corresponds to a time resolution of 1 ns, which is sufficient to capture the dynamics of the input signals expected in the target applications. This design choice facilitates also the implementation of the counter: given a time frame of 250 ns,

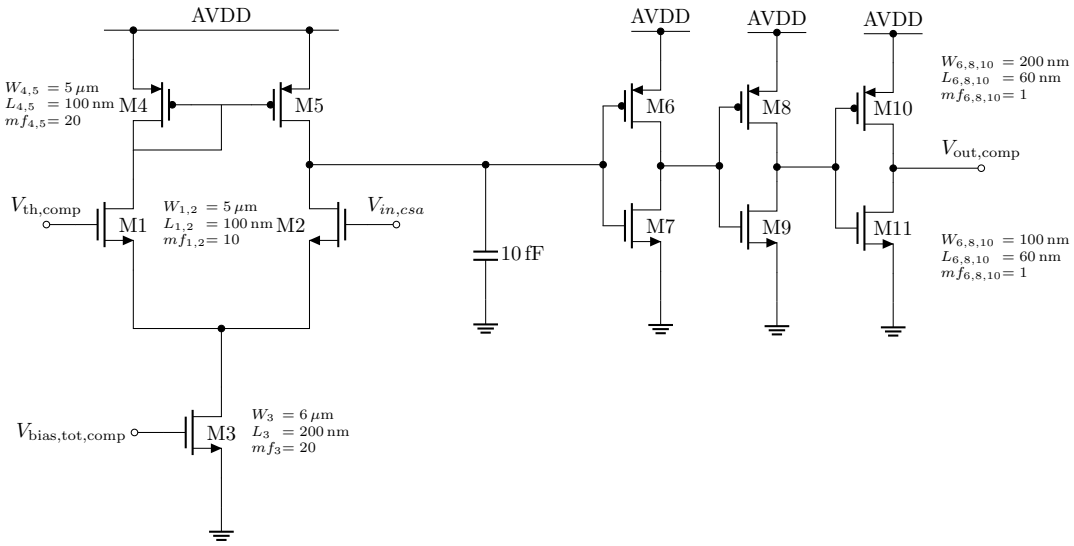


Figure 4.23: Schematic representation of the comparator circuit for the ToT channel. The comparator is responsible for processing the output signal from the charge sensitive amplifier and driving the subsequent digital logic. A 10 fF capacitor is connected to the output node of the differential pair to slow down the response time and reduce high-frequency noise, improving overall stability.

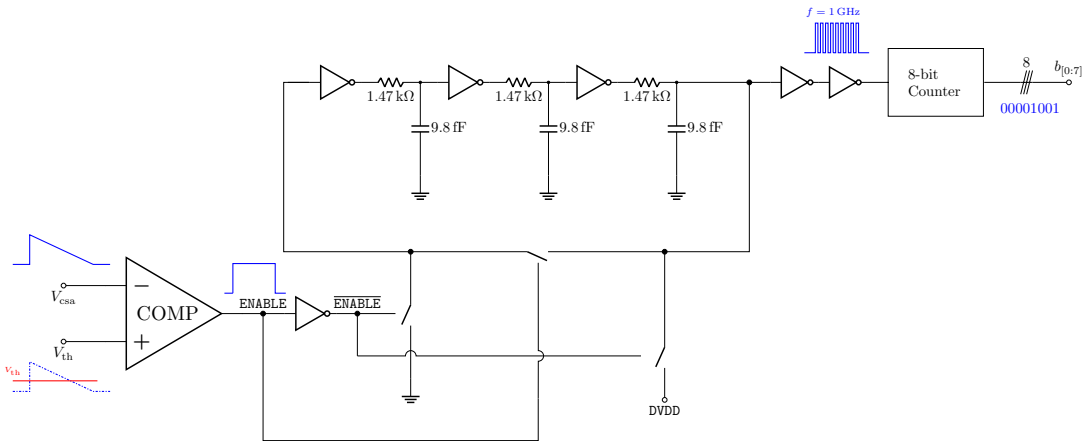


Figure 4.24: Schematic representation of the ToT counting section. The oscillator generates a high-frequency clock signal for the 8-bit counter, enabling precise measurement of the signal duration above threshold.

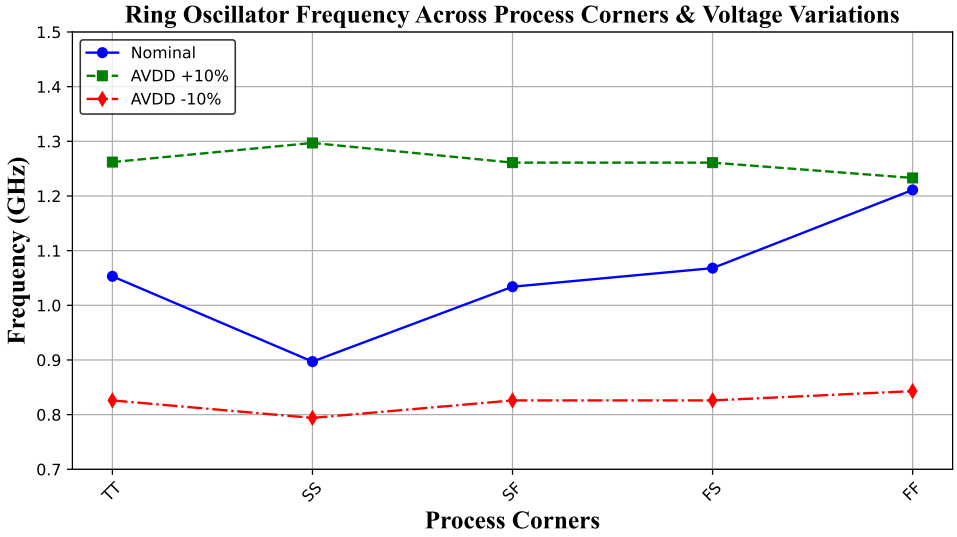


Figure 4.25: Post-layout simulation results of the ring oscillator frequency stability across process, voltage, and temperature (PVT) corners. The plot demonstrates reliable operation and frequency consistency near 1 GHz for all simulated conditions.

the counter must be able to count up to 250 clock cycles, which fits well within the 8-bit range (0-255).

The ring oscillator has been designed using three inverters connected in a loop, with a passive RC low-pass filter to stabilize the frequency after each inverter. The values for the low-pass filter are $R = 1.47\,\text{k}\Omega$ and $C = 9.8\,\text{fF}$ and have been chosen to achieve the desired frequency through SPICE simulations. The oscillation is activated by the comparator output signal, which closes the loop when the comparator output is high, enabling the counting process. When the comparator output goes low, the loop is opened, stopping the oscillation and thus the counting. Simulations have shown that the ring oscillator does not need a startup circuit, as it starts oscillating reliably when enabled by the comparator output. In the open loop configuration, one side of the chain is connected to ground, and the other side is connected to `DVDD`. As a result, the counter does not count, ensuring a stable and known state when counting is not active. Post-layout simulations have been carried out to validate the frequency stability of the ring oscillator across process, voltage, and temperature (PVT) corners. Typical-typical (TT),fast-slow (FS), slow-fast (SF) corners have been simulated considering a 27 °C temperature. Slow-slow (SS) and fast-fast (FF) corners have been simulated considering respectively −40 °C and 80 °C. For each corner, a variation of the supply voltage of ±10% has also been considered. The results of the simulations shown in the plot in Figure 4.25 confirm that the ring oscillator maintains a frequency close to 1 GHz across all PVT corners, with variations within acceptable limits for the intended application.

As mentioned, the signal from the ring oscillator is fed into an 8-bit counter, which increments its value on each rising edge of the clock signal while the comparator output remains high. When the comparator output goes low, the counting stops, and the current value of the counter represents the ToT measurement. The schematic representation of the counter is shown in Figure 4.27. As one can see, it is implemented using a series of flip-flops that store the count value. Each flip-flop represents one bit of the counter, and they are connected in such a way that the output of one flip-flop serves as the clock

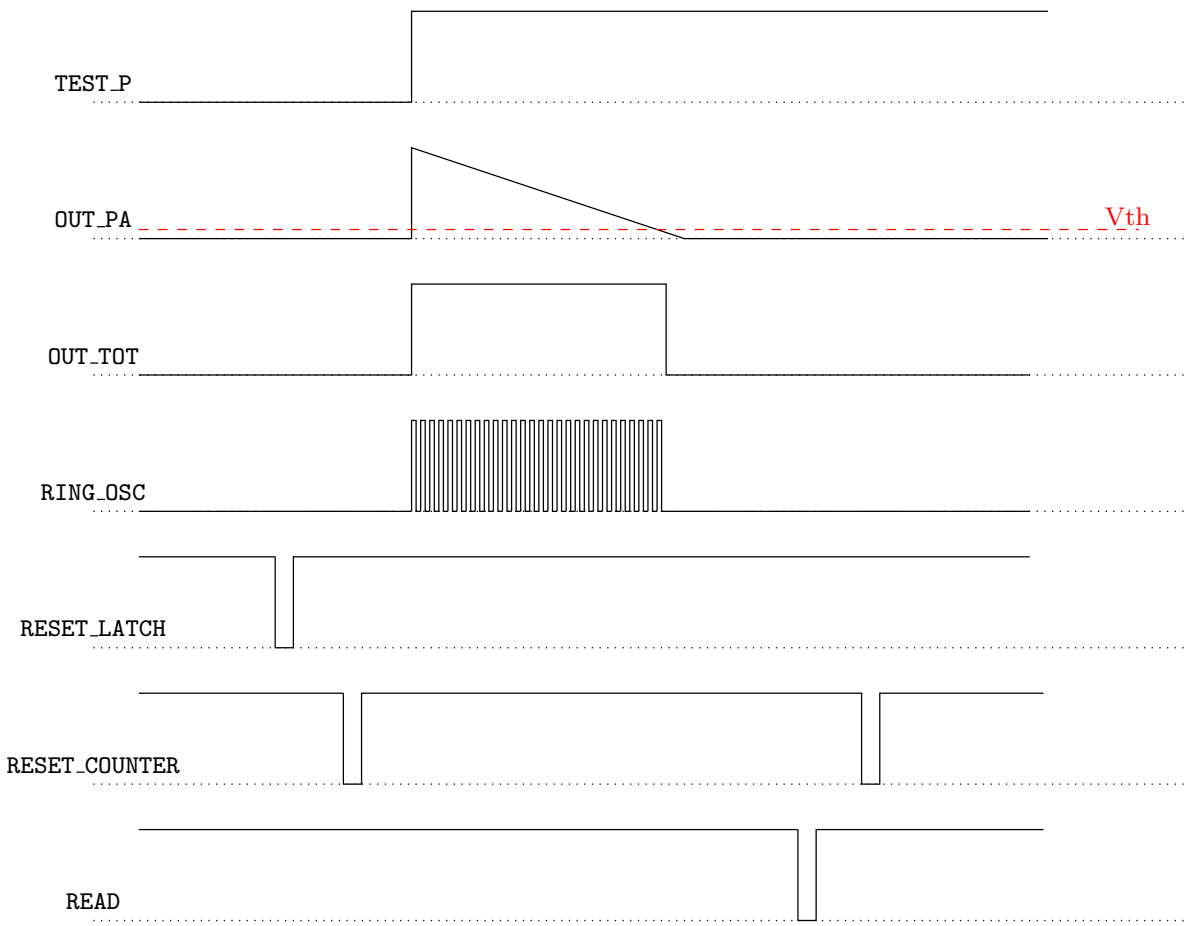


Figure 4.26: Representation of the timing diagram for the signals involved channel. This diagram qualitatively illustrates the recommended timing sequence for data acquisition.

input for the next flip-flop in the series, forming a ripple counter. This ripple (asynchronous) counter architecture is simple but introduces propagation delays between bits, which can affect speed and timing accuracy; for higher-speed applications, a synchronous counter—where all flip-flops share the same clock—would be preferable. However, for this design, the propagation delay in an 8-bit ripple counter is negligible compared to the 1 GHz clock period, so the ripple architecture is sufficient and does not limit performance. One important aspect of the counter design is the reset mechanism, which ensures that the counter starts from zero at the beginning of each measurement cycle. This is achieved by using a global reset signal that clears all flip-flops in the counter when activated.

A second important aspect is how to read the counter value after the measurement is complete. In the developed prototype, this can be done by buffering the counter output before driving the chip pads, using a set of output digital buffers. The chosen approach leverages the use of a latch that captures the output value for each flip-flop. This operation is handled by a global `READ` signal that, when activated, latches the current value of the counter into a set of output registers. This latching mechanism decouples the counter from the capacitance of the output pads, allowing the counter to operate continuously and accurately without being affected by timing errors or missed counts that could arise from driving large loads directly.

As above mentioned, another important global digital signal is the `RESET` signal, which is used to reset all the flip-flops in the counter to zero at the beginning of each measurement cycle. This ensures that each ToT measurement starts from a known state, preventing any residual counts from previous measurements from affecting the current reading.

While designing the data acquisition system, it is crucial to consider the timing of the `READ` and `RESET` signals to ensure accurate and reliable operation. A recommended timing sequence is as follows: (1) Assert `RESET` to clear the counter before the measurement cycle; (2) Deassert `RESET` to enable counting as the measurement window opens; (3) After the comparator output returns low (indicating the end of the measurement), assert `READ` to latch and output the counter value; (4) Deassert `READ` before the next cycle. For practical implementation with an FPGA or a microcontroller, refer to Figure 4.26 for a suggested timing diagram. This explicit timing avoids race conditions in practical implementations. The reading of the output data can be managed by an external FPGA or microcontroller, which can control the timing of the `READ` and `RESET` signals, as well as handle the data acquisition and processing. It is recommended that the external controller ensures a minimum pulse width of 10 ns for both `READ` and `RESET` signals, with setup and hold times of at least 5 ns relative to the measurement window, to guarantee reliable latching and resetting of the counter and avoid timing errors. The output of the counter has to be processed using a parallel bus, with each bit of the counter output connected to a dedicated output pad of the chip.

In order to validate the overall performance of the ToT channel, post-layout simulations have been carried out to assess the linearity of the response with respect to the number of input photons. The simulations were performed by sweeping the input charge from 1 to thousands of photons, considering a photon energy of 9 keV. Simulations, as shown later in this section, confirm a linear relationship between the number of input photons and the measured ToT in both gain modes, supported by a ring oscillator operating at $\sim$1 GHz with good stability across process and voltage variations.

To quantitatively assess the linearity of the ToT measurement system, the response has been compared against a best-fit linear model across the entire input range. For each input signal level, the deviation from the fitted line was evaluated, and the maximum

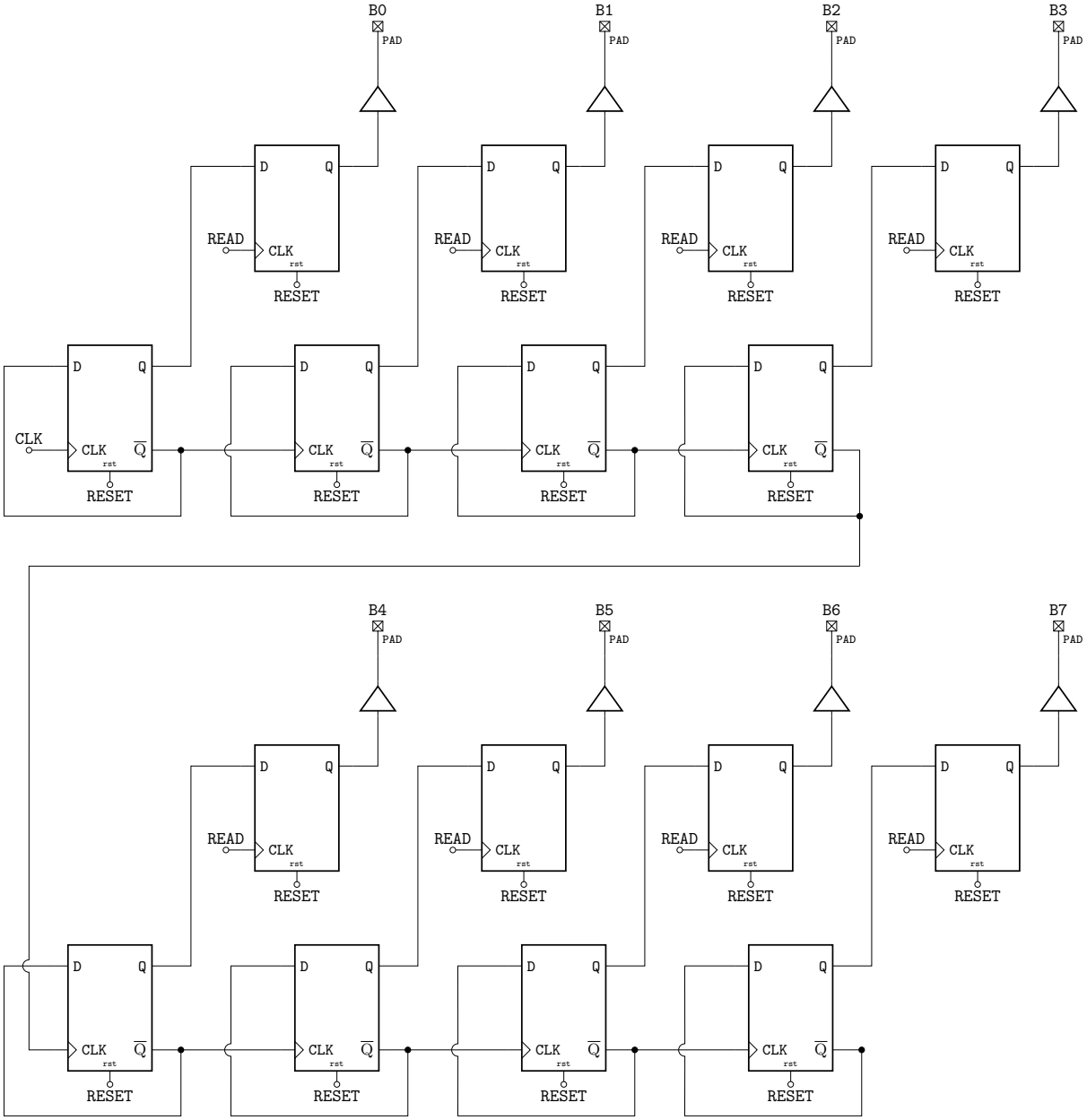


Figure 4.27: Schematic representation of the 8-bit counter used in the ToT channel. The counter records the duration of the comparator output pulse, providing a digital measure of the signal above threshold.

absolute deviation was normalized to the full-scale output value, providing a measure of the Integral Non-Linearity (INL).

This definition directly quantifies the worst-case deviation from an ideal linear response. In this design, the peak INL is 1.74% in the 1–100 photon range (high-gain mode) and 1.44% in the 100–10^3 photon range (low-gain mode), as shown in Fig. 4.28. These results confirm that the bilinear ToT architecture achieves good linearity over a wide dynamic range, making it suitable for demanding X-ray imaging applications.

Several parameters can be adjusted to tune the ToT response of the system, including the preamplifier feedback discharge current in both high-gain and low-gain modes, the threshold voltage for the comparator that switches between gain modes, and the threshold voltage for the comparator that drives the ToT counting system. Post-layout simulations have been carried out to evaluate the effect of varying these parameters on the ToT response. Figures 4.29 show the effect of varying the CSA feedback discharge current (regulated by the transconductor bias, `BIAS_GM`) on the ToT response in both high-gain and low-gain modes. As the discharge current increases, the ToT decreases for a given input signal, as the feedback capacitor discharges more quickly. This allows for tuning the dynamic range and sensitivity of the system to match specific application requirements. Figures 4.30 illustrate the impact of varying the comparator threshold voltage on the ToT response in both gain modes. Adjusting the threshold voltage changes the point at which the comparator switches, thereby affecting the duration for which the signal remains above threshold. Lowering the threshold voltage increases the ToT for a given input signal, while raising it decreases the ToT. This provides another degree of freedom for optimizing the system's performance based on the expected signal characteristics and noise environment.

4.3 The prototype chip

A prototype chip, whose layout was shown in Figure 4.18,including the described structures and, in particular, two independent standalone readout channels, has been submitted for fabrication in July 2025 in a 28 nm CMOS technology. The pinout of the chip is shown in Figure 4.31. Red pins are used for analog power and analog signals. Blue pins are used for digital power and digital signals. Two domains are used to separate the analog and digital sections of the chip, minimizing noise coupling and interference. Tables 4.7 and 4.8 summarize the list of the implemented IOs in the chip, specifying the type of each pin, the number of pads used, and a brief description of its function.

As mentioned earlier, the chip integrates two versions of the same channel: one with all the blocks described in the previous sections, and one with only the analog front-end. They are referred to as version B and version A, respectively. The latter allows for a more straightforward characterization of the analog performance of the front-end, without the influence of the digital section. The analog output of the CSA is buffered through a cascade of two source followers, which provide a low output impedance and the ability to drive a large capacitive load (around 10 pF). The buffered output is available on two separate pads, because of the necessity to drive a load of about 1 mA. Splitting the output in two pads allows to reduce the current load on each pad, improving the signal integrity and reducing the risk of damage to the chip.

Both the versions of the channel provide to the pads also the digital signal relative to the latch that switches between high-gain and low-gain modes. This signal can be used to monitor the switching behavior of the gain stage and to validate the functionality of

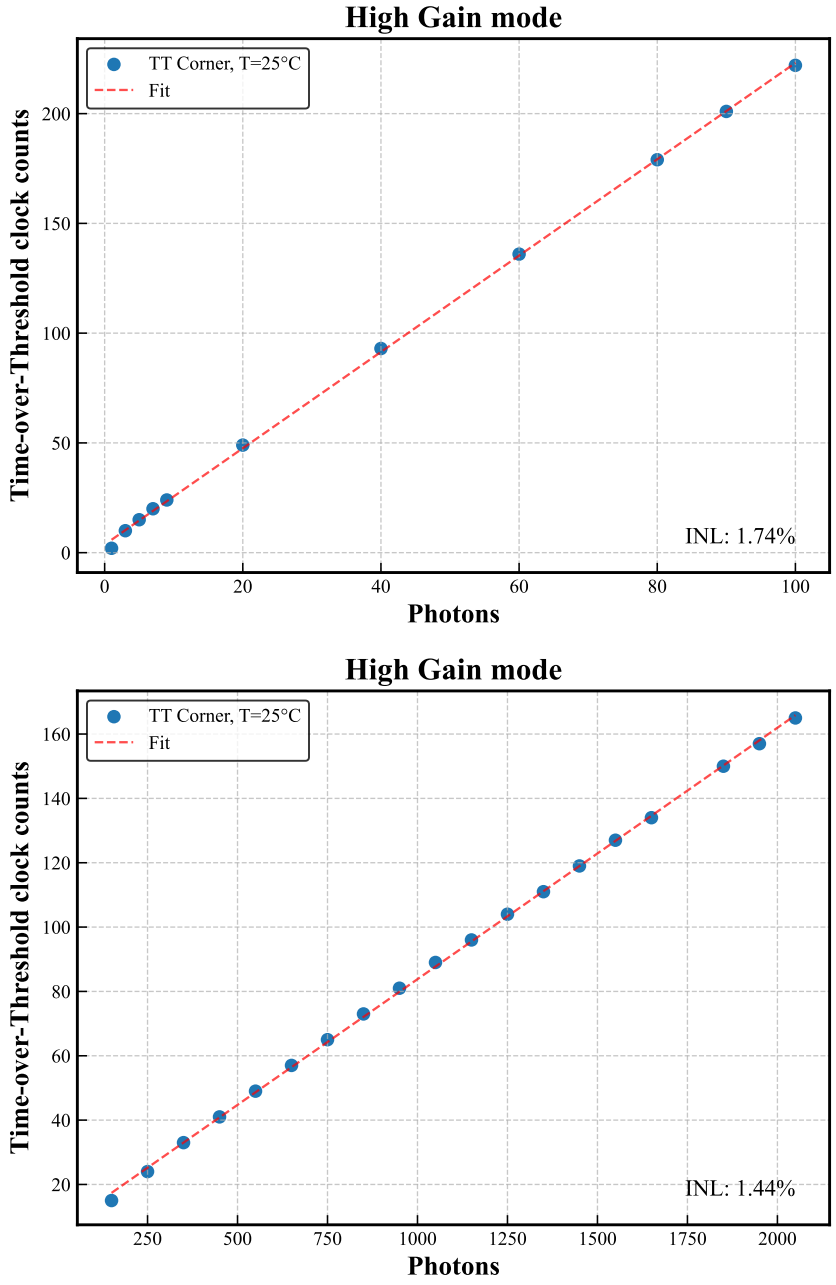
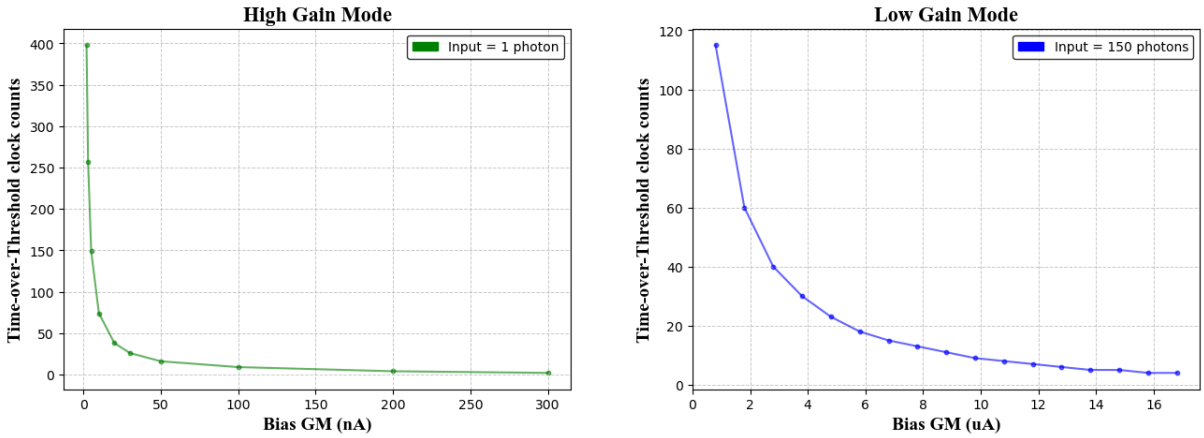
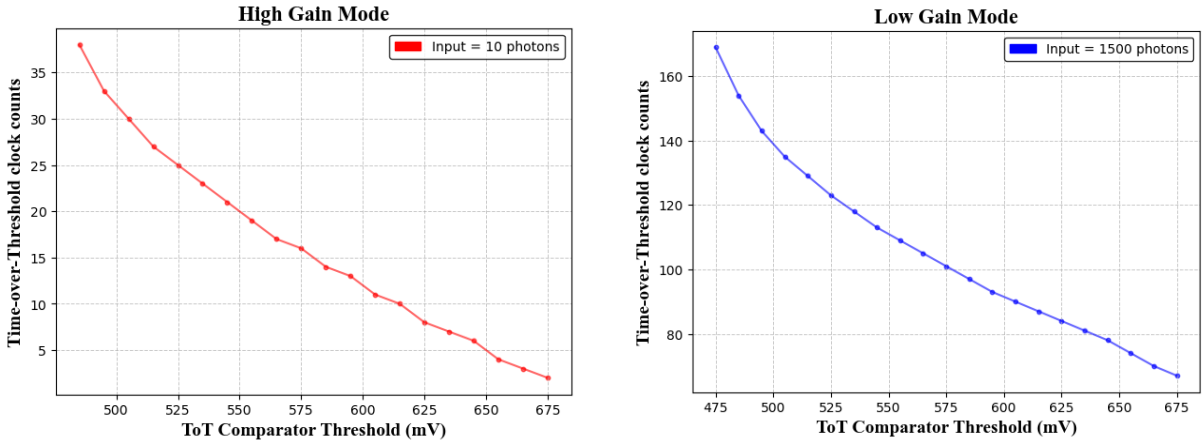


Figure 4.28: Linearity of the response of the analog channel calculated from the ToT with respect to the number of input equivalent photons: (Top) high gain configuration and (Bottom) low gain configuration.



(a) (b)

Figure 4.29: ToT response as a function of the discharge current: (a) high-gain mode, showing the effect for weak signals. The simulations have been evaluated with a comparator threshold voltage of 490 mV, an input of 1 photon in the TT corner.; (b) low-gain mode, illustrating the effect for large signals. The simulation has been evaluated with a comparator threshold voltage of 525 mV, an input of 150 photons in the TT corner.



(a) (b)

Figure 4.30: ToT response as a function of the comparator threshold voltage: (a) high-gain mode, showing the impact of threshold adjustment for weak signals. The simulations have been evaluated with a discharge current of 100 nA and an input of 1 photon in the TT corner; (b) low-gain mode, illustrating threshold tuning for strong signals. The simulation has been evaluated with a discharge current of 6.8 µA and an input of 1500 photons in the TT corner.

the feedback network and knowing when the system is in high-gain or low-gain mode.

Again, pixel bias management is crucial. For this purpose a peripheral block is integrated in the chip. It provides the necessary bias currents to the various components of the pixel matrix, including the charge sensitive amplifier, comparator, and other circuitry, thereby ensuring proper operation and performance. The same approach adopted for the flash-ADC and ToT for High Energy Physics version has been retained. As a matter of fact, the peripheral block includes a set of current mirrors with proper multiplication factors to generate the required bias levels.

The implemented approach leverages the connection of the current mirror loads to chip pads, which are implemented by means of external fixed resistors in series with a trimmer; the trimmer is manually adjusted during calibration to finely tune the bias current, which is essential for optimizing the performance of the front-end channels.

The peripheral block provides the following bias levels:

- `BIAS_GM_HIGHGAIN`= 30 µA. After a scaling factor of 100:1 in the current mirrors, this results in an actual feedback current of $I_{\mathrm{b,high\_gain}} \approx 300\,\mathrm{nA}$ for the transconductor in the CSA feedback in high-gain mode.

- `BIAS_GM_LOWGAIN`= 68 µA. With a mirror factor of 10:1, this results in an actual feedback current of $I_{\mathrm{b,low\_gain}} \approx 6.8\,\mu\mathrm{A}$ for the transconductor in the CSA feedback in low-gain mode.

- `BIAS_LATCH_COMP`= 50 µA. With a mirror factor of 10:1, this results in an actual tail current of $I_{\mathrm{b,latch\_comp}} \approx 5\,\mu\mathrm{A}$ for the comparator switching between high/low gain.

- `BIAS_P_BUF`= 50 µA. Tail current for the p-stage of the source follower buffer of CSA_B (set to $\sim 50\,\mu$A).

- `BIAS_PA`= 350 µA. With a mirror factor of 1:1. Bias current for the input device, chosen as a trade-off between noise, speed, and matching to optimize overall front-end performance.

- `BIAS_SF`= 100 µA. With a mirror factor of 100:1, this results in an actual bias current of $I_{\mathrm{b,SF}} \approx 1\,\mu\mathrm{A}$ for the source follower driving the high/low gain comparator.

- `BIAS_TOT_COMP`= 350 µA. With a mirror factor of 10:1, this results in an actual tail current of $I_{\mathrm{b,tot\_comp}} \approx 35\,\mu\mathrm{A}$ for the comparator used in the ToT section.

As mentioned, the references can be managed directly through dedicated pads, allowing for external adjustment and fine-tuning. This approach provides flexibility in setting the references both using laboratory instrumentation or by employing a DAC controlled by an FPGA or microcontroller on the test board. The characterization setup is currently under development; key aspects such as the design of the test board, integration of FPGA or microcontroller for timing and data acquisition, and provision for adjustable voltage references are being evaluated to ensure compatibility with the chip's requirements and to enable comprehensive performance testing. It is recommended to include a DAC to provide the voltage references for the comparators, allowing for easy adjustment and optimization of the threshold levels during testing and characterization, in order to evaluate the performance of the system under different operating conditions.

Table 4.7: List of implemented **analog** IOs.

IO name	Type	# pad	Description
AGND	Analog Ground	1	Analog ground
AVDD	Analog Power	1	Analog power supply
BIAS_GM_HIGHGAIN	Analog Bias	1	Tail current for transconductor (CSA, high gain)
BIAS_GM_LOWGAIN	Analog Bias	1	Tail current for transconductor (CSA, low gain)
BIAS_LATCH_COMP	Analog Bias	1	Tail current for HG/LG comparator
BIAS_P_BUF	Analog Bias	1	Tail current for P-stage buffer CSA_B (set to $\sim$50 μA)
BIAS_PA	Analog Bias	1	Bias current for input device
BIAS_SF	Analog Bias	1	Bias current for source follower to HG/LG comparator
BIAS_TOT_COMP	Analog Bias	1	Tail current for ToT comparator
CAL_HI	Analog In	1	High reference level for injection circuit
CAL_LO	Analog In	1	Low reference level for injection circuit
GND_BUF	Analog Ground	1	Ground for CSA_B buffer
OUT_PA_BUF	Analog Out	2	Buffered preamp output (duplicated, $\sim$1 mA)
P_AGND	Analog Ground	1	Peripheral analog ground
P_AVDD	Analog Power	1	Peripheral analog power supply
VDD_BUF	Analog Power	1	Power supply for CSA_B buffer
VTH_GM	Analog Ref	1	Threshold for CSA transconductor
VTH_LATCH_COMP	Analog Ref	1	Threshold for HG/LG comparator
VTH_TOT_COMP	Analog Ref	1	Threshold for ToT comparator

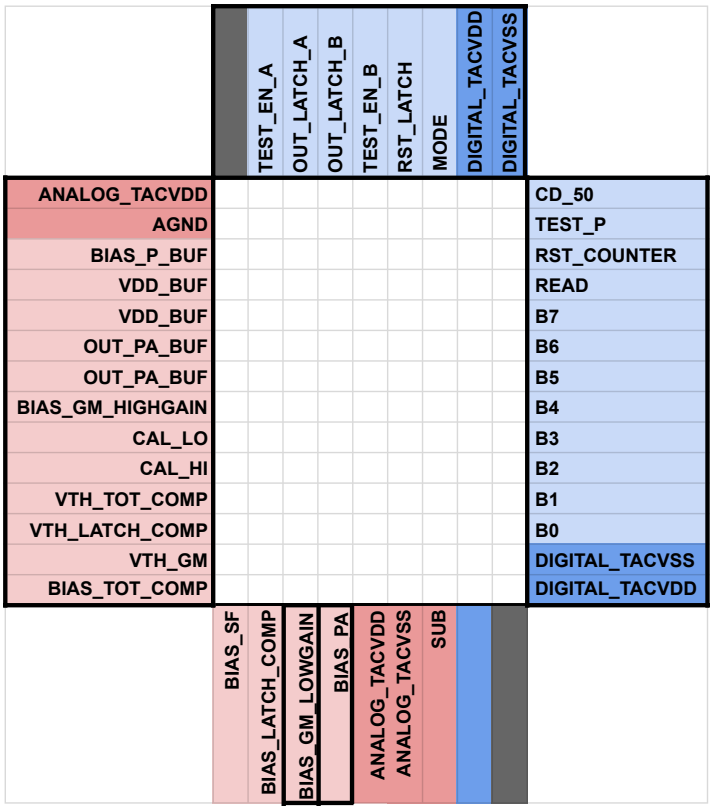


Figure 4.31: Pinout of the bilinear ToT prototype chip.

Table 4.8: List of implemented **digital** IOs.

IO name	Type	# pad	Description
B[0:7]	Digital Out	8	Counter output (B0=LSB, B7=MSB)
CD_50	Digital In	1	Enable 50 fF capacitance (detector emulation)
DGND	Digital Ground	1	Digital ground
DVDD	Digital Power	1	Digital power supply
MODE	Digital In	1	Selection of injection capacitance (2pF / 50fF)
OUT_LATCH_A	Digital Out	1	Preamp A mode monitor (0=HG, 1=LG)
OUT_LATCH_B	Digital Out	1	Preamp B mode monitor (0=HG, 1=LG)
OUT_TOT_B	Digital Out	1	ToT comparator output (without counter)
READ	Digital In	1	Counter bit transfer (posedge)
RST_COUNTER	Digital In	1	Counter reset (negedge)
RST_LATCH	Digital In	1	Preamp mode latch reset (HG/LG)
TEST_EN_A	Digital In	1	Enable injection circuit for preamp A
TEST_EN_B	Digital In	1	Enable injection circuit for preamp B
TEST_PULSE	Digital In	1	Injection signal (posedge)

Conclusions

This work addresses the gap in the literature regarding the practical applicability of 28 nm CMOS technology for front-end electronics in pixel detectors, targeting both high-energy physics and advanced X-ray imaging. The research focused on the design and experimental characterization of three integrated prototypes, demonstrating that this technology meets the requirements of future experimental physics.

The first prototype, developed within the FALAPHEL project, implements a zero-dead-time front-end with an in-pixel 2-bit flash ADC. This architecture is tailored for experiments with very high luminosity and high event rates, successfully processing consecutive signals in adjacent bunch crossings and ensuring zero dead time. The simulated threshold dispersion was below $30\,e^-$ r.m.s., and the measured equivalent noise charge (ENC) was approximately $63\,e^-$ r.m.s., comparable to state-of-the-art readout chips such as those developed by the RD53 collaboration. Furthermore, the power consumption per pixel is low, about 5.4 µW/pixel in a 25 µm × 50 µm cell, making it compatible with the power budgets for LHC upgrades. The stability of the threshold with respect to injection delay was also investigated, revealing negligible variations for positive delays and a significant increase for negative delays.

The second architecture, developed for both the FALAPHEL and PiHex projects, is based on the Time-over-Threshold (ToT) technique. It is designed for accurate energy measurements and robust operation in high-radiation environments. Simulations indicated noise levels not exceeding $50\,e^-$ r.m.s. at $-20\,°C$ for a detector capacitance of 50 fF, and the simulated time-walk was below 25 ns for an overdrive of $50\,e^-$ in the bandwidth-limited configuration. The untuned threshold dispersion was about $200\,e^-$ r.m.s., which was reduced to $16\,e^-$ r.m.s. after fine in-pixel tuning. The integral non-linearity (INL) of the ToT response was found to be close to 2 % for an input charge range up to $15\,000\,e^-$. The chip design has been completed and submitted, with characterization planned for late 2025 and early 2026. A custom setup has been specifically developed for the testing of the submitted prototype.

The third prototype, developed within the PiHex project, introduces a bilinear dynamic ToT architecture for X-ray imaging. This solution features an automatic gain switching mechanism, allowing the system to operate in a high-gain mode for weak signals (from 1 photon to 100 photon) and a low-gain mode for strong signals (from 100 photon to 4000 photon). This approach extends the dynamic range while maintaining low noise and fast response. Post-layout simulations confirmed response linearity, with INL of 1.7 % in the 1 photon–100 photon range and 1.4 % in the 100 photon–4000 photon range. The ToT counting system employs a ring oscillator generating a 1 GHz clock signal, enabling a time resolution of 1 ns. The prototype chip, which includes two versions of the channel (full and analog-only), was submitted for fabrication in July 2025.

Table 4.9 summarizes the main specifications and the results achieved for each prototype, highlighting the compliance with the application requirements. These results

confirm the suitability of 28 nm CMOS technology for future pixel detectors in HEP and X-ray imaging.

Table 4.9: Summary of application requirements and performance metrics for the 28 nm CMOS front-end prototypes designed in this work. The table compares the key specifications and experimental/simulated results across the three developed architectures.

	Zero-Deadtime FE	**ToT HEP FE**	**Bilinear ToT FE**
Target Application	HL-LHC Upgrades / FCC-hh (High Rate) Inner Tracker	FCC-hh / HL-LHC Upgrades Inner Tracker	FEL / X-ray Imaging instrumentation
Pixel Pitch	$25 \times 50\,\mu$m	$25 \times 100\,\mu$m	$110 \times 60\,\mu$m
Pixel Architecture	CSA + Discriminator + 2-bit Flash ADC	CSA with optional regular or limited BW + Discriminator + Digital blocks for ToT/ToA measurement	Double feedback CSA + Discriminator + local RO + ToT counter
Gain Stage	Regulated cascode	Self-cascode	Self-cascode
Main Requirements	Zero dead-time, High event rate capability	Accurate linear energy measurement	High Dynamic Range, Single photon sensitivity
ENC [e^- rms]	$\sim$63 e^- (Meas. @ 50 fF, Room temperature)	$\sim$48 e^- (Sim. @ 50 fF, $-20\,^\circ$C)	$\sim$242 e^- (Sim. High Gain)
Power Consumption	5.4 µW/pixel (Static)	Low Power Design (Target $< 5\,\mu$W)	Dynamic (Gain dependent)
Timing Performance	Dead-time (< 25 ns processing)	Time-walk < 25 ns (in-time threshold)	1 ns Resolution (Fast ToT clock)
Linearity / DR	2-bit discrete output	INL $\approx 2\,\%$	INL $< 1.8\,\%$ (1k–4k ph range)
Status & Results	**Characterized**: Proved 40 MHz operation w/o pile-up	**Tapeout 2025**	**Tapeout 2025**

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