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Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades

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Serial powering is the baseline option for the pixel detectors in both the ATLAS and the CMS experiments targeting the phase II HL-LHC upgrade. The Shunt-LDO regulator is integrated in the front-end chips to generate the required supply voltages. A new compensation scheme has been developed to assure stable operation with large on-chip low-ESR (equivalent series resistance) load capacitances. A two-stage bandgap voltage reference circuit has been implemented to improve regulation performance. Security features have been added to protect against overvoltage and overload. Additional features have been added to allow regulator operation with small supply currents during the installation phase.

Topical Workshop on Electronics for Particle Physics TWEPP2019
2-6 September 2019
Santiago de Compostela - Spain

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PoS(TWEPP2019)067

1. Introduction

A current based supply scheme of serially connected modules has been chosen as the baseline powering option for the pixel detectors in both the ATLAS and the CMS experiments targeting the phase II HL-LHC upgrade. In this supply scheme the Shunt-LDO regulator shown in figure 1 is integrated in the pixel front end chips to convert the current supply into the required supply voltages for the analog and digital part [1]. For these regulators, a parallel operation on chip and at module level is required to avoid single points of failure and hot spots to provide redundancy and to increase system reliability. Balanced shunt current distribution across devices placed in parallel is reached even if the regulators generate different output voltages by introducing a configurable slope at the Current-Voltage characteristic of the regulator input. The regulator is implemented with cascoded core transistors in 65 nm CMOS technology to tolerate supply voltages up to 2V and high radiation doses at the same time. A set of three successive test chips has been produced and tested to validate the proper operation of the circuitry.

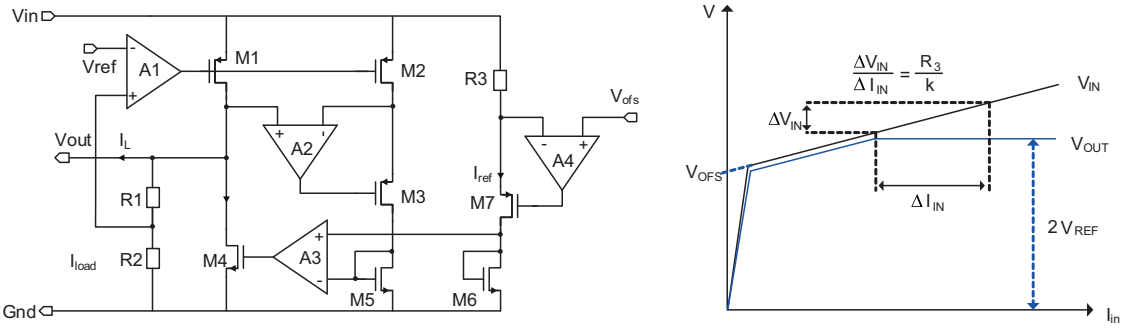

Figure 1: Simplified schematic of the Shunt-LDO (left). Characteristic IV curve for input and output (right).

2. Stabilization of the LDO

Conventional compensation methods like ESR-Compensation are not practical since the large on chip capacitance cancels the stabilizing effect. Therefore a new compensation scheme has been developed which enables a stable operation with a low-ESR on chip load capacitance of 300 nF, as shown in figure 2. The new implemented scheme is based on a slow-rolloff frequency compensation [2] and does not rely on the ESR of the external blocking capacitor. The current flow through the pass device M1 is sensed and mirrored to transistor M2 and drained to resistor R_s. The lower terminal is defined by the use of source follower M4 since it is not feasible to connect it to the regulator output port or to GND because otherwise the voltage headroom becomes either too small or the voltage across M2 gets too high especially at 2V input voltage. Sudden load steps lead to voltage changes across R_s which are coupled into the feedback path by capacitor C_s. This circuit introduces a double zero into the open-loop regulator transfer function which has a stabilizing effect on the entire system. An AC simulation is shown on the right side in figure 2 which depicts the characteristic of the output pole and the newly introduced zeros. It can be observed that first the pole dominates at low frequencies while the influence of the zero appears at higher frequencies. The frequency of the double zero ω_{zs} can be calculated at the interception point between the amplitude

response of the regulator output stage and the compensation circuit which leads to the result given in equation 2.1.

$$\omega_{zs} = \frac{1}{\sqrt{2}C_{out}R_{LG}}\sqrt{-1+\sqrt{1+\frac{{R_{LG}}^4{g_{m1}}^2{C_{out}}^2}{{g_{m2}}^2{R_o}^2{C_s}^2{R_x}^2}}} \tag{2.1}$$

Where $R_{\mathrm{LG}} = R_{\mathrm{load}} \,||\, (R_1 + R_2) \,||\, r_{\mathrm{ds1}}$, $R_{\mathrm{x}} = R_1 \,||\, R_2$ and $R_{\mathrm{o}} = r_{\mathrm{ds2}} \,||\, R_{\mathrm{s}}$.

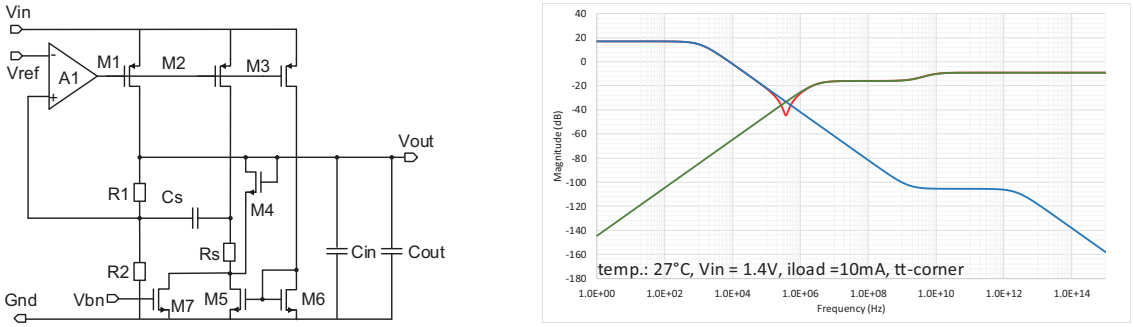

Figure 2: Schematic of the compensation circuit for the LDO part (left). Amplitude response of regulator output stage (blue), compensation circuit (green) and of combined circuitry (red) (right).

3. An improved Bandgap scheme

A new two-stage bandgap scheme has been implemented in order to generate precisely defined reference signals for the regulator. A first untrimmed 2V-tolerant bandgap is supplied by the unregulated input voltage and generates a reference signal for a linear preregulator. The preregulator is implemented as an LDO and is used to supply the second stage bandgap which is built with a current mode realization [3] and improves the PSRR significantly compared to the previous scheme. Besides more accurate defined reference signals V_{ref} and V_{ofs} can be achieved by employing a current trimming procedure to compensate random process variations.

4. Protection Circuits

Measurements in serial powering demonstrators have shown that the module voltage will drop in the event of a regulator overload which leads to overvoltages at other modules connected in the same serial chain. To avoid overload cases a protection circuit has been implemented which detects occurring overloads as undershunt current scenarios and reacts by reducing the regulator output voltage. In addition a further security feature has been integrated to protect the regulator from overvoltages. The schematics of both circuits are shown in figure 3.

4.1 Undershunt Current Protection

The Under Shunt Current Protection circuit has been integrated in order to protect the regulator from exceeding load currents. In the event of an overload, the output voltage is reduced by lowering the reference voltage V_{ref}, whereby the input voltage is independent and still remains constant.

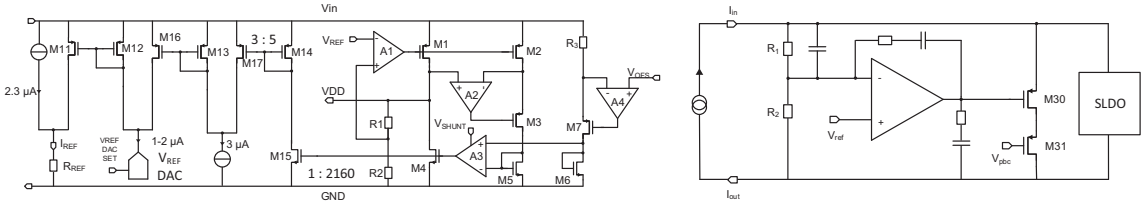

Figure 3: Schematic of the undershunt current protection (left). Schematic of the overvoltage protection (right).

Since a high load current reduces the shunt current, the current flow through shunt device M4 is sensed and used to detect an overload condition. In order to limit the voltage drop across the pass device M1, the reference current which is used to define the reference voltage V_{ref} is fixed to the minimum value. An additional current is supplied by a configurable DAC and defines the total reference current for the nominal state. In case of an overload the additional current is reduced or disabled.

4.2 Overvoltage Protection

A further security feature is provided by the circuit shown on the right of figure 3 which protects the regulator against overvoltages. The depicted circuit is a conventional shunt regulator which is formed by an amplifier, a cascoded shunt device and a voltage divider formed by R_1 and R_2. The circuit operates in parallel to the Shunt-LDO and controls the shunt device M30 to drain all excess current in case the input voltage exceeds 2V. The transistor M31 is powered by the biasing network and is necessary to tolerate voltages up to 2V. The capacitors and series resistors shown in the circuit are integrated to stabilize the system.

5. High and Low Power Mode

During the installation phase or maintenance, the system will be operated without active cooling. Accordingly, the regulator needs to startup reliably even with supply currents which are much smaller than the current reached under nominal working conditions in order to reduce the heat development. A new configuration circuit provides the opportunity to switch between two offset voltages that are classified as high and low power mode. An AC coupled square wave signal is rectified and used as a control signal to change the offset voltage. By switching into the low power mode an additional resistor is activated which increases the offset voltage to enable the operation with small supply currents. The second offset voltage used for the high power mode ensures an efficient operation with a large supply current for the nominal state. Measured results for both modes are presented in figure 4 and clarify that the nominal input voltage for the low power mode can be achieved at significantly lower supply currents. A two-stage rectifier built with MOS transistors is used to rectify the AC-Signal [4]. The two-stage structure is necessary in order to achieve a sufficiently large amplitude for the rectified signal.

5.1 Startup Circuit

An additional circuit was integrated to ensure a reliable startup at small supply currents. The

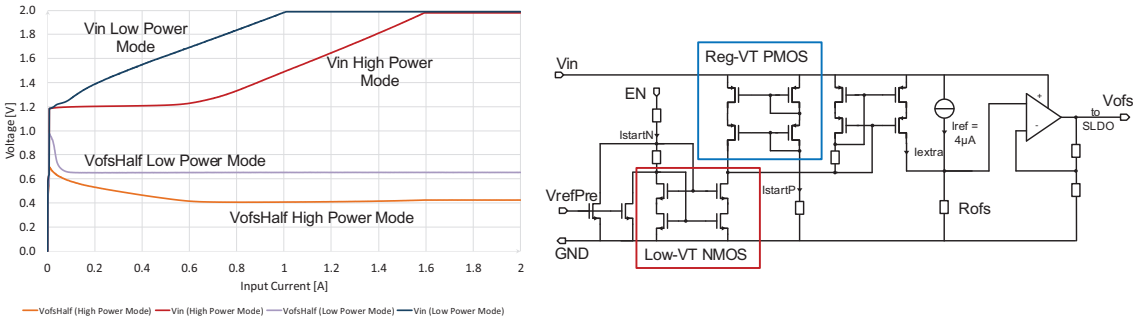

Figure 4: Input and half offset voltage during the high and low power mode (left). Schematic of the start-up circuit (right).

circuit will increase the reference signals V_{ofs} and V_{ref} during the power up phase to increase the regulators input impedance in order to improve the startup procedure. In the nominal case, both signals are defined by a reference current that is generated by the second stage bandgap. Since the reference current can't reach the desired value during power up, a further current is added to increase both reference values. However, this additional current is only active for small supply currents and is interrupted as soon as the preregulator bandgap is activated. The structure can be seen in figure 4 and was implemented with a wide-swing cascode current mirror built with low-Vt transistors and a further standard cascode current mirror built with regular-Vt devices. The former current mirror drains the current first and inject the auxiliary current into resistor R_{ofs}. The second current mirror structure is activated later.

6. Conclusion

A new compensation circuit has been successfully applied to the regulator which ensures stability for the entire system regardless of the high on chip capacitance. The new bandgap structure has significantly improved the PSRR and has the possibility to generate more precisely defined reference values by trimming. Overload and overvoltage scenarios can be now eliminated by additional security circuits. A further operating mode has also been introduced for test purposes during the installation phase without an active cooling system. In addition, a startup circuit has been supplemented to enhance the system reliability during the power up phase.

References

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