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The path towards the application of new microelectronic technologies in the AIDA community

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The Workpackage 3 of the AIDA project has the goal of facilitating the access of the high energy physics community to the most advanced semiconductor technologies, from nanoscale CMOS to innovative interconnection processes. The AIDA network is studying 3D integration with the main goal of designing novel tracking and vertexing detector systems based on high-granularity pixel sensors, with aggressive and intelligent architectures for sensing, analogue and digital processing and storage, and data transmission. This talk reviews the ongoing efforts and discusses the challenges that are being tackled in this framework to qualify technologies and devices for actual applications.

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1. Introduction

3D integration has triggered a wide interest in the high energy physics (HEP) community in view of the design of novel pixel detector systems with advanced readout electronics. In the microelectronic industry, this technology is defined as consisting of the vertical integration of thinned and bonded silicon integrated circuits (IC) with vertical interconnects between the IC layers [1]. In the industrial semiconductor world, 3D integration has been mainly developed as a way of increasing memory capacity, of making microprocessors faster (by decreasing the length of interconnections) and of improving the performance of imaging sensors by a pixel-level advanced signal processing. For future tracking and vertexing applications, the HEP community is planning to qualify 3D integration as a technology that makes it possible to devise pixel sensors with advanced architectures, smaller form factor, less material and dead areas, separation of sensing, analog and digital function [2].

In this scenario, the Workpackage 3 (WP3) of the AIDA project [3] was conceived as a network of institutions and research groups working on various flavors of 3D integration with the common goal of qualifying this technology for a next generation of HEP pixel detectors. This task foresees the fabrication of pixel sensors and CMOS readout ICs, which have then to be interconnected and form 3D vertically integrated devices. WP3 has organized itself in several subprojects, pursuing different technological approaches to 3D integration, depending at what stage the TSVs (Through Silicon Vias) are fabricated in readout chips. These approaches can be categorized in the "via first/middle" (vias are etched and filled during the CMOS processing) and "via last" techniques (vias are processed after the completion of the CMOS processing). With this latter technique, vertical vias of a relatively large size (typically of the order of 100 μm) can be fabricated. These large vias can be etched in the peripheral regions of readout chips to bring electrical connections to the backside, where a metal redistribution layer can be used to route signals and power to and from detector services. A support can be bonded to pads on this redistribution layer to achieve the chip connection to the external world. This allows for removing the chip periphery that is usually allocated for wire bonding pads, eliminating most if not all of the chip dead area. Moreover, the "via last" technique makes it possible to fabricate 3D devices with heterogeneous layers. This means that each layer can be fabricated in a different technology and optimized for its function, e.g., combining a high-resistivity fully-depleted pixel sensor with a readout chip in an advanced CMOS generation. The "via first/middle" approach is the technology of choice for more advanced applications of 3D integration, thanks to the higher TSVs density. In the case of pixel detector systems, this can be exploited in the design of small pitch sensing elements with advanced electronic functions performed in the pixel readout cells. The minimum possible size of pixels is obviously determined by another essential technological parameter, that is, the density of bonding pads between the device layers, going from relatively standard bump bonding processes at 50 μm pitch or more to high-density thermocompression copper-copper bonding with a pitch of a few μm.

AIDA WP3 subprojects are exploring a wide and diverse set of 3D integration technologies, as it was already discussed at the 2012 VERTEX workshop [4]. In the present paper, the progress and the plans of these subprojects are reviewed, discussing the results that were accomplished so far and the lessons that are being learned from the experience of the pixel detector community with 3D integration. It is important to notice that, while the AIDA main focus concerns detectors for high energy physics, the activities discussed here are of great relevance for medical imaging and photon science applications as well, and some WP3 subprojects are successfully developing demonstrators which target these fields.

2. Current R&D with "via last" 3D technologies in the ATLAS pixel community

Two of the WP3 subprojects are using the integrated circuits that were developed for the readout of pixel sensors in the ATLAS experiment at LHC. The first demonstrator modules with 3D integration features in high energy physics were built using FE-I3 ATLAS pixel chips with "via last" TSVs by IZM [5]. Planar pixel sensors were bump bonded to 90-µm thin FE-I3 chips with TSVs and backside redistribution layer. Successful tests proved that the performance of the resulting modules is not impaired by 3D technological steps. It appears then possible to design 4-side buttable pixel modules with the new FE-I4 ATLAS readout chip or its future successors for applications in the High Luminosity LHC (HL-LHC). Fig. 1 shows how the concept of a pixel detector module currently designed for the ATLAS IBL may evolve to a 4-side buttable device in future HL-LHC detector upgrades.

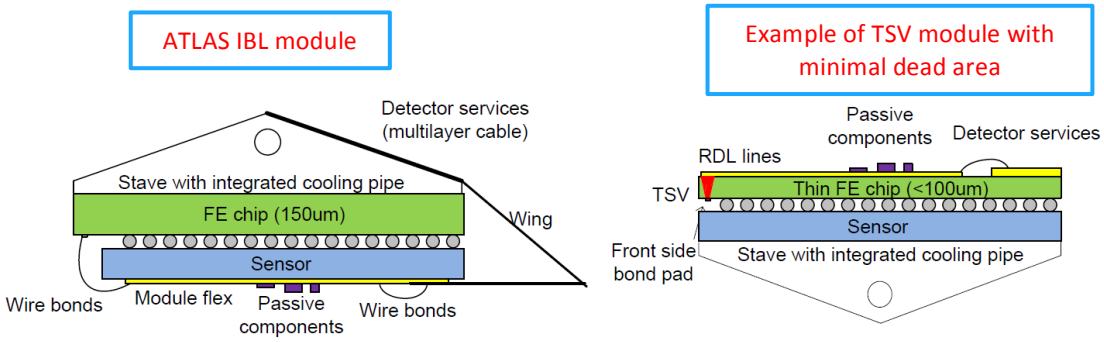

Figure 1. Concept for the evolution of ATLAS pixel modules with TSVs for backside connectivity.

As a next step, IZM is currently processing the new generation ATLAS pixel readout chip for the IBL and HL-LHC, the FE-I4B, which is fabricated in a 130 nm CMOS technology. The example of this chip gives here the opportunity to discuss an interesting aspect of "via last" processing in CMOS wafers, as shown by Fig. 2. TSVs are used here to connect standard wire bonding pads to the chip backside. It is important to design these pads in such a way that it is not required to etch vias across the entire thick underlying metal stack. This was achieved in the FE-I4 design by connecting the first metal level M1 (just above the silicon substrate with the transistors) to the uppermost metal level M8 and the aluminum pad. In this way the vias need

only to be etched up to M1 through a silicon substrate thinned to 150 µm. The tapered vias have a diameter of about 100 µm at the bottom and 40 µm at the top.

3D integration tests on FE-I4 are also under way with the potentially more advanced ICV-SLID (InterChip Vias – Solid-Liquid InterDiffusion) process by EMFT [6]. The EMFT etching process allows for TSVs with a large aspect ratio (10:1) and a small diameter (5 µm). Fig. 3 show how this process can be used to connect the CMOS readout chip to an active edge pixel sensor, fabricating a detector with very little dead area.

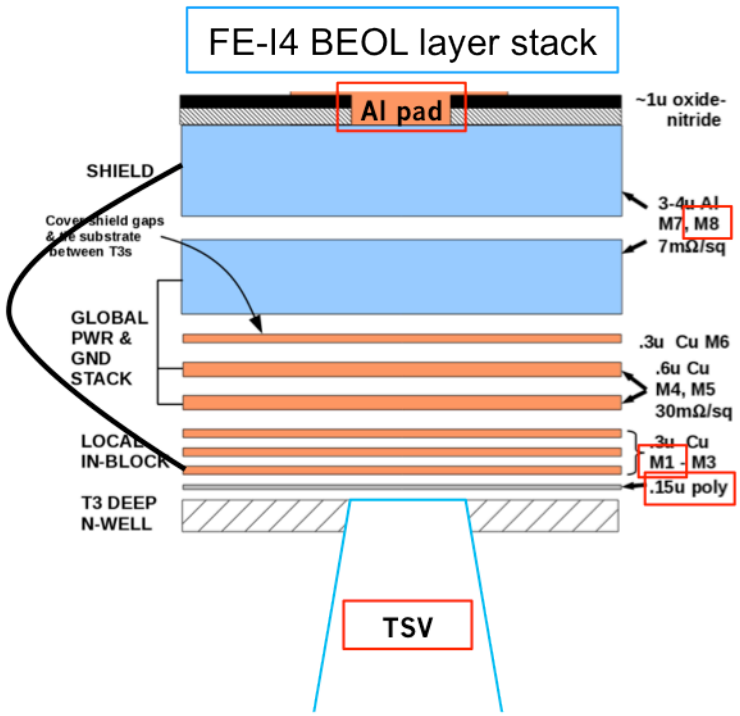

Figure 2. Metal stack under the wirebonding pads of the FE-I4 chips, with TSVs etched from the chip backside.

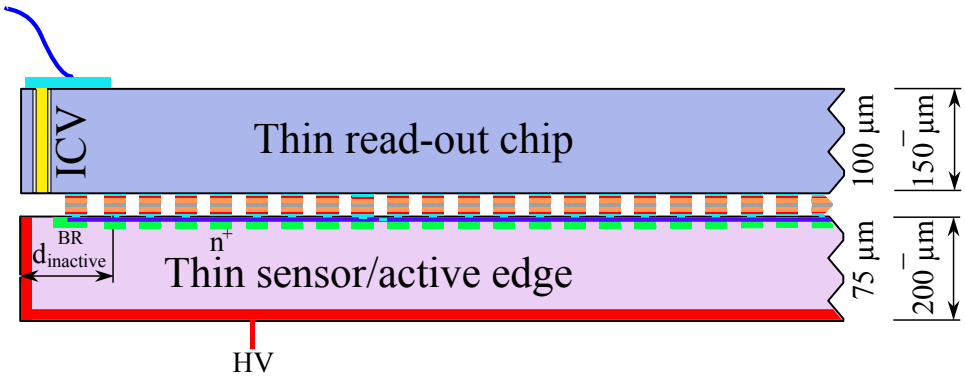

Figure 3. Interconnection between a CMOS readout chip and an active edge pixel sensor with the ICV/SLID process.

The SLID technology is bumpless and allows in principle for a high density of interconnections, limited only by the pick and place accuracy. FEI3 wafers have already been processed with this technology and successfully interconnected (interconnection only without vias). The different architecture of the FEI4 chip with respect to the FEI3 (no free area for vias in the wire bond area, connection directly to metal 1) requires a modification of EMFT's TSV technology. Instead of etching the vias from the front side through the metal layers into the bulk and consecutive back thinning, the vias need to be etched in already thinned wafers from the backside. The need of passivation of the via walls and contact opening to metal 1 is more challenging especially for large aspect ratio vias. This may require larger via diameters than in the old FEI3 project, but it is planned to maintain diameters below 25 µm, which is still substantially smaller than vias from other via last processes. EMFT has completed the layout of TSVs and is still working on optimizing process details, with the goal of beginning wafer post-processing in the next few months.

In the ATLAS community, there are also plans to use through-silicon vias for backside connection in the next generation of readout chips that will be designed in the 65 nm CMOS node [7]. The plan is to use a similar concept as in Fig. 3 for the interconnection between the readout chip and the sensor layer.

3. AIDA activities for 3D integration of imaging sensors

In AIDA WP3, "via last" 3D integration as an enabling tool for 4-side buttable pixel modules is also being successfully tested in the design of detectors for X-ray imaging.

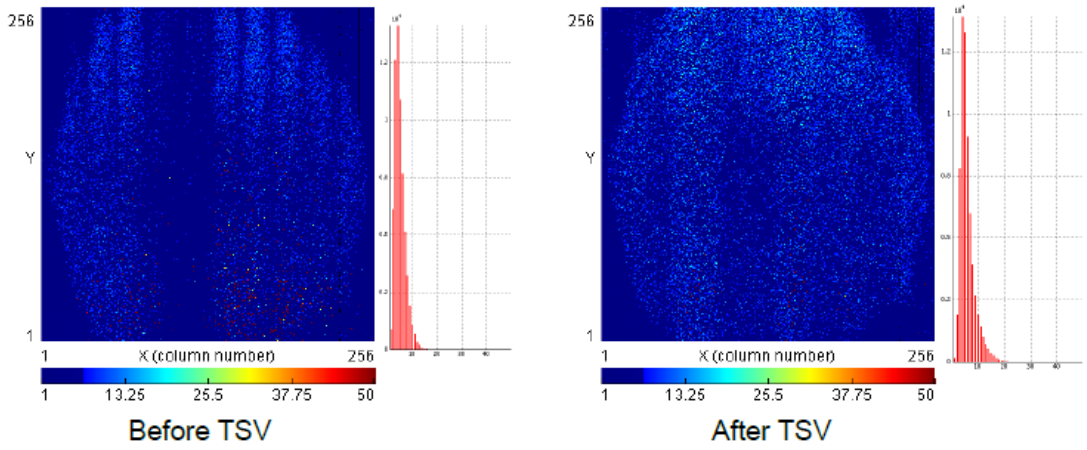

Figure 4. Noise distribution of the MEDIPIX3 chip with and without TSV processing. No significant noise increase is visible.

Excellent results were recently achieved with the MEDIPIX3 chip [8]. The aim of the project is to utilize an existing mature TSV technology made available by CEA-LETI as a part of their "Open 3D" initiative. The LETI via-last process offers vias of about 40 µm diameter and 3:1 aspect ratio [9]. MEDIPIX3 is a 130 nm CMOS chip for high resolution X-ray spectral

imagers based on hybrid pixel detectors. It comprises a 256x256 matrix of pixel readout cells with a 55 μm pitch. Each cell is highly programmable, e.g. making it possible to operate at 110 μm pitch in spectroscopic mode. The post-processing at CEA-LETI has already been performed successfully. Noise performance showed no difference between chips with and without TSVs, as shown by Fig. 4.

Successful tests were then performed on the full assembly of a 110 μm-thick MEDIPIX3 chip bump bonded to a 300 μm-thick edgeless silicon pixel sensor from Advacam via LETI TSVs. This is a very important milestone for AIDA WP3 as the chip had a full redistribution layer on the back side and it was mounted on a standard PCB [10]. This development points the way forward to tiling large sensor areas in a seamless way.

Another WP3 subproject is applying 3D integration techniques to the HEXITEC readout chips for CZT pixel sensors designed for dual isotope SPECT imaging [11]. For this application, there is a need for seamless sensor tiles. This is addressed by exploring two different aspects of 3D integration. The first is similar to what has been discussed before, concerning backside interconnection of I/O pads by etching TSVs in the substrate. To this purpose, single layer HEXITEC wafers have been post-processed at Tohoku-Microtec [12]. The second activity plans for the fabrication of readout chips with two vertically interconnected layers ("tiers"). The first tier hosts the same analog circuitry as in HEXITEC, whereas an ADC for each pixel and the digital readout are located in the second tier. The chips have been tested separately and are fully functional. 3D processing has begun with the ICV-SLID process at EMFT. There is one TSV interconnect from the analog pixel on the top layer to the digital on the bottom layer (as shown by Fig. 5) and one for each I/O connection as all readout is from the top layer.

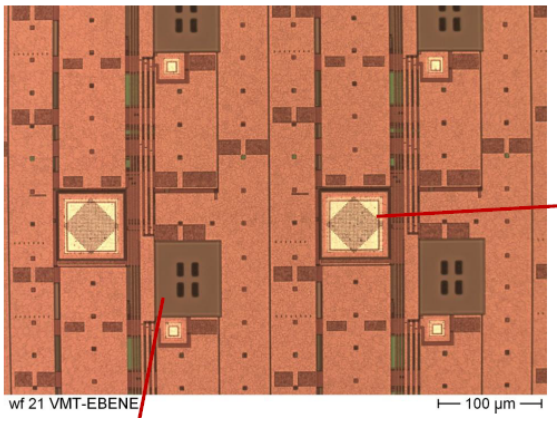

Figure 5. Tungsten vias in the 3D Hexitec analog layer: four black rectangles with 3 μm x 10 μm cross section inside the brown rectangles (free silicon area), through 50 μm silicon.

4. Plans with high-density 3D interconnection processes

With respect to the technologies discussed in the previous section, more aggressive, "via first/middle" versions of 3D integration (with TSVs and wafer bonding pads of a few μm pitch)

may provide the means to design pixels with smaller size, approaching 10 μm, as it is for example required by vertex detectors at future linear colliders. With a 3D integrated circuit, this can be achieved without reducing pixel-level electronic functions. On the contrary, with multiple interconnections in a single pixel cell, it is possible to devise novel readout architectures based on information processing, storage and transmission effectively performed at the level of a pixel or of a region of pixels.

In the past few years, in the HEP community a wide interest arose for the "via middle" process by Tezzaron/GlobalFoundries [13, 14]. In such a process, through-silicon vias are etched in the silicon wafers in the early stages of CMOS fabrication, just after transistor processing steps and before the deposition of the various levels of metal interconnects. It is then possible to fabricate integrated circuits with two tiers by the bonding of two 130 nm CMOS wafers, as depicted by Fig. 6. In this process, TSVs have a 1.2 μm diameter, a 2.5 μm pitch and a 6 μm depth. Interconnection bonds between layers have a 4 μm pitch.

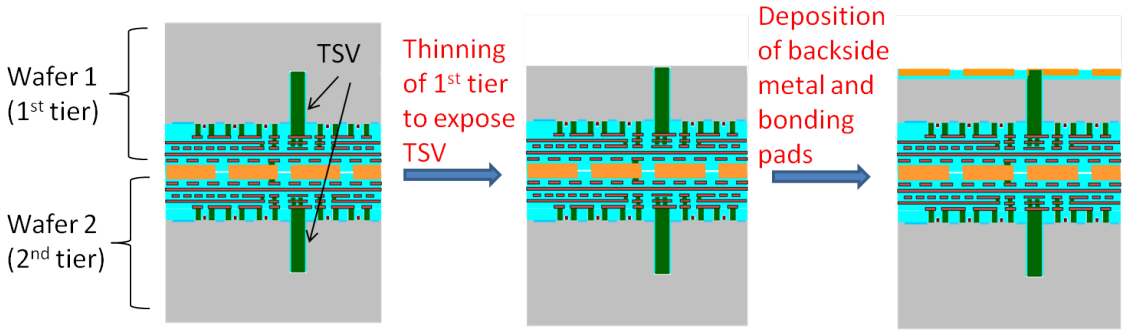

Figure 6. The last steps of 3D processing after wafer bonding by Tezzaron: wafer thinning and backside metal deposition.

CMOS pixel sensors and two-layer integrated circuits have been fabricated and successfully tested in this Tezzaron technology by Fermilab which organized the first MPW run [14] and by research groups in AIDA WP3 [15, 16], providing an extensive demonstration of the potential of high-density 3D processes. In WP3, on the basis of these results, there are plans for submitting new 3D chips with the Tezzaron process, and design studies were already carried out to define the circuit architecture and the pixel layout in these new devices. One of these chips is devised for the readout of pixel sensors, either classical fully-depleted ones or CMOS MAPS (Monolithic Active Pixel Sensors). The final device structure is then foreseen to comprise three layers. Besides the sensing layer, the other two layers are designed in the 3D CMOS Tezzaron process: they will respectively host the analog front-end and the digital readout circuits. This 3D integrated circuit could be connected to the sensing layer by a standard bump bonding process or by a more advanced low-mass and high-density interconnection technology. Design studies demonstrate that in a 50 μm x 50 μm 2-layer readout cell it is possible to integrate the classical readout chain for semiconductor detectors (preamplifier, shaper, discriminator with local threshold adjustment), while the digital layer of the cell can host an advanced pixel-level logic implementing a novel readout architecture which enables a

sparsified and time-ordered readout of the pixel matrix [17]. The actual fabrication of this chip is still pending, since presently (December 2013) a new multiproject wafer (MPW) run has not been scheduled yet.

Another 3D device has been designed by a WP3 group in the Tezzaron process and consists of 2 layers of Geiger-Mode APD (Avalanche PhotoDiodes) arrays with integrated CMOS readout [18]. In this case, the goal is to increase the fill factor of such devices. This is achieved by stacking two detector layers, one on top of the other, where the top layer will contain sensors occupying the dead regions in the bottom layer. Fill factor can be increased up to 92% by using this 3D stacking of sensors. This design makes it also possible to read out the pixels with electronic circuits operated in a gated mode, so that the dark count rate can be greatly reduced without degrading the fill factor.

Because of the delays in the schedule of future MPW runs in the Tezzaron process, alternative technologies are being evaluated for the fabrication of two-tier CMOS devices. Currently, there are plans to accomplish this goal by exploiting CMOS image sensor processes where the particle-sensing region is a relatively thick (15 to 40 μm), high-resistivity epitaxial layer, that can be at least partially depleted for a better signal-to-noise ratio and radiation hardness [19]. A small pitch CMOS pixel sensor could then be read out by a high performance digital chip, fabricated in the same process and interconnected to the sensor by means of fine pitch 3D integration techniques.

5. Conclusions and outlook

The European HEP detector community has organized itself in AIDA WP3 with the aim of exploring 3D integration and its potential in view of very demanding future applications at the LHC Phase-II upgrades and the linear colliders. Especially in the case of the "via last" flavor, results are very promising and are leading to the fabrication of 3D devices with interconnected pixel sensors and readout electronics, with backside connectivity to remove dead areas. With finer-pitch, "via first/middle" processes technical problems appear to be more difficult and still require a considerable R&D effort. However, they have already shown their very high potential for high performance pixel devices.

The growing appeal of 3D integration is proven by the new ideas that are currently stemming from the design solutions conceived and demonstrated in the AIDA WP3 network. An example in the HEP field is the idea of using "via last" TSVs at the periphery of pixel chips and create a backside bridge between two adjacent pixel detectors, so that it is possible to combine the information from a region encompassing pixels from both detectors [20]. The implementation of this concept could help in optimizing the efficiency of a p_T-discriminating module, where hits in two closely spaced strip and pixel sensor layers are correlated. Ideas for developing multilayer readout chips with vertical interconnections are already being proposed in the photon science field as well [21]. They foresee 3D integration of analog, digital and DRAM layers, each in the optimal CMOS technology.

The future evolution of the 3D devices discussed in this paper will of course be closely linked to the development of 3D integration processes in the microelectronic industry, and to their actual availability to an external and usually small volume customer such as a group

developing pixel detectors for particle tracking or X-ray imaging. The WP3 community is presently developing plans to continue its R&D activities, for the full development of 3D integration for HEP detector applications, especially as far as the qualification of fine-pitch (of the order of 20 μm or even less) interconnections is concerned.

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