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# Perspectives of 65 nm CMOS technologies for high performance front-end electronics

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The 65 nm CMOS generation is currently being evaluated as a promising solution for the integration of high speed circuits with high functional density in a small pixel. This technology node has specific features, such as new materials introduced to limit the current tunneling through the thin dielectric, that need to be thoroughly investigated. In order to assess how these new physical parameters impact on the device properties, such as noise and radiation hardness, this paper presents and discusses the characterization of 65 nm CMOS transistors, in terms of intrinsic gain, gate leakage current and noise performance, before and after irradiation with $\gamma$-rays. A comparison with data coming from less scaled technologies is also provided.

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## 1. Introduction

Deep-submicron CMOS technologies, thanks to their large scale of integration, have been extensively used for the development of front-end electronics for hybrid pixels and monolithic active pixel sensors (MAPS). However, the demand for higher in-pixel functionalities along with the reduction of pixel cell size is driving the interest of the designer community towards the 65 nm node or to vertical integration technologies (3D). This seems to be a critical choice in view of satisfying the resolution, readout speed and radiation tolerance, as required by high energy physics experiments at the next generation facilities. As far as standard 2D technologies are concerned, the 130 nm CMOS node is currently the focus of integrated circuit designers for the development of Application Specific Integrated Circuits (ASICs) in detector applications [1]. Nonetheless, the 65 nm process is considered an interesting solution in view of the development of high-density, high-performance mixed-signal readout circuits. At nanoscale geometries, the impact of new dielectric materials and processing techniques (silicon strain, gate oxide nitridation) on the analog behavior of MOSFETs has to be carefully evaluated [2, 3]. This is carried out in Section 2 of this paper, concerning the characterization of 65 nm CMOS devices from the stand point of intrinsic gain, linearity, gate leakage current, and noise performance. In Section 3, the radiation tolerance of the technology is discussed. In Section 4, a prototype chip designed in a 65 nm process, provided by IBM, is described. Finally, in Section 5, the collaborative activities on the 65 nm technology, developed in the framework of the AIDA project, are presented.

## 2. Technology characterization

The MOSFETs studied in this work belong to a 65 nm Low Power (LP) CMOS process from a commercial vendor (Foundry A). The equivalent thickness $t_{ox}$ is 1.95 nm and the maximum allowed supply voltage $V_{DD}$ is 1.2 V for the core devices we have tested. The devices were designed with a standard open, interdigitated layout with a finger width of 5 $\mu$m, except for transistors with $W$=1000 $\mu$m, which have a finger width of 10 $\mu$m. This work also reports on measurement results for general purpose (GP) transistor type, coming from a 90 nm CMOS process manufactured by Foundry A, and from a 90 nm and a 130 nm CMOS processes provided by a second vendor (Foundry B). For 130 nm devices, $t_{ox}$=2.4 nm, and $V_{DD}$=1.2 V; for 90 nm transistors, $t_{ox}$=2.0 nm and $V_{DD}$=1.0 V. Static and signal parameters were measured by means of an Agilent E5270B Precision Measurement Mainframe with E5281B SMU Modules. The spectral density of the noise in the channel current of the device under test was amplified by a purposely developed wideband interface circuit, which allows for noise measurements in the 100 Hz - 100 MHz range [4], and detected by an Agilent 4395A Network/Spectrum Analyzer.

### 2.1 Intrinsic gain

The intrinsic gain, being the maximum voltage gain obtainable from a single transistor, is an extremely useful figure of merit to understand the impact of scaling on the performance of analog circuits. The intrinsic gain is defined as the ratio of the channel transconductance $g_m$ to the output conductance $g_{ds}$. It has been shown that the intrinsic gain depends on the scaling of the gate length



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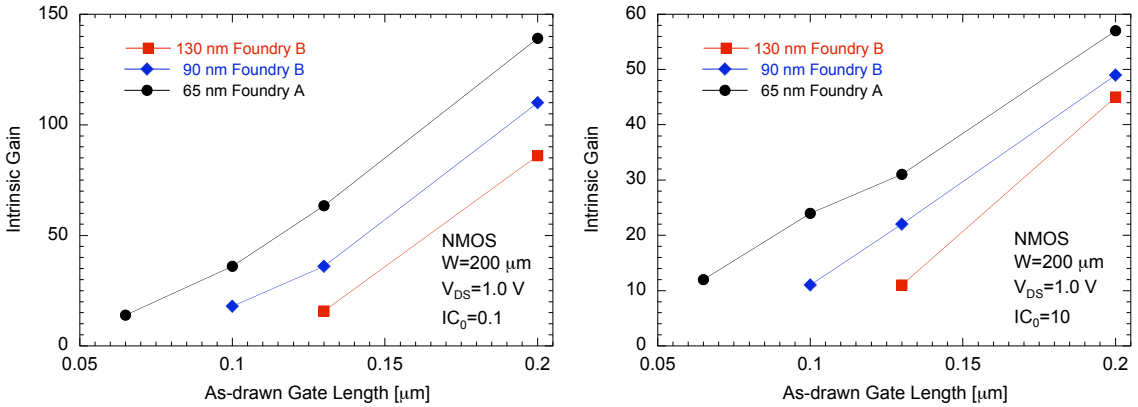


**Figure 1:** intrinsic gain as a function of the gate length $L$ for NMOS devices belonging to three technology nodes. On the left, devices are biased at the boundary between the weak and the moderate inversion ($I_{C0}$=0.1), and on the right, at the boundary between the moderate and the strong inversion ($I_{C0}$=10).

and on the coefficient $\alpha$ for constant-field scaling [5]:

$$\frac{g_m}{g_{ds}} \propto \alpha \cdot L. \tag{2.1}$$

In this work, the intrinsic gain has been studied as a function of the technology node, the channel length $L$ and the device inversion level. The actual inversion level of a MOS transistor, at a given current, can be expressed by means of the inversion coefficient $I_{C0}$= $I_D/I_Z^*$·W/L. $I_{C0}$ depends on the characteristic normalized drain current defined as $I_Z^*$=2$\mu$ $C_{OX}nV_T^2$, where $\mu$ is the channel mobility, $n$ is a coefficient proportional to the inverse of the subthreshold slope of $I_D$ as a function of $V_{GS}$ and $V_T$ is the thermal voltage. At the center of the moderate inversion, that is at $I_DL/W$=$I_Z^*$, the inversion coefficient is equal to 1. Under the hypothesis that the moderate inversion region extends one decade before and one decade after $I_Z^*$, the weak inversion region can be assumed to take place for devices with an inversion coefficient smaller than 0.1, while the strong inversion approximation is valid for devices with an inversion coefficient greater than 10. The impact of scaling on the intrinsic gain can be evaluated by looking at the plots reported in Figure 1, which shows the trend of this parameter, as a function of the gate length, for NMOS devices belonging to three different technology nodes. The devices are biased at the same inversion level. Since $I_{C0}$ is proportional to the $I_D\frac{L}{W}$ product, different bias currents are considered for the various geometries, while a constant drain-to-source voltage $V_{DS}$=1.0 V is applied. In Figure 1 (left), devices are biased at $I_{C0}$=0.1, that is at the boundary between the weak and the moderate inversion, while in the plot of Figure 1 they are biased at $I_{C0}$=10, that is at the onset of strong inversion. As foreseen by previous equations, if the gate length does not scale, we have an improvement in the intrinsic gain. Instead, if $L$ scales by the same factor $\alpha$ as the technology node, the intrinsic gain is not degraded by scaling in agreement with the constant field scaling rules [5].

### 2.2 Gate leakage current

One of the main limits in the use of nanoscale technologies is the reduction of the gate oxide thickness into the direct tunneling regime. The gate current, being caused by individual charge



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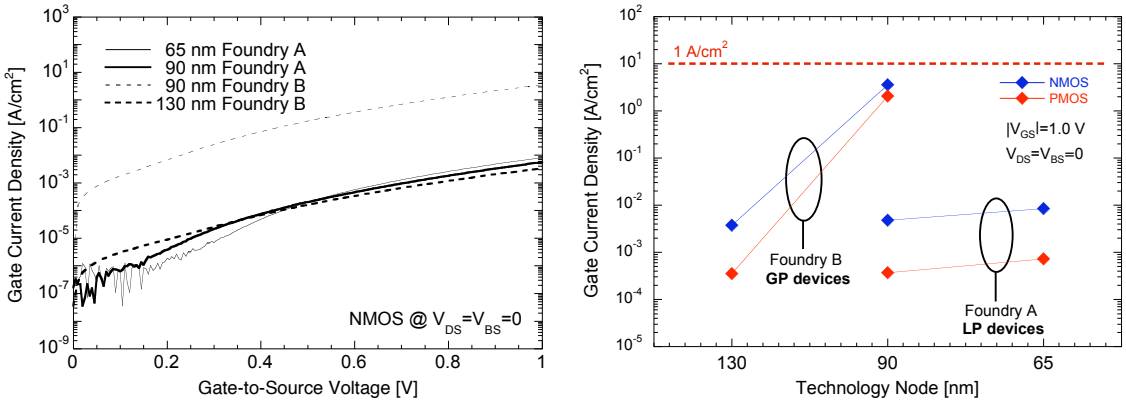


**Figure 2:** (left) gate current density as a function of the gate-to-source voltage $V_{GS}$ for NMOSFETs from two different foundries and different CMOS nodes and (right) mean values of the gate current density obtained from devices belonging to different foundries and different CMOS nodes, and measured at gate-to-source voltage $|V_{GS}|$=1.0 V.

carriers randomly crossing a potential barrier, results in an increase of the static power consumption for digital circuits and might degrade noise performance in analog applications, because of the shot and $1/f$ noise contributions associated to $I_G$ [6]. Figure 2 shows measured values of the gate current density ($I_G$ normalized to the device gate area) for NMOS and PMOS devices belonging to different nodes and manufactured by different foundries. The plot shows how the gate current density varies between the two 90 nm processes from different foundries and with different flavors. Measured values relevant to the 65 nm process are well below the commonly used limit of 1 A/cm$^2$, as expected for the Low Power flavor of this node.

### 2.3 Analysis of noise parameters

In the investigated 65 nm technology the gate-referred noise voltage spectra were measured for PMOS and NMOS with different gate widths and lengths and at different drain currents. The gate referred noise voltage spectrum of a CMOS device can be modeled by means of the following equation [7]:

$$S_e^2(f) = S_W^2 + S_{1/f}^2 = 4k_BT\frac{\Gamma}{g_m} + \frac{K_f}{C_{ox}WL}\frac{1}{f^{\alpha_f}}. \tag{2.2}$$

The first term is typically dominated by thermal noise in the device channel, $g_m$ is the device transconductance, $k_B$ is the Boltzmann's constant and T is the absolute temperature. The value of the $\Gamma$ parameter depends on the degree of channel inversion and on the effect of the bulk on the transconductance $g_m$. It also takes into account possible excess noise contributions, which in deep-submicron devices may be related to short channel effects. The second term is relevant to the fluctuations of the $1/f$ type in the drain current $I_D$ and includes the $1/f$ noise intrinsic coefficient $K_f$ and the coefficient $\alpha_f$, which accounts for the slope of the low frequency portion of the spectrum in log-log plots. In order to get more insight into the white noise behavior, it is possible to evaluate



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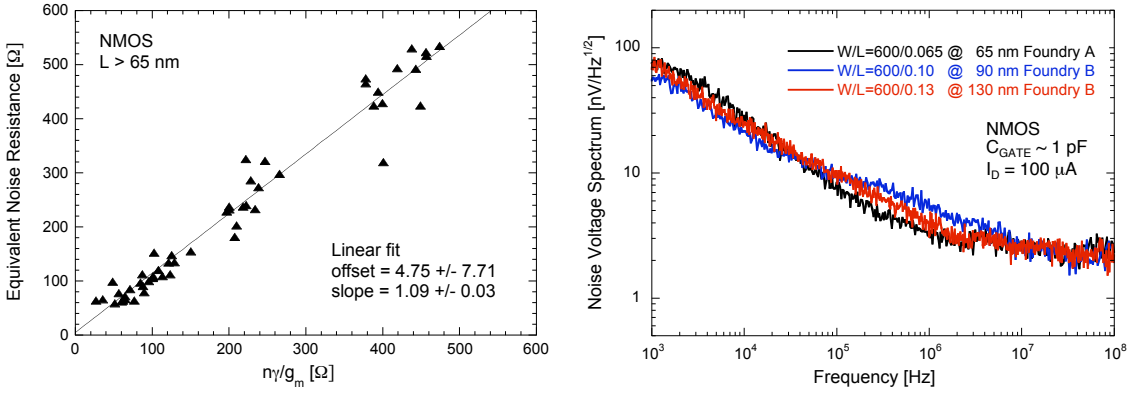


**Figure 3:** (left) equivalent channel thermal noise resistance $R_{eq}$ for NMOS devices ($V_{DS}$=0.6 V) and (right) noise voltage spectra of NMOS with same gate capacitance belonging to the 130, 90 and 65 nm CMOS technology nodes.

it in terms of the equivalent channel thermal noise resistance, $R_{eq}$, whose expression is given by:

$$R_{eq} = \frac{S_W^2}{4k_BT} = \frac{\Gamma}{g_m} = \alpha_W \frac{n\gamma}{g_m}, \tag{2.3}$$

where $\alpha_W$ is an excess noise factor [8] and $\gamma$ ranges from 1/2 in weak inversion to 2/3 in strong inversion. In Figure 3 (left), $R_{eq}$ is plotted as a function of $n\gamma/g_m$ for NMOS devices featuring a channel length greater than the minimum allowed by the technology. Values of the subthreshold slope $n$ in the range 1.2-1.3 have been obtained from static measurements while the coefficient $\gamma$ is calculated for each $I_D$ value by means of the equations proposed in [9]. According to (2.3) the slope of the fitting straight line determines the $\alpha_W$ coefficient while its offset with the origin is related to contributions from parasitic resistances. The extrapolated value of $\alpha_W$ is close to unity (except for MOSFETs with L=65 nm, where $\alpha_W \approx$1.3), indicating that no sizeable short channel effects could be ascribed to the considered operating conditions. Noise contributions from parasitic resistances turn out to be negligible too. A comparison of noise for different CMOS nodes is carried out in Figure 3 (right), showing noise voltage spectra for NMOSFETs from 130 nm, 90 nm and 65 nm CMOS processes, biased at $I_D$=100 $\mu$A. The fact that NMOSFETs featuring approximately the same value of $WLC_{OX}$ exhibit a similar $1/f$ noise points out that the value of the $K_f$ parameter changes little across different CMOS generations. In the case of PMOSFETs, scaling down to the 65 nm node appears to have a different impact on $1/f$ noise: in particular, we found that P-channel devices have a very similar noise voltage spectrum as compared to N-channel devices across the entire frequency range. We may conclude that scaling to the 65 nm process does not affect noise performance significantly, although PMOSFETs appear to lose their $1/f$ noise advantage over NMOSFETs [10].

## 3. Evaluation of the radiation tolerance

Two different sets of DUTs were irradiated up to 5 Mrad($SiO_2$) and 10Mrad($SiO_2$) total dose with $\gamma$-rays from a $^{60}$Co source with a dose rate of about 8 rad($SiO_2$)/s. A third set was exposed to



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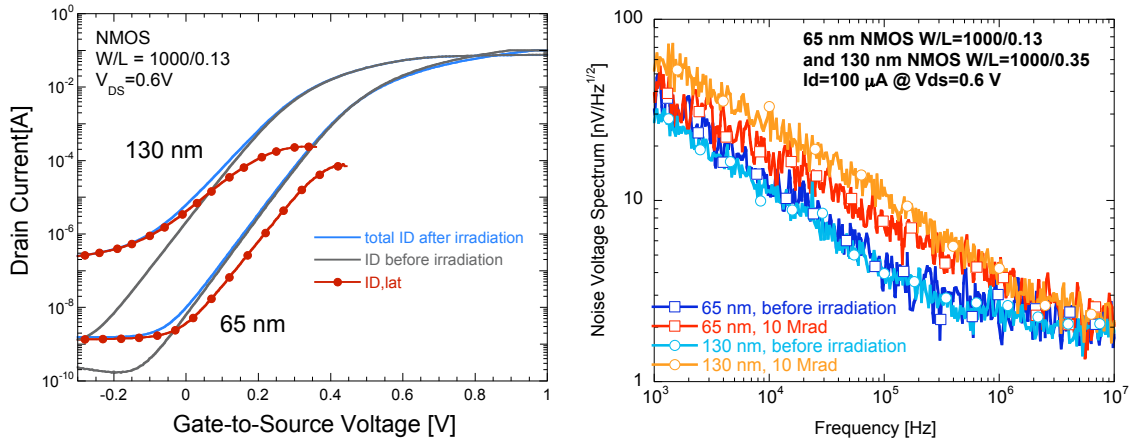


**Figure 4:** (left) drain current as a function of the gate-to-source voltage $V_{GS}$ before and after exposure to a 10 Mrad total dose of $\gamma$-rays, for NMOSFETs with W/L=1000/0.13 in the LP 65 nm process and in a 130 nm technology and (right) noise voltage spectra before and after exposure to a 10 Mrad total dose of $^{60}$Co $\gamma$-rays of NMOS transistors with similar gate capacitance in the LP 65nm and in a 130 nm process at $I_D$=100 $\mu$A.

a 5 Mrad($SiO_2$) total dose of 10 keV X-rays from a X-rays machine at Laboratori Nazionali di Legnaro (Italy) at a dose rate of 500 rad($SiO_2$)/s. The MOSFETs were biased during irradiation in the worst-case condition, that is, with the gate of N-channel devices kept at $V_{DD}$ and all other terminals grounded. In order to investigate radiation-induced degradation in the DUTs, the behavior of the $1/f$ and white noise terms, along with the main static parameters, were studied before and after irradiation. In some previous works [11, 12], of the authors discussed the total ionizing dose (TID) effects on the analog performance of CMOS technologies in the 100 nm range and demonstrated their high degree of radiation tolerance. This feature is related to the fast removal of holes from the ultrathin gate oxide of MOSFETs. On the other hand, charge trapping in the thicker shallow trench isolation (STI) oxides has been proposed as the main reason for analog performance degradation in N-channel MOSFETs exposed to ionizing radiation. Radiation-induced charge buildup in the STI oxides may invert the adjacent P-type region in the body of N-channel devices, creating a leakage path between source and drain. In a multifinger NMOS, it is possible to model this wih as lateral parasitic devices (two for each transistor finger) which add a contribution to the total drain current $I_D$ and noise of the device. Figure 4 (left) shows an example of the behavior of the total drain current, before and after exposure to a 10 Mrad total dose of $\gamma$-rays, as a function of the gate-to-source voltage for 130 nm and 65 nm NMOSFETs. The plot also shows the current $I_{D,lat}$ (whose value is obtained by subtracting the preirradiation $I_D$ from the total drain current measured after irradiation, as explained in [13]) flowing in the lateral parasitic device. The drain current is more severely affected by sidewall leakage in the 130 nm technology as compared to the 65 nm one. This could be explained by a higher doping concentration in the P-type body for the 65 nm process, which mitigates the inversion of the surface along the STI sidewalls. In Figure 4 (right), the radiation effects on noise are evaluated for an NMOS device with W/L=1000/0.35 belonging to a 130 nm technology and for an NMOS with W/L=1000/0.13 belonging to the 65 nm LP process. Noise voltage spectra are very similar before irradiation since the devices have a similar gate ca-



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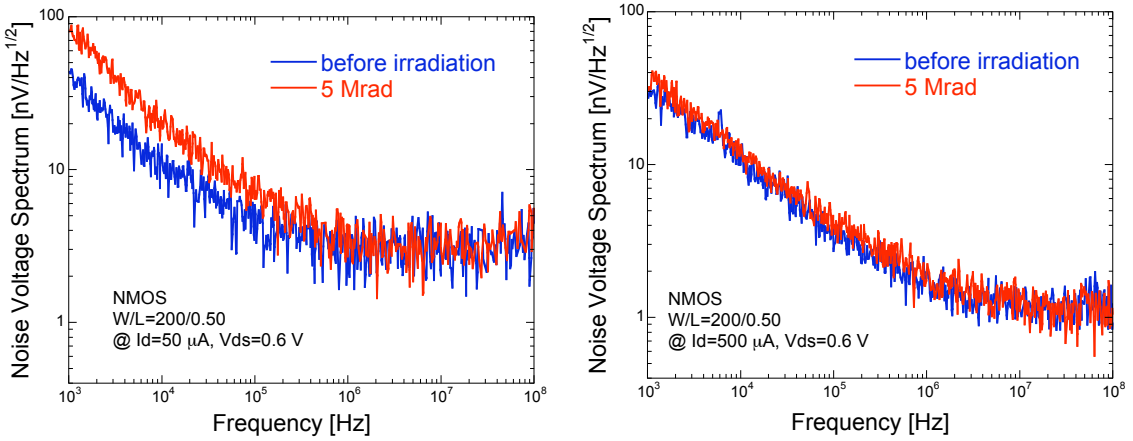


**Figure 5:** noise voltage spectra before and after exposure to X-rays (5 Mrad integrated dose) for an NMOS at $I_D$=50 $\mu$A (left) and $I_D$=500 $\mu$A (right).

pacitance $C_G$=$C_{OX}$WL. After irradiation, the $1/f$ noise increase is smaller for the 65 nm transistor. As discussed for $I_{D,lat}$ in Figure 4 (left), this may be related to the larger impact of lateral parasitic transistors on noise performance in the case of the 130 nm technology. Figure 5 shows the noise voltage spectra of 65 nm NMOSFETs with W/L=200/0.5, measured before and after exposure to ionizing radiation. After the irradiation, the behavior of the noise voltage spectrum in the 65 nm devices is similar to what we observed in previous CMOS generations. Channel thermal noise is not sizably affected by ionizing radiation, whereas a moderate $1/f$ noise increase is detectable in devices operated at low drain current density, as depicted in Figure 5 (left). At higher current density, changes in the low-frequency portion of the spectrum are almost negligible, as shown in Figure 5 (right). This is related to the larger effects that lateral parasitic devices have at low current densities on the overall properties of NMOSFETs. Irradiation effects on static, signal and noise characteristics of P-channel devices are negligible too, as observed in less scaled technologies. Data analysis does not point out any novel radiation damage mechanism which could be related to the technological advances associated with the process we examined in this work and confirms the high degree of tolerance to ionizing radiation that appears to be typical of sub-100 nm CMOS technologies.

## 4. The Apsel65 chip

A prototype chip, named Apsel65, has been designed in a 65 nm technology provided by IBM. The Apsel65 is a proof-of-principle prototype which may help estimate the impact of nanoscale CMOS technologies beyond the 100 nm frontier on the main parameters of front-end electronics for pixel detectors. The prototype chip includes two Deep N-Well (DNW) Monolithic Active Pixel Senosors (MAPS) matrices, featuring a 40 $\mu$m pixel pitch, and a fast front-end (FFE) conceived for the readout of high resistivity pixels. In the DNW MAPS, the collecting electrode consists of a deep N-well integrating part of the front-end stage in the internal P-well. This stage is physically overlapped with the area of the sensitive element, allowing a more complex pixel-level readout



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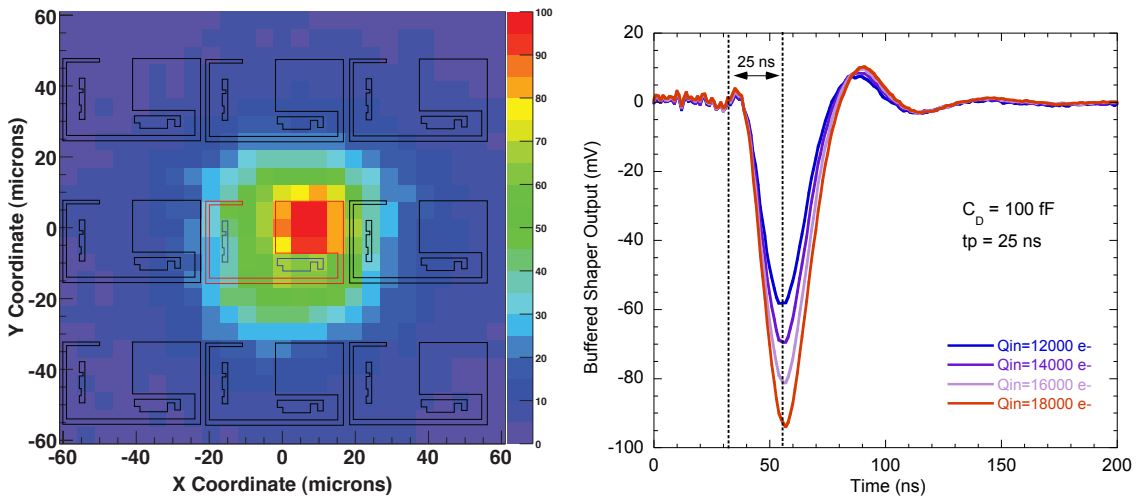


**Figure 6:** (left) charge collected by the central pixel of M1 matrix as a function of the laser position. The layout of the deep N-well and of the standard N-wells has been superimposed and (right) signal at the FFE shaper output for different values of the injected charge.

electronics. The area of PMOSFETs in the elementary cell was minimized since they are integrated in N-wells that act as competitive electrodes with respect to the main collecting one. As an example of the characterization results, the charge collected by the central pixel of the 3x3 MAPS matrix is shown in Figure 6 (left) as a function of the position of an infrared laser used to stimulate the sensor. On the right, the figure shows the FFE shaper output as a response to an input charge ranging from 12000 to 18000 electrons injected into the channel by means of an external pulser. The peaking time is close to 25 ns, in good agreement with the simulation results. More details can be found in [14]. Some information concerning CMOS MAPS, along with a comparison of different solutions, can be found in [15] and in [16], which also outlines the perspectives of CMOS pixel sensors for future HEP experiments.

## 5. AIDA: collaborative activities on the 65 nm technology

The AIDA project (Advanced Infrastructure for Detectors at Accelerators) is a European FP7 project, started in February 2011, with the aim of addressing the creation, improvement and integration of key research infrastructures in Europe, developing advanced detector technologies for future particle accelerators as well as transnational access to facilities that provide these research infrastructures [17]. The project is composed by nine work packages, which can be grouped into three types: networking (WP2, 3, 4), transnational access to facilities (WP5, 6, 7) and construction and improvement of infrastructures (WP8, 9). In the framework of WP3, dedicated to Microelectronics and Interconnection Technology, the task WP3.3 is defining the plans for the creation of microelectronic libraries and mixed-signal blocks in advanced technologies to be made available to the community of users in HEP. It was decided to focus the work on two different technologies: 65 nm CMOS, and a SiGe BiCMOS process (to be selected in 2013). Work is in progress towards the submission of various blocks, including both analog (e.g.: band-gap references, biasing digi-



PoS(Vertex 2012)026

tal to analog converters, voltage regulators etc.) and digital test structures (e.g.: PLLs, IO pads, parametrizable memory blocks, SEU resistant storage elements for digital libraries etc.). CERN is working to provide by Q2 2013 a new frame contract with a foundry for the access to a 65 nm Low Power technology.

## 6. Conclusions

The 65 nm CMOS process is being considered as the technology to be used for readout ASICs development at the next generation colliders. This paper presented results relevant to the static and noise characterization and to the effects of ionizing radiation on devices belonging to a 65 nm CMOS low power technology. The behavior of the white noise term is consistent with equations valid in weak and moderate inversion, as observed in other fabrication processes. Comparison with previous CMOS nodes shows that scaling to the 65 nm process does not affect $1/f$ noise performance significantly; nonetheless, PMOSFETs appear to gradually lose their $1/f$ noise advantage over N-channel devices. Data analysis does not point out any novel radiation damage mechanism which could be related to the technological advances associated to an aggressively scaled process such as the one considered in this work. This technology validation activity is essential for the upcoming work on the design of rad-hard analog and digital blocks in 65 nm for the AIDA project. Moreover, a prototype including DNW MAPS structures and a fast front-end intended for the readout of high-resistivity pixel sensors has been submitted in a 65 nm CMOS process provided by IBM. This prototype may help estimate the impact of nanoscale CMOS technologies beyond the 100 nm frontier on the main parameters of front-end electronics for pixel detectors and will provide useful information for future submissions of larger chips.

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